PROTOCOL

for laboratory-exercise

L-C-Oscillator

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OBJECT OF MEASUREMENT:
Collpits-Oscillator with JFET(in drain-ground circuit)
Collpits-Oscillator with Transistor (collector and base circuit)

USED DEVICES:
Multimeter
Oscilloscope Tektronix

Protocol was saved on “EL-Labor Abgabeordner“ on: 01.04.2014

Task:
The task was to calculate, assemble and measure an L-C Oscillator in various forms. As first task, a Collpits oscillator with a JFET should be calculated and measured. Secondly, the same oscillator with a transistor in common collector circuit should be calculated and measured. Thirdly, and lastly, this circuit should be adapted to a common base circuit and measured.

1. Collpits oscillator with a JFET in drain ground circuit:

1.1 Measuring Up and IDss:

At first, IDss and UP needed to be measured for further calculation.

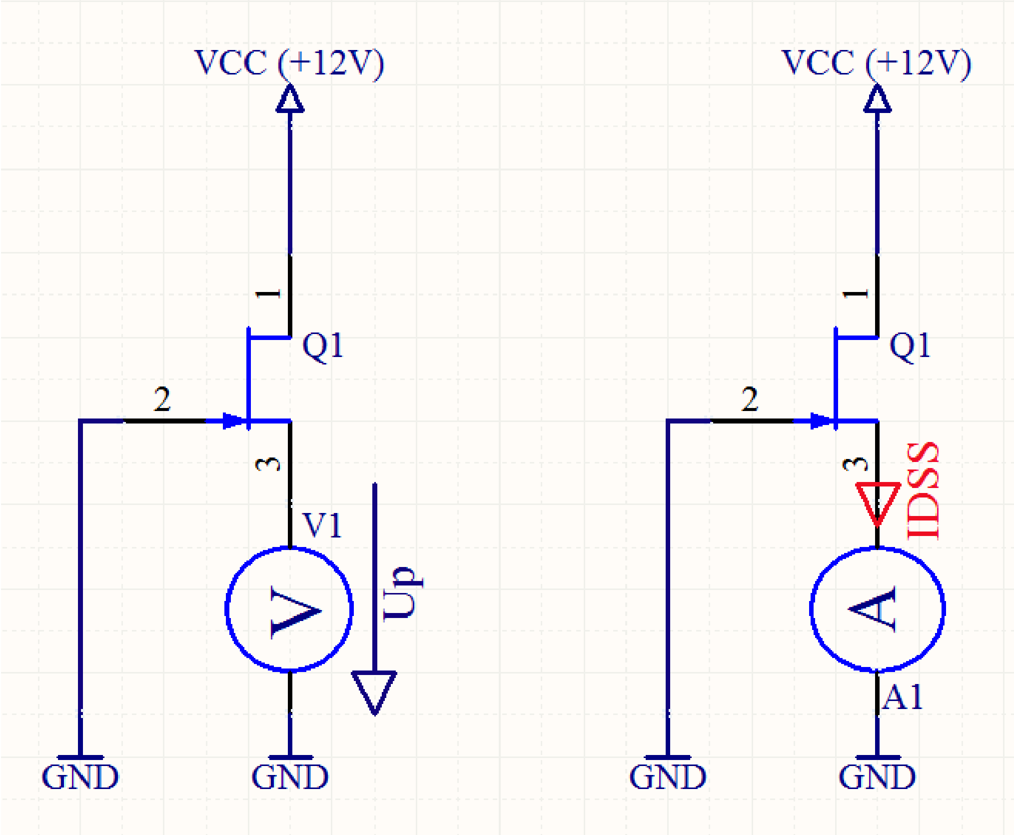

Fig.1: Measurement of Up and IDss.
With this measurements turned out, that Up was 5,64V and Idss was 17,4mA.

1.2 Calculations:

For all following calculations the values in *Tab.1* were used.

L [µH]	Ub [V]	f0[kHz]
22	12	600

Tab.1: given values.

At first, the total capacity was calculated with the following formula:

$$C_{ges} = \frac{1}{4\pi^2 {f_0}^2 L} = 3{,}1982nF$$

Next, the specific capacity was calculated. In this case, one capacitor needed to be assumed:

$$C_1 = 3 * C_2$$

That given, C2 could be calculated by following:

$$C_2 = \frac{4}{3} C_{ges} = 4{,}26nF$$
$$C_1 = 12{,}79nF$$

Now, Rs could be calculated with the previous measured values (*Fig.1*):

$$Rs = \frac{\frac{Up}{2}}{\frac{Idss}{4}} \cong 680\Omega$$

1.3 Circuit:

With the previous calculated values this following circuit was built:

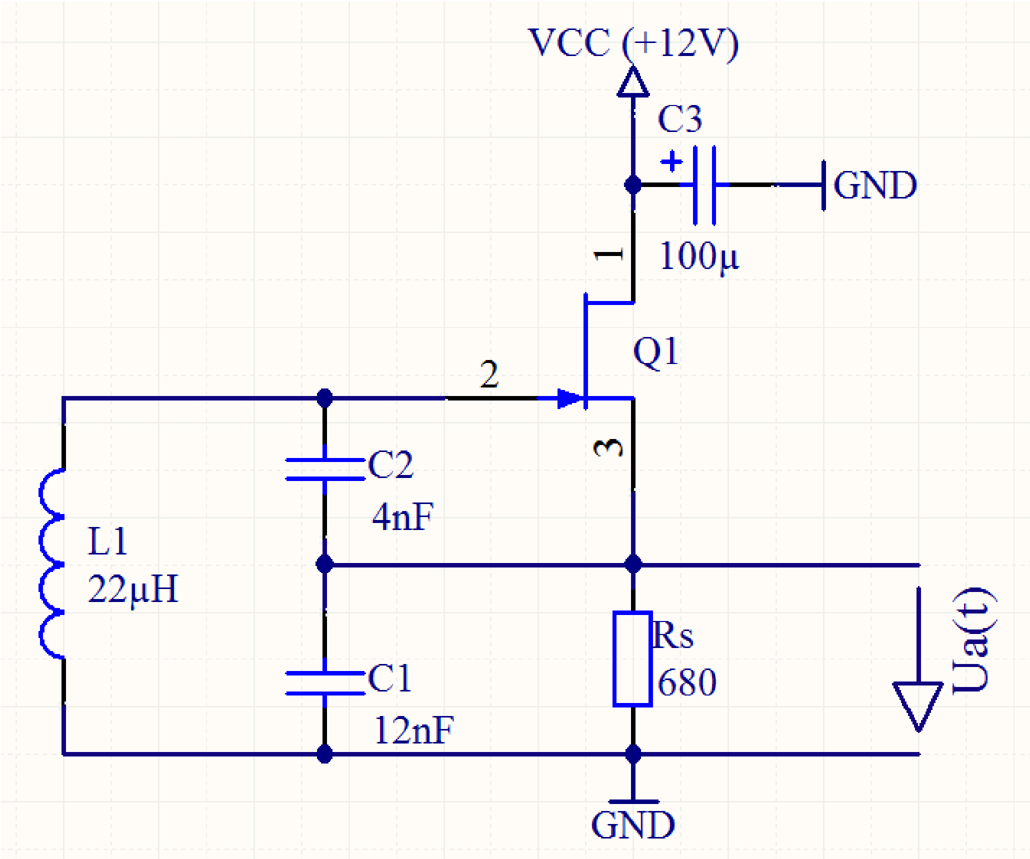

Fig.2: Colpits oscillator with JFET.

1.4 Measurements:

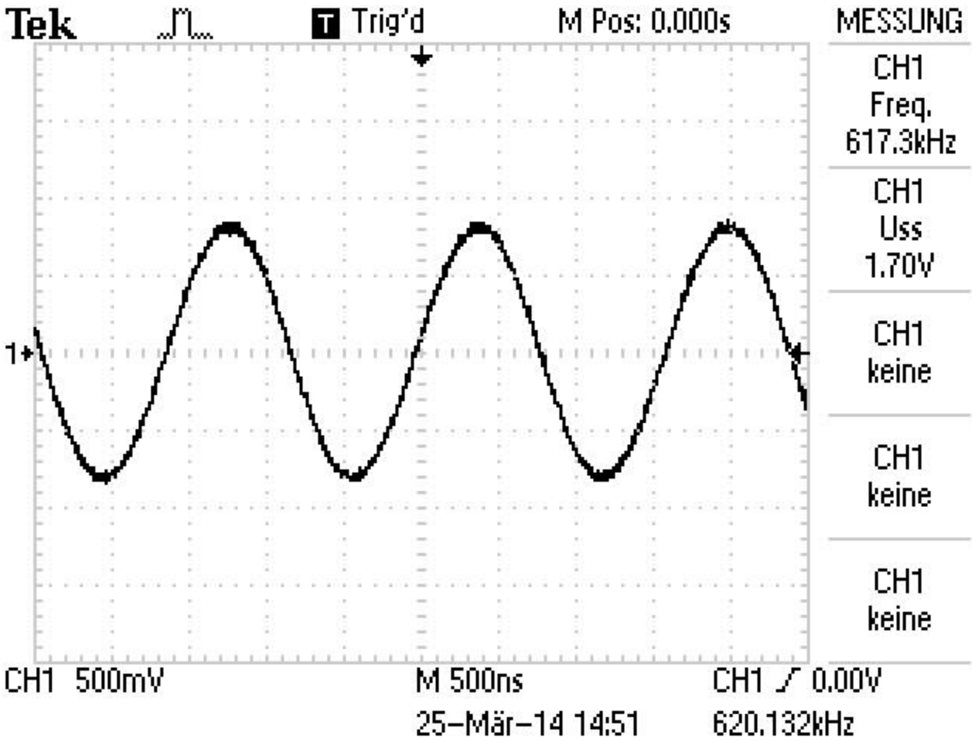

Fig.3: Signal of the calculated oscillator.

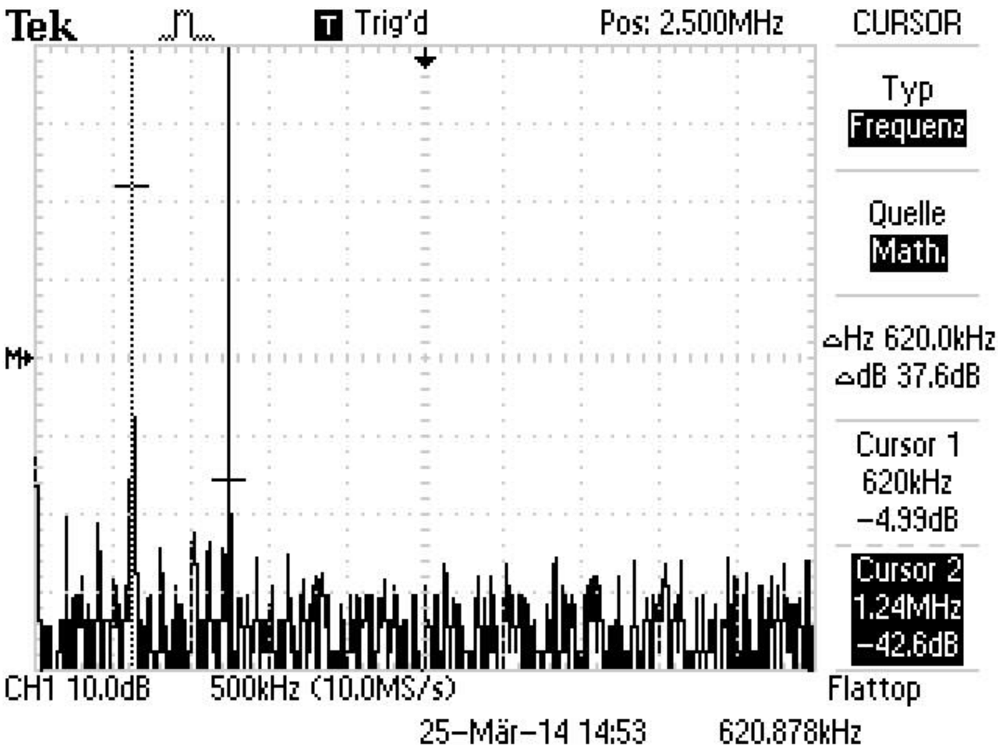

Fig.4: FFT of the oscillator.

1.5 Comment:

As seen in *Fig.4*, there are only odd harmonics. This is because of the quadratic characteristic of the JFET. Because the characteristic of the JFET is quadratic, the only possible harmonics are odd ones.

The THD is at this particular oscillator is $k = \frac{1}{75,85} * 100 = 1,32\%$.

2. Collpits oscillator with a Transistor in common collector circuit:

2.1 Calculations:

Since this oscillator should also have a 600 kHz frequency, the same values for C1, C2 and L1 were used. Only one coupling capacitor (C3), two resistors for bias point adjustment (R1, R2) and one resistor (RE) for adjusting the collector emitter current (ICE) were calculated.

Calculating the resistors for the bias point (R1, R2):
At first, VCC (+12V) was divided in the same amount onto the transistor and RE. In other words, Uce and URE were 6V each. This would result in a 1:1 voltage divider. Since UBE is about 0,6V, the voltage divider resulted in 56kΩ for R1 and 68kΩ for R2.

Calculating RE:
Now that UE is already given, only the current ICE needs to be inferred. This was done with 1mA. This equals for RE:

$$RE = \frac{UE}{ICE} = 6k\Omega \cong 5{,}6k\Omega$$

Calculating the coupling capacitor:
The frequency for calculating the capacitor was inferred 10 times lower than the oscillation frequency (60kHz).

$$T = \frac{1}{f} = 16{,}6\mu s$$

$$T = R * C$$

$$R = \frac{R1 * R2}{R1 + R2} \cong 3k\Omega$$

$$C = \frac{T}{R} = 5{,}55nF$$

2.2 Circuit:

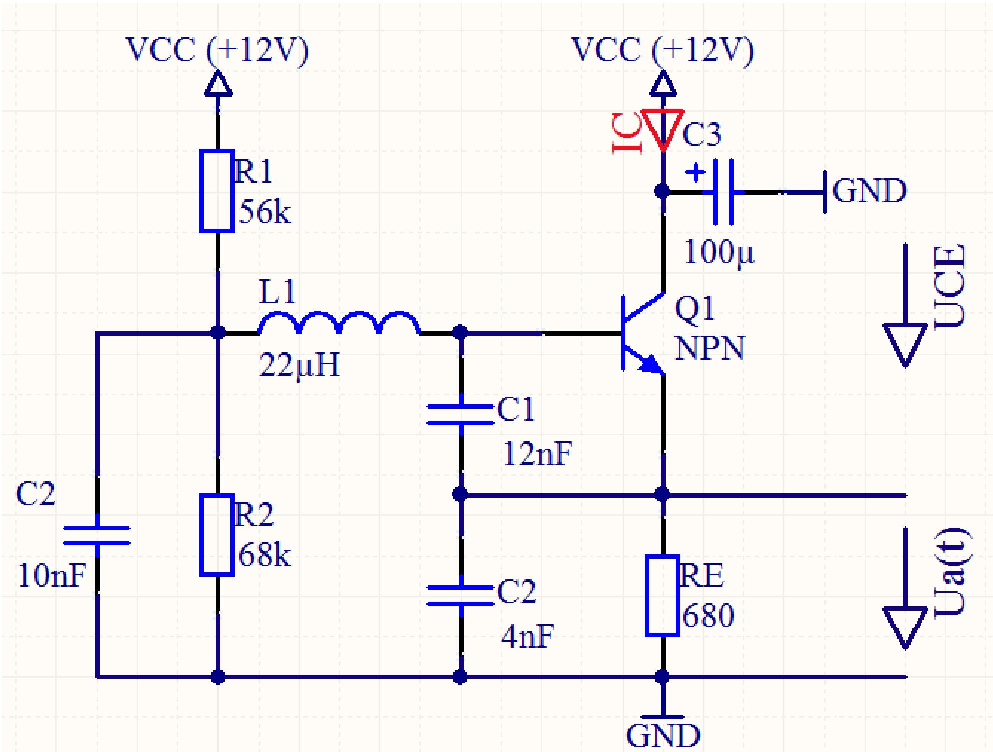

Fig.5: Collpits oscillator with a transistor

2.3 Measurements:

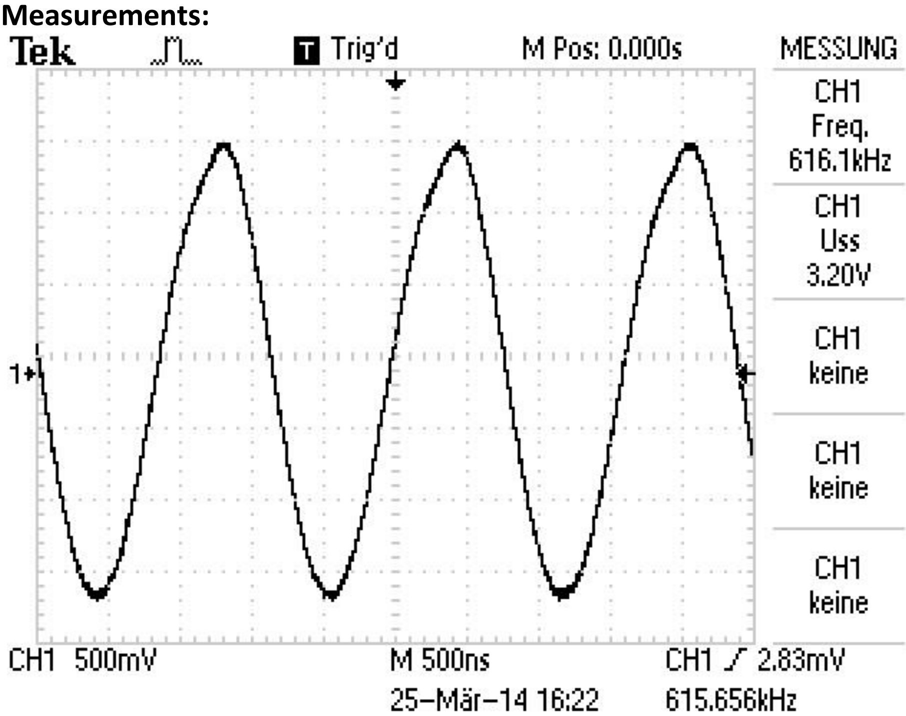

Fig.6: Signal of the oscillator with 12V supply voltage

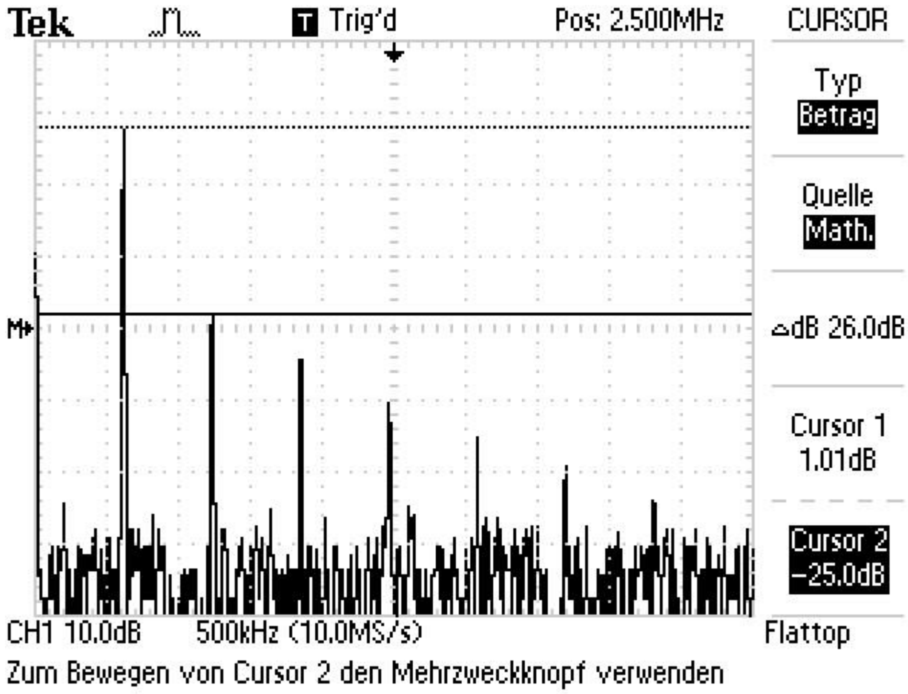

Fig.7: FFT of the oscillator with 12V supply voltage.

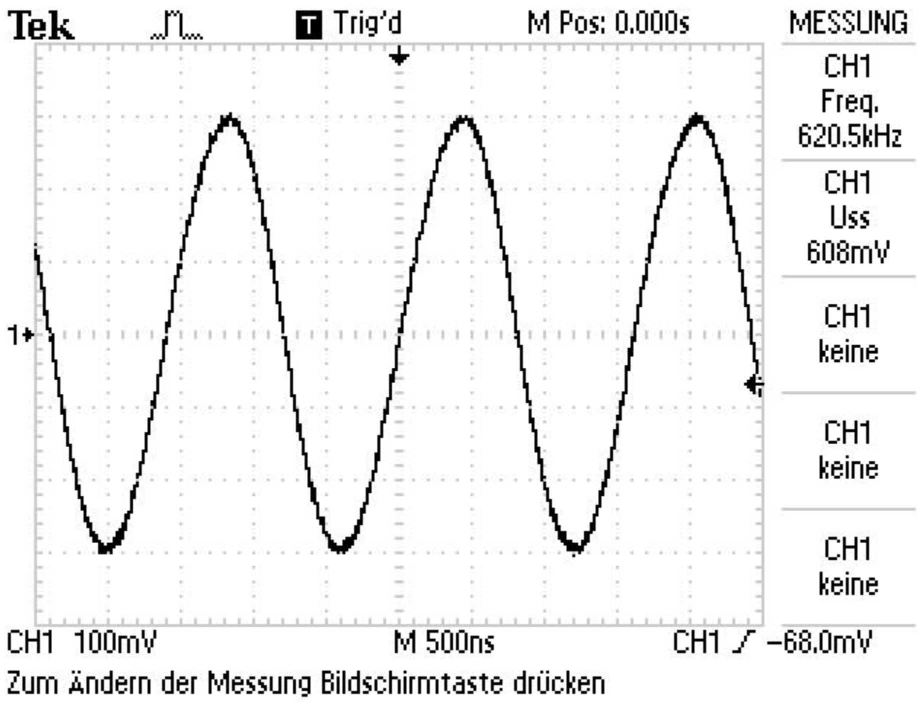

Fig.8: Signal of the oscillator with 3,3V supply voltage

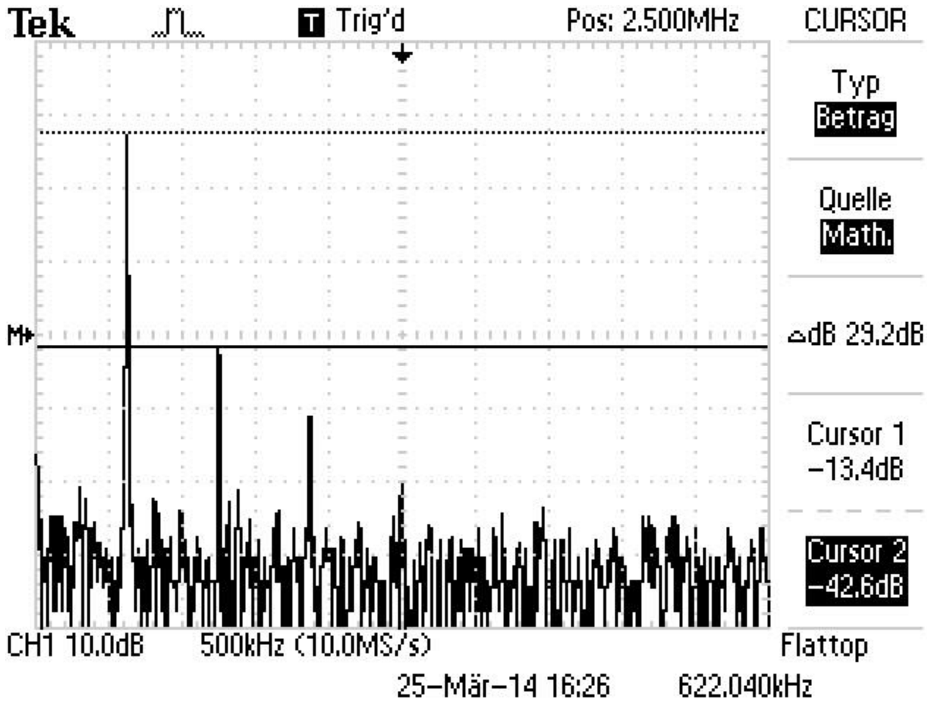

Fig.9: FFT of the oscillator with 3,3V supply voltage

2.4 Comment:

As in *Fig.6* and *Fig.7* can be seen, the signal is full of odd and even harmonics, this is why the signal is so deformed and not sinus-looking. The THD in this case is $k = \frac{1}{19,95} * 100 = 5{,}01\%$.The reason for this is the characteristic of the transistor. This problem can be partly solved simply by minimizing the supply voltage of the circuit. We found out that the best signal is delivered when the circuit is supplied with the minimum voltage (3,3V, *Fig.8, Fig.9*). With this supply voltage the THD is $k = \frac{1}{28,84} * 100 = 3{,}47\%$. Here can be proved that the THD is less when the supply is less.

3. Collpits oscillator with a Transistor in common base circuit:

3.1 Calculations:

Since this oscillator should also have a 600 kHz frequency, the same values for C1, C2 and L1 were used. Only the capacitors C3 and C4, two resistors for bias point adjustment (R1, R2) and one resistor (RE) for adjusting the collector emitter current (ICE) were calculated.

Calculating RE:
For this calculation UC and IE needs to be inferred. This was done with 1,8V and 1mA. This equals for RE:

$$RE = \frac{UE}{ICE} = 1k8\Omega$$

Calculating the resistors for the bias point (R1, R2):
Now that UE is already given, the voltage divider needs to be $UE = \frac{R2}{R1} * Uges$, which results in 100kΩ for R1 and 27kΩ for R2.

3.2 Circuit:

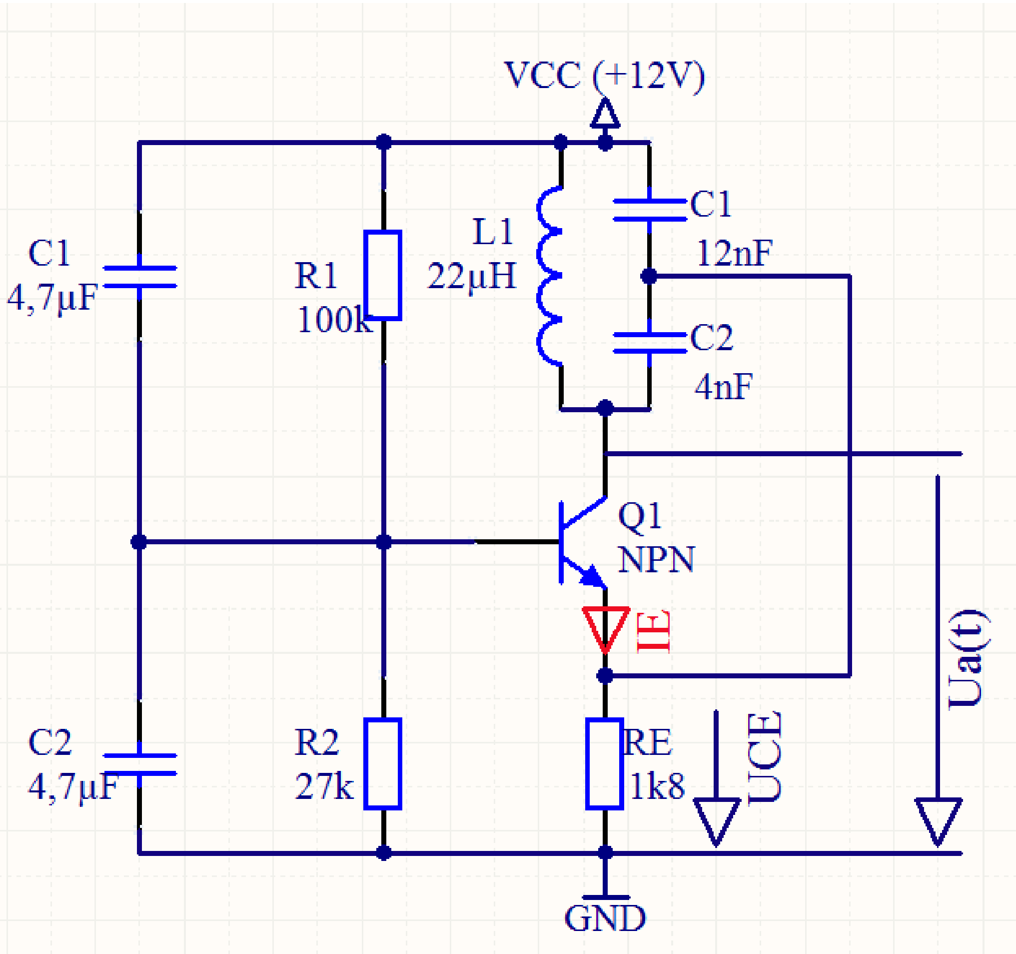

Fig.10: Collpits oscillator with transistor in common base circuit.

3.3 Measurements:

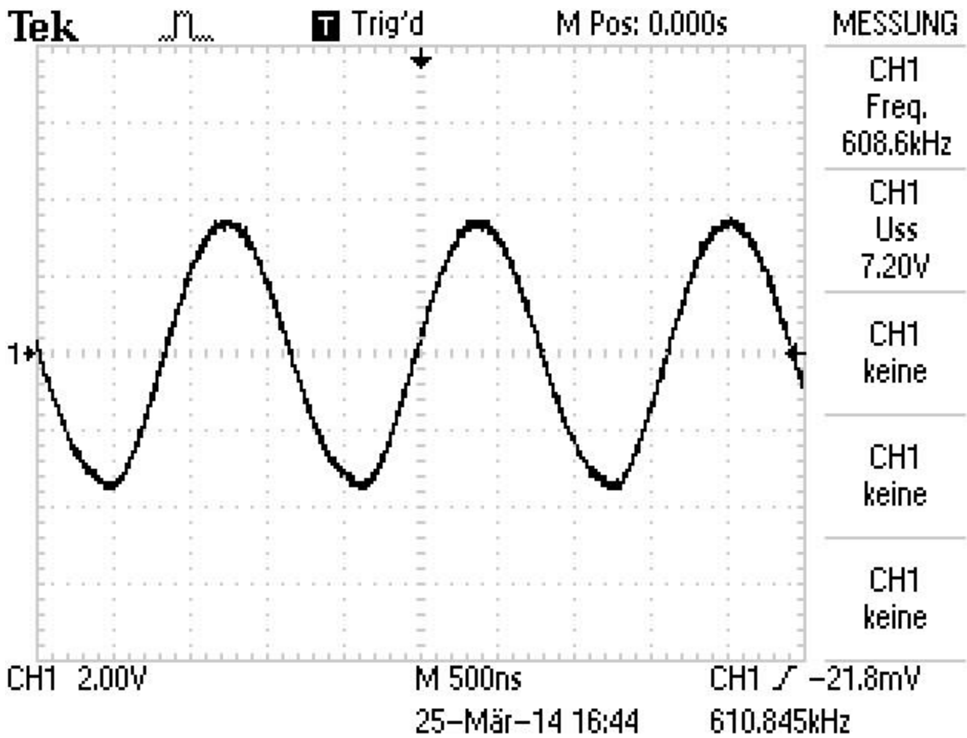

Fig.10: Signal from the collpits oscillator with transistor in common base circuit.

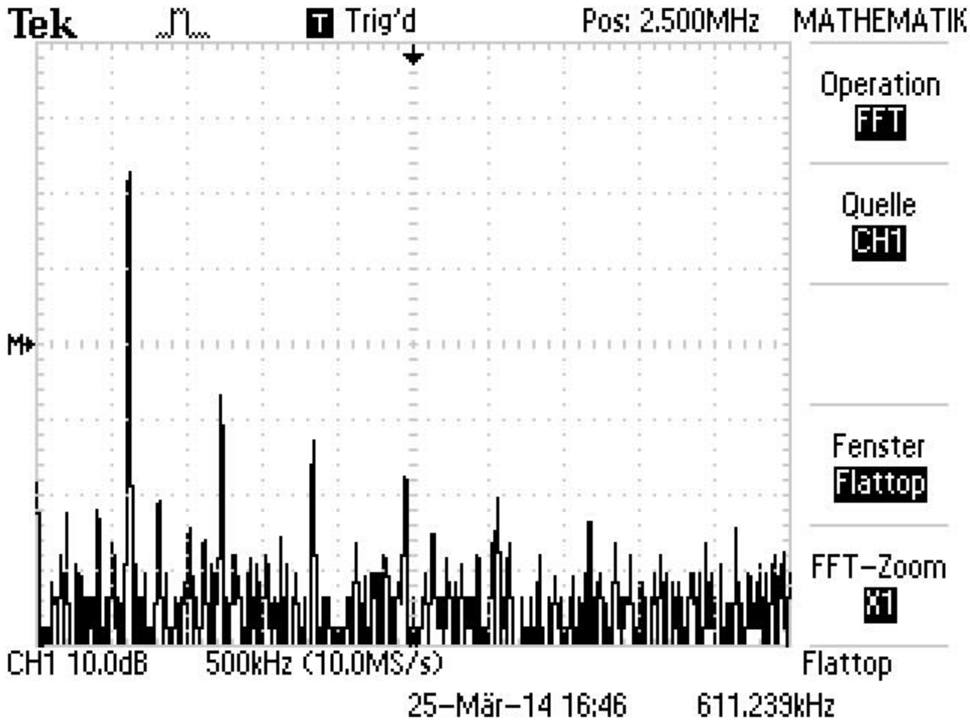

Fig.11: FFT from the oscillator.

3.4 Comment:

As seen at the second oscillator, this collpits oscillator with a transistor in common base circuitry has also odd and even harmonics. This is because of the characteristic of the transistor.

The THD at this oscillator is $k = \frac{1}{28{,}18} * 100 = 3{,}55\%$.

Compared to the JFET oscillator, the Transistor oscillator has a very high THD. This is because of the quadratic characteristic of the JFET. Because of this, there are only odd harmonics, which are less distinct. This leads to less THD.