Multiplier-Accumulator control using Voltage control oscillator (VCO)

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I. ABSTRACT

This work aims to design and implement two blocks: VCO block using *eSIM* and Multiplier-Accumulator (MAC) unit using *Makerchip* (converts Verilog code to *Ngveri* model file). Combining these two blocks will perform a Mixed Signal application as Multiplier-Accumulator control using voltage control oscillator (VCO).

II. INTRODUCTION

Mixed Signal Circuit Design using Voltage control oscillator (Analog) & MAC(Digital) blocks. Voltage control oscillator responsible for initiating by generating clocks for MAC & Counter, which provide MAC resultant as output in R3 register.

In the majority of digital signal processing applications, the critical operations are multiplication and accumulation. Real-time signal processing requires a high speed and high throughput Multiplier-Accumulator (MAC) unit, which is always a key to achieve a high-performance digital signal processing system. Furthermore, to support this we need low rise and fall time of clocks which feed to counter unit (verilog). It provides data to register R1 and R2/R1or R2 and R1or R2(any one use as constant/variable) and then passes to Accumulator/Adder block using the second clock from Voltage control oscillator.

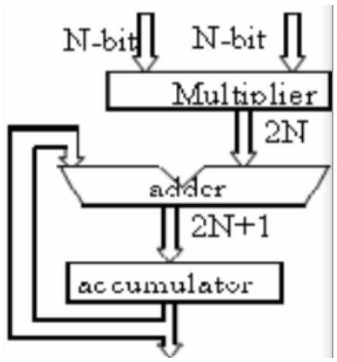
III. CIRCUIT ARCHITECTURE

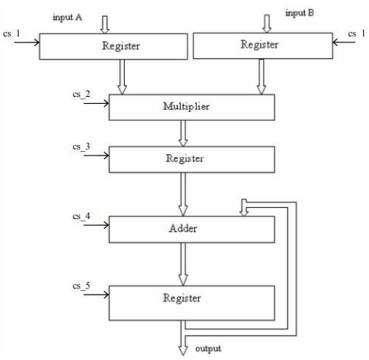
A. *Voltage control oscillator(VCO)*

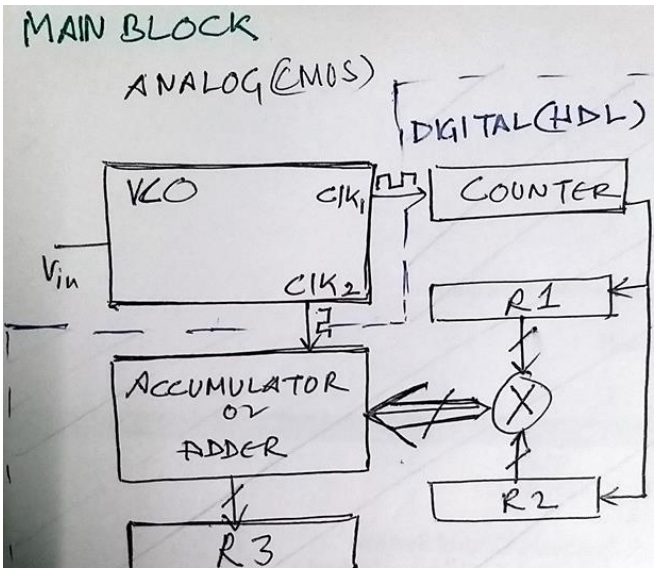
Using a ring oscillator that runs asynchronously with an external clock signal. *Fig Delay Block* shows the basic delay stage schematic used in the oscillator. *Fig VCO block* shows the complete oscillator. Here the frequency of the oscillator can be adjusted by adding or removing inverters in the delay stage. Applying a voltage to the Reference circuit will starts VCO block

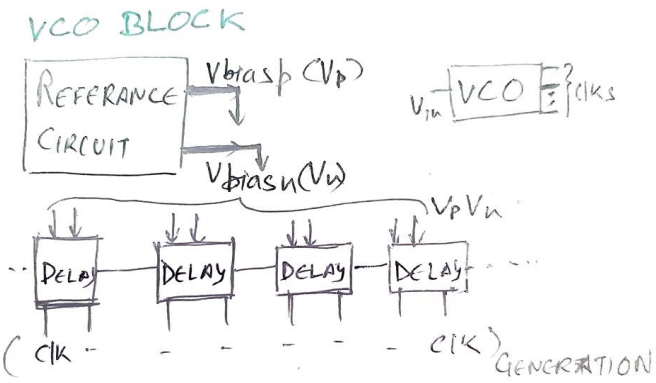
B. *Multiplier-Accumulator (Verilog)*

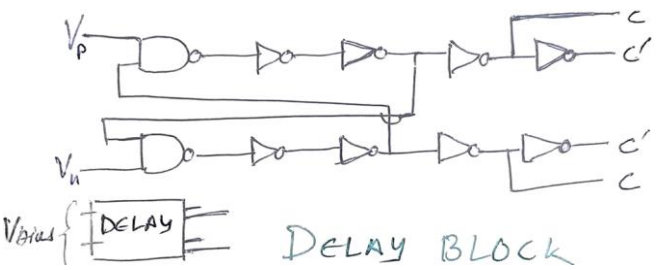
In MAC unit, data flows from the input register to the output register through multiple stages: multiplier, adder, and accumulator. During each multiplication and addition operation, the units in the MAC blocks may not be required to be on until the actual data gets in from the previous stage. On considering delay of each stage. Every block gets enabled only after some delay.











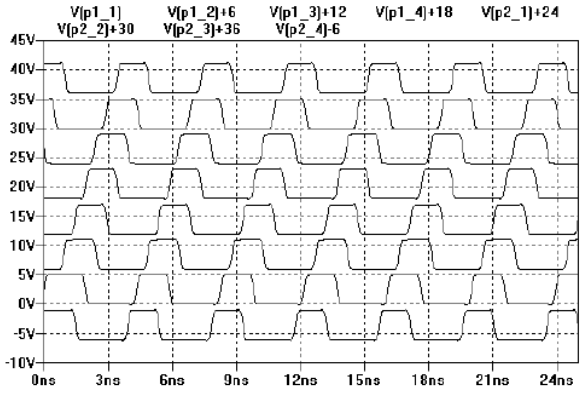


Fig. VCO Simulation

IV. REFERENCES

[1] VLSI Design and Implementation of Low Power MAC Unit with Block Enabling Technique
[2] CMOS Mixed-Signal Circuit Design, 316