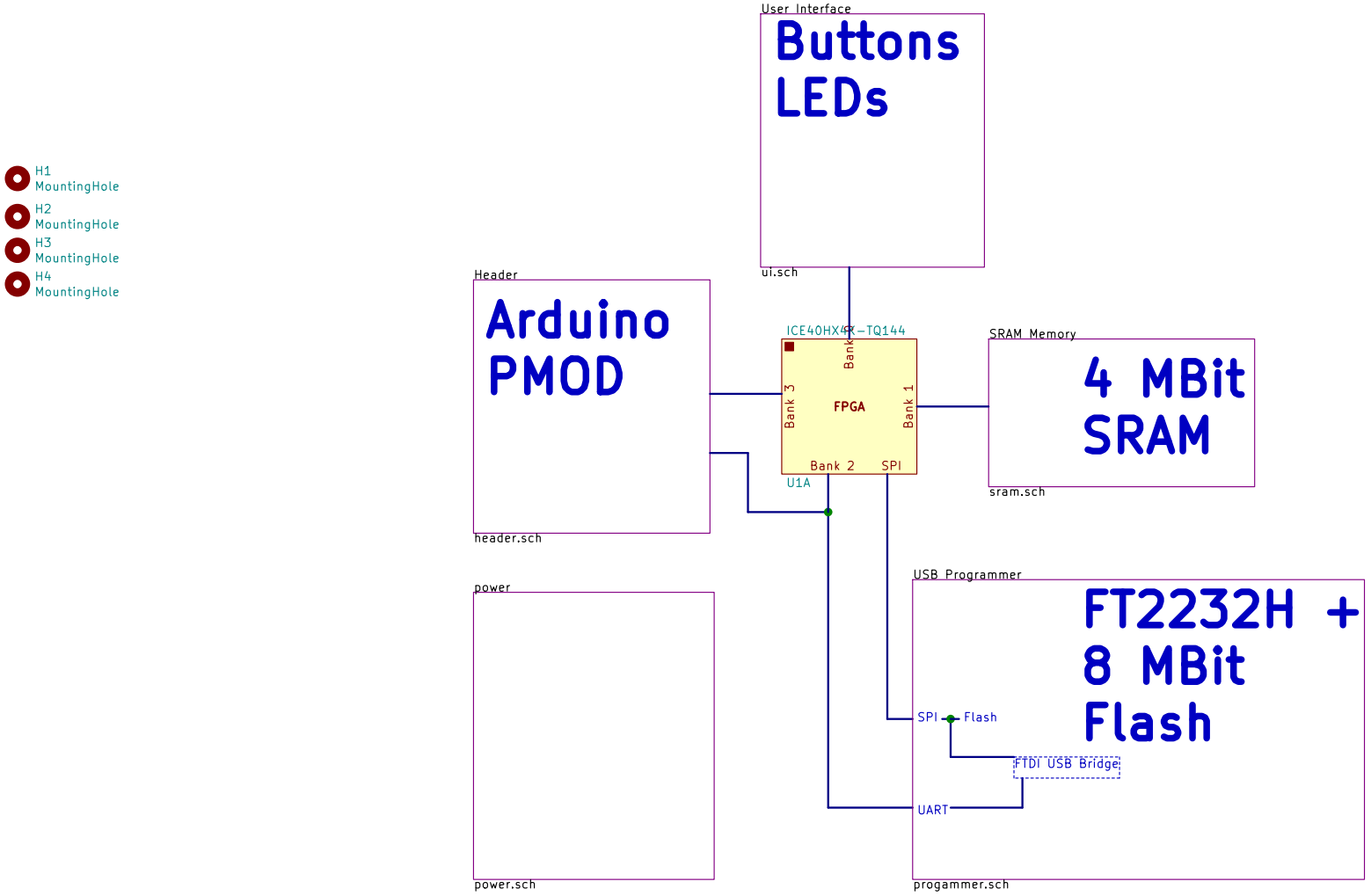

https://www.latticesemi.com/en/Products/FPGAandCPLD/iCE40

http://www.latticesemi.com//media/LatticeSemi/Documents/UserManuals/EI/icestickusermanual.pdf

http://www.latticesemi.com//media/LatticeSemi/Documents/UserManuals/EI/EB85.pdf
https://www.latticesemi.com/-/media/LatticeSemi/Documents/DataSheets/iCE/FPGA-DS-02029-3-5-iCE40-LP-HX-Family-Data-Sheet.ashx?document_id=49312
https://www.latticesemi.com/-/media/LatticeSemi/Documents/PinPackage/PackageDiagrams.ashx?document_id=213

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Size: A4	Date:	**Rev:**
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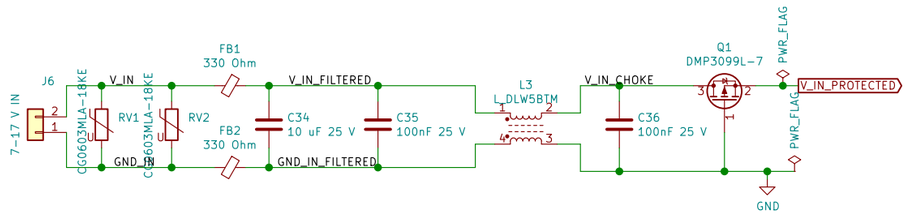
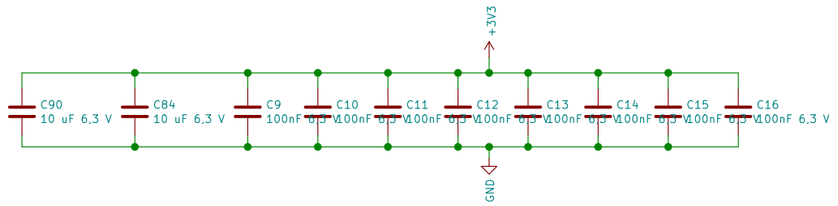
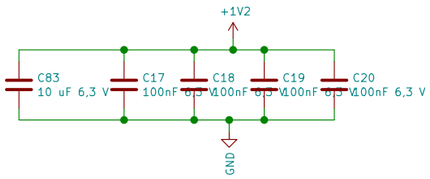
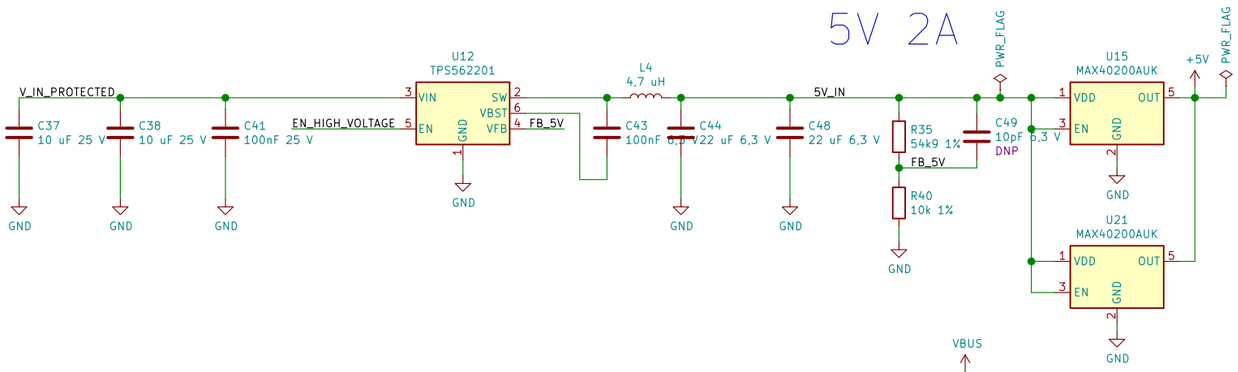
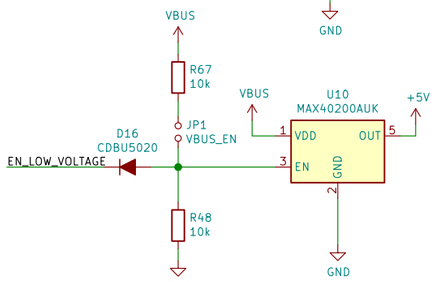


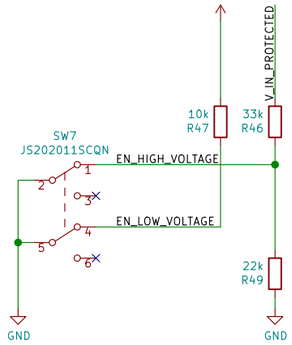


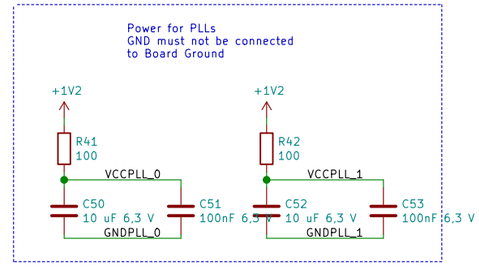


5V 2A

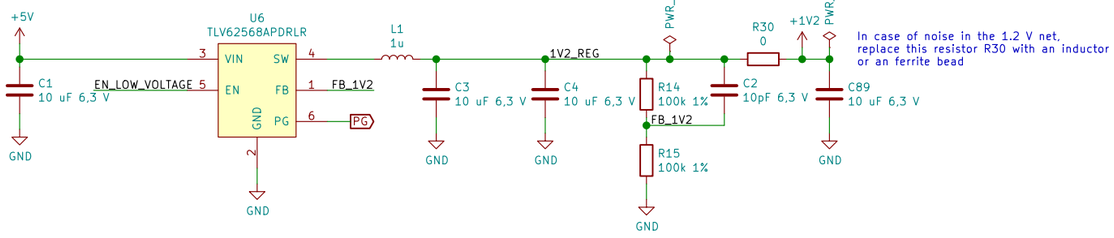




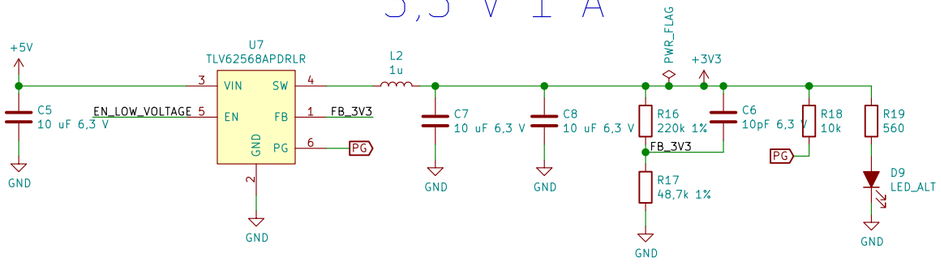




1,2 V 1 A

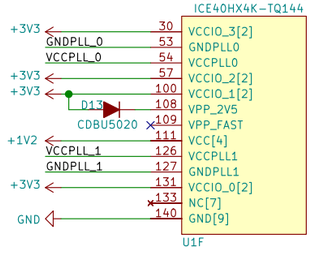


3,3 V 1 A



Note: Use TLV62568ADRLR for 2 A

Bank Power



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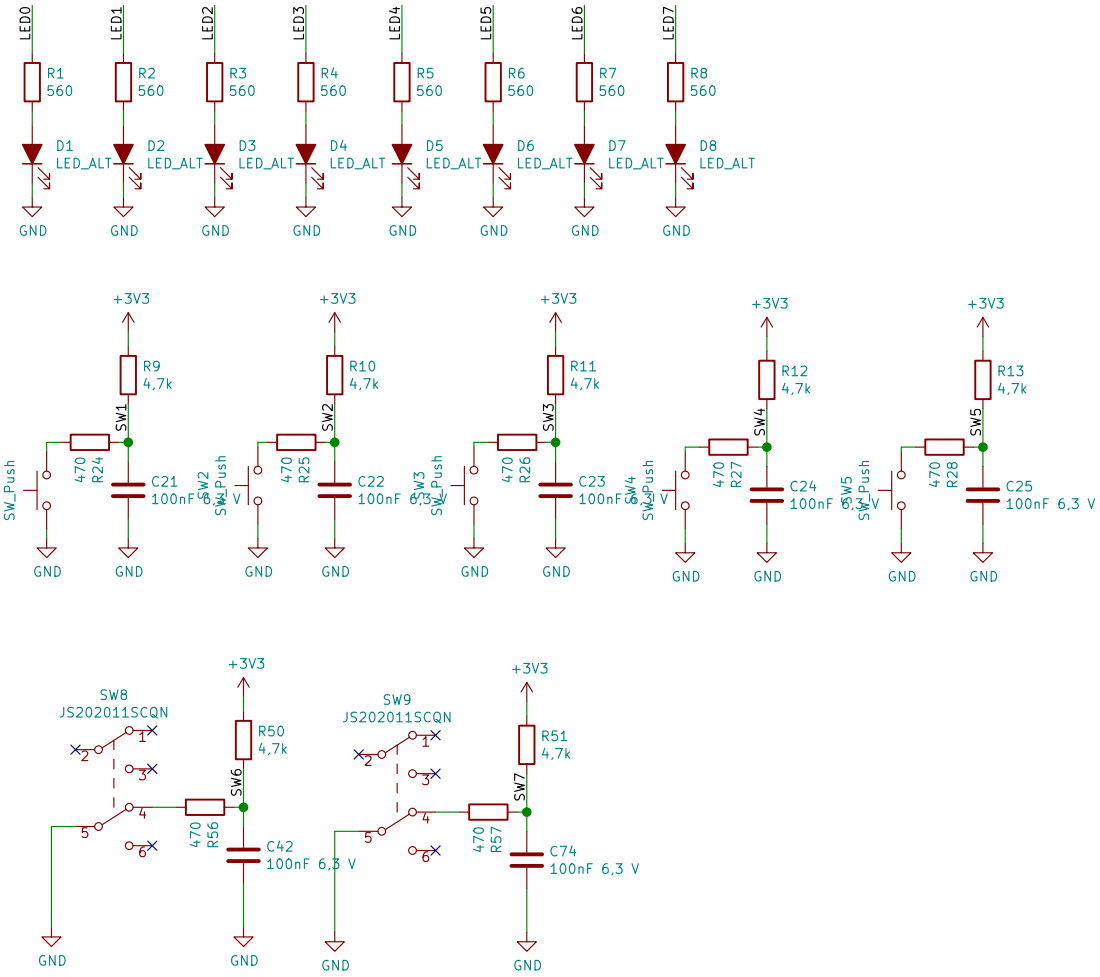
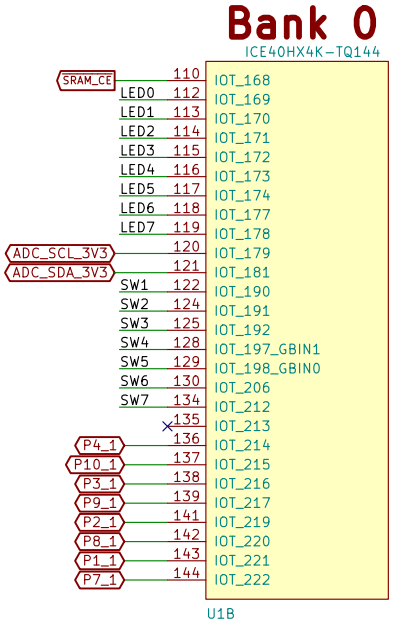
KiCad E.D.A. kicad 5.1.0		Id: 2/6





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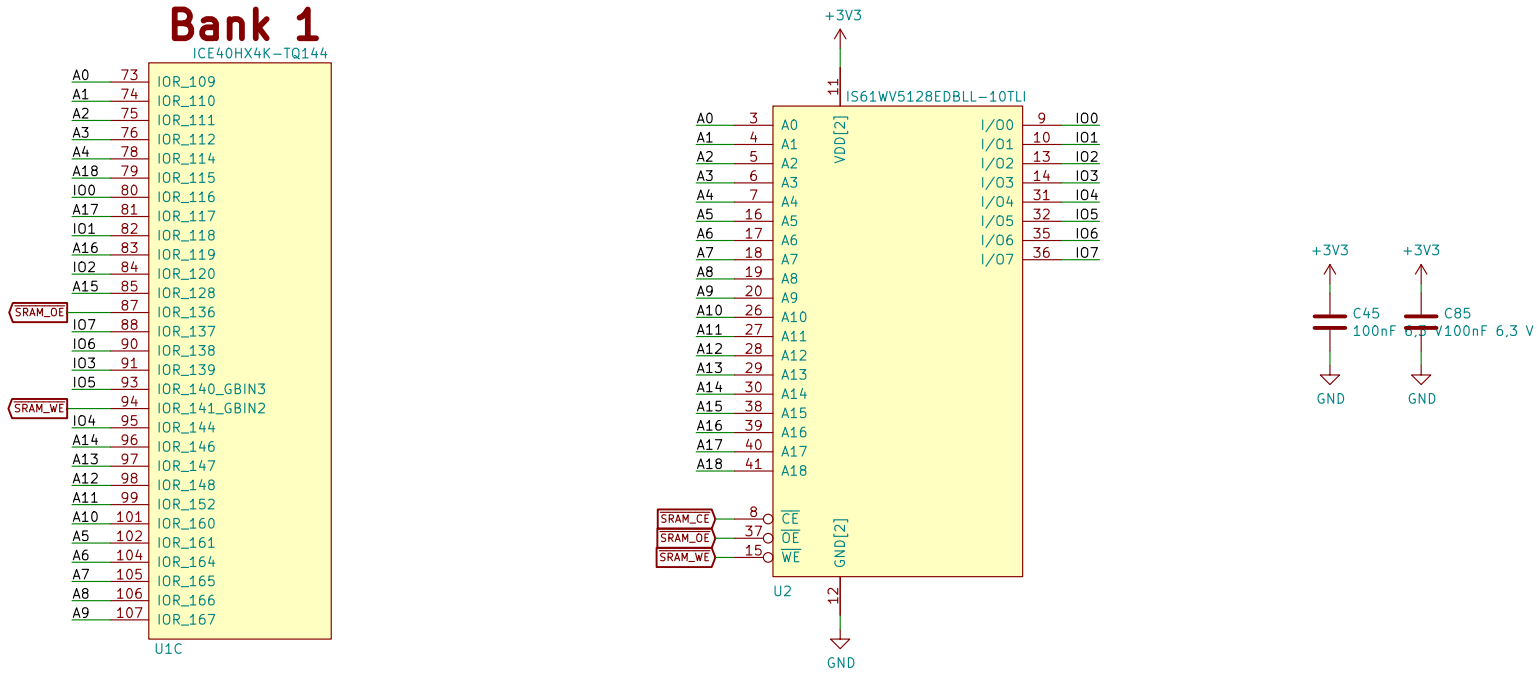
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 5.1.0		Id: 3/6



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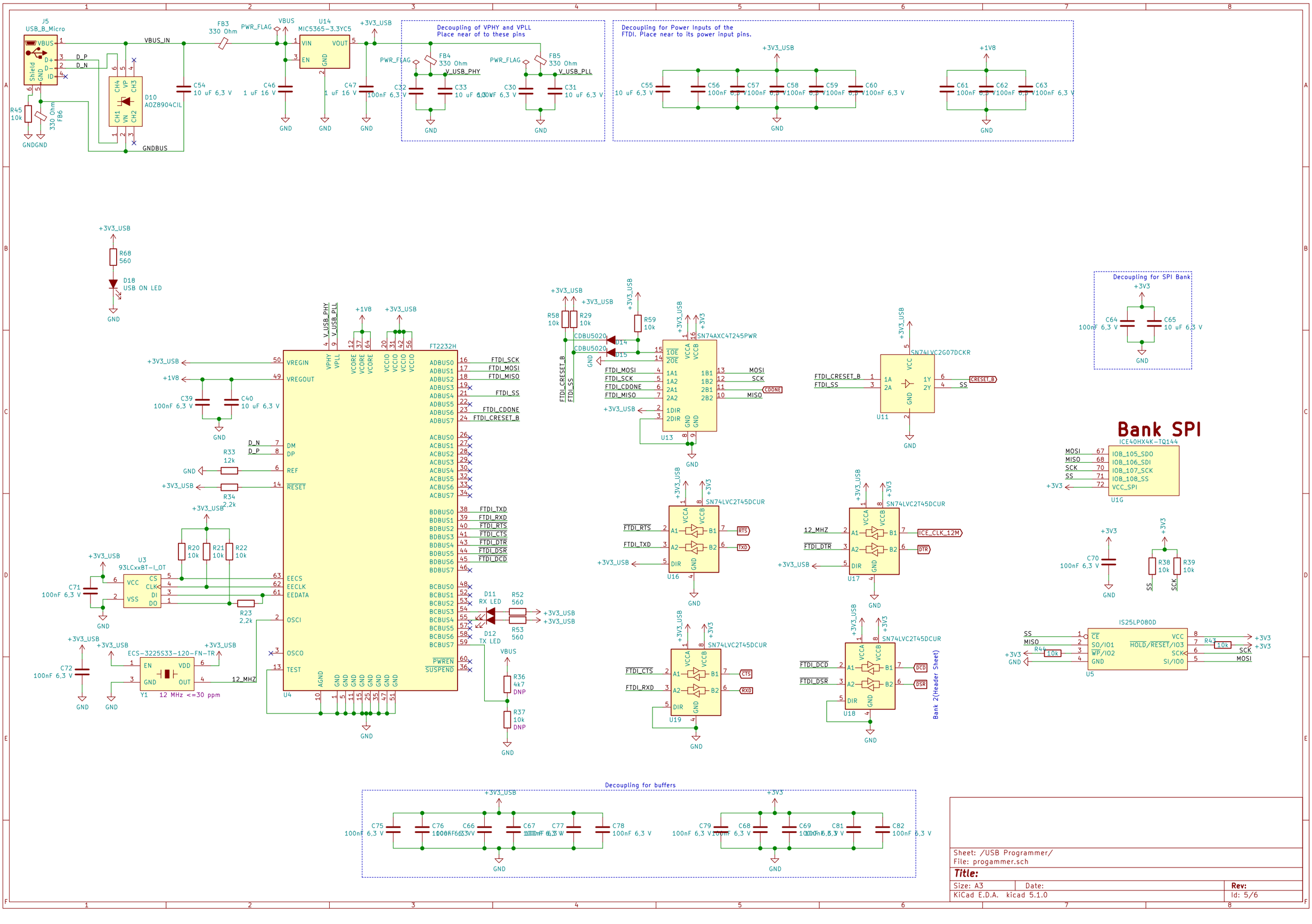
Size: A4	Date:	**Rev:**
KiCad E.D.A. kicad 5.1.0		Id: 4/6


J5
USB_B_Micro
VBUS
D+
D-
ID
Shield
GND
D_P
D_N
VBUS_IN
FB3
330 Ohm
PWR_FLAG
VBUS
U14
MIC5365-3.3YC5
VIN
VOUT
EN
GND
+3V3_USB
C54
10 uF 6,3 V
C46
1 uF 16 V
C47
100nF 6,3 V
D10
AOZ8904CIL
CH4
VP
CH3
CH1
VN
CH2
R45
10k
FB6
330 Ohm
GNDGND
GNDBUS
Decoupling of VPHY and VPLL
Place near of to these pins
FB4
330 Ohm
V_USB_PHY
FB5
330 Ohm
V_USB_PLL
C32
C33
10 uF 6,3 V
C30
C31
10 uF 6,3 V
Decoupling for Power Inputs of the
FTDI. Place near to its power input pins.
C55
10 uF 6,3 V
C56
100nF 6,3 V
C57
100nF 6,3 V
C58
100nF 6,3 V
C59
100nF 6,3 V
C60
100nF 6,3 V
+1V8
C61
100nF 6,3 V
C62
100nF 6,3 V
C63
100nF 6,3 V
R68
560
D18
USB ON LED
FT2232H
V_USB_PHY
V_USB_PLL
VREGIN
VREGOUT
VPHY
VPLL
VCORE
VCCIO
ADBUS0
ADBUS1
ADBUS2
ADBUS3
ADBUS4
ADBUS5
ADBUS6
ADBUS7
ACBUS0
ACBUS1
ACBUS2
ACBUS3
ACBUS4
ACBUS5
ACBUS6
ACBUS7
BDBUS0
BDBUS1
BDBUS2
BDBUS3
BDBUS4
BDBUS5
BDBUS6
BDBUS7
BCBUS0
BCBUS1
BCBUS2
BCBUS3
BCBUS4
BCBUS5
BCBUS6
BCBUS7
PWREN
SUSPEND
FTDI_SCK
FTDI_MOSI
FTDI_MISO
FTDI_SS
FTDI_CDONE
FTDI_CRESET_B
FTDI_TXD
FTDI_RXD
FTDI_RTS
FTDI_CTS
FTDI_DTR
FTDI_DCD
FTDI_DSR
C39
100nF 6,3 V
C40
10 uF 6,3 V
DM
DP
D_N
D_P
R33
12k
REF
RESET
R34
2,2k
R20
10k
R21
10k
R22
10k
U3
93LCxxBT-I_OT
CS
CLK
DI
DO
VCC
VSS
EECS
EECLK
EEDATA
C71
100nF 6,3 V
R23
2,2k
OSCI
OSCO
TEST
AGND
C72
100nF 6,3 V
ECS-3225S33-120-FN-TR
EN
VDD
OUT
Y1
12 MHz <=30 ppm
12_MHZ
D11
RX LED
D12
TX LED
R52
560
R53
560
R36
4k7
DNP
R37
10k
DNP
R58
10k
R29
10k
R59
10k
CDBU5020
D14
D15
SN74AXC4T245PWR
1OE
2OE
VCCA
VCCB
1A1
1A2
2A1
2A2
1B1
1B2
2B1
2B2
1DIR
2DIR
MOSI
SCK
CDONE
MISO
U13
SN74LVC2T45DCUR
U16
U17
U18
U19
RTS
TXD
CTS
RXD
DCD
DSR
ICE_CLK_12M
Bank 2(Header Sheet)
SN74LVC2G07DCKR
CRESET_B
SS
U11
Decoupling for SPI Bank
C64
100nF 6,3 V
C65
10 uF 6,3 V
Bank SPI
ICE40HX4K-TQ144
IOB_105_SDO
IOB_106_SDI
IOB_107_SCK
IOB_108_SS
VCC_SPI
U1G
C70
100nF 6,3 V
R38
10k
R39
10k
IS25LP080D
CE
SO/IO1
WP/IO2
SI/IO0
HOLD/RESET/IO3
R44
10k
R43
10k
U5
Decoupling for buffers
C75
100nF 6,3 V
C76
100nF 6,3 V
C66
100nF 6,3 V
C67
100nF 6,3 V
C77
100nF 6,3 V
C78
100nF 6,3 V
C79
100nF 6,3 V
C68
100nF 6,3 V
C69
100nF 6,3 V
C81
100nF 6,3 V
C82
100nF 6,3 V
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File: progammer.sch
Title:
Size: A3
Date:
Rev:
KiCad E.D.A. kicad 5.1.0
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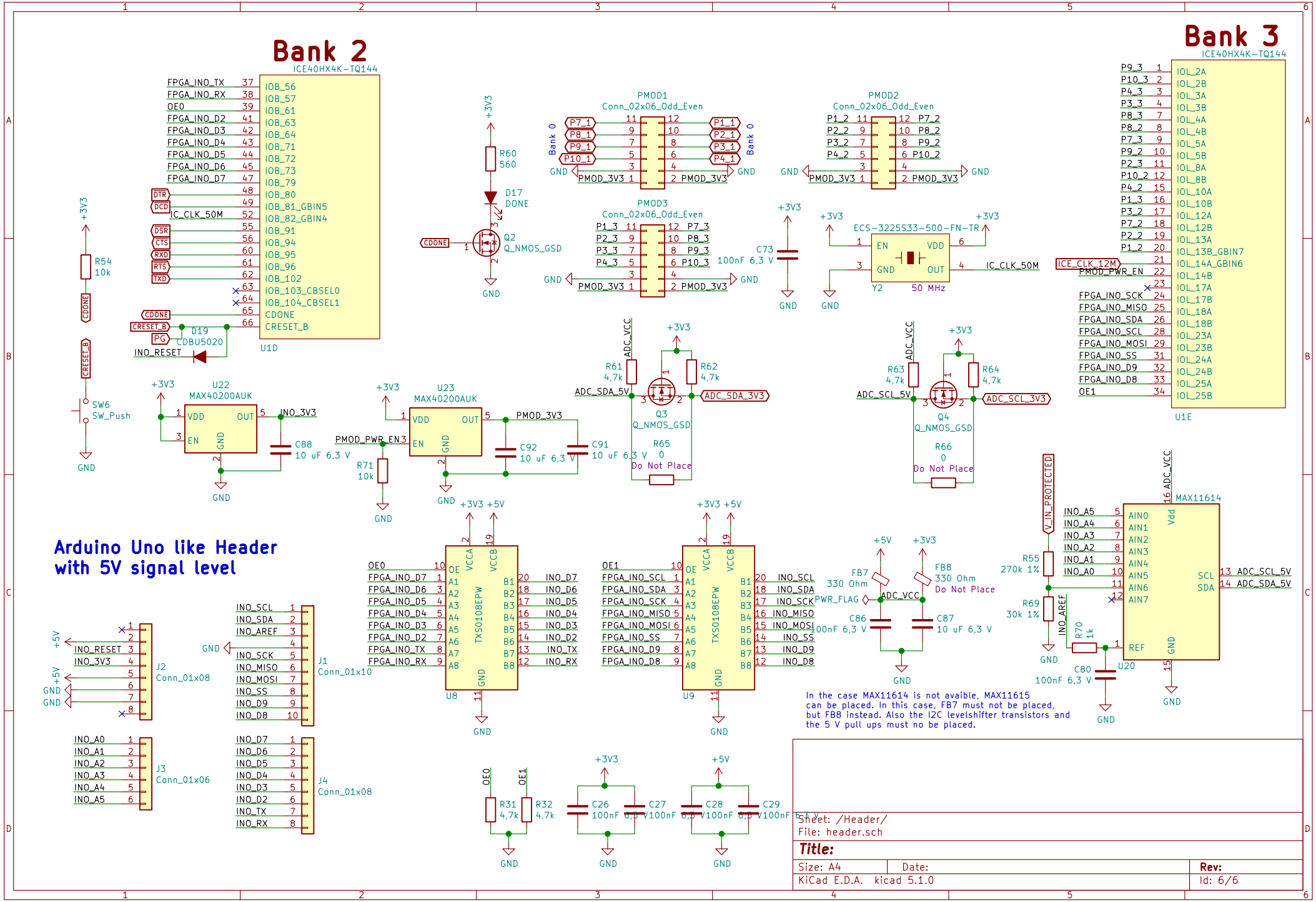
Bank 2
ICE40HX4K-TQ144
U1D
Bank 3
ICE40HX4K-TQ144
U1E
PMOD1
Conn_02x06_Odd_Even
PMOD2
Conn_02x06_Odd_Even
PMOD3
Conn_02x06_Odd_Even
ECS-3225S33-500-FN-TR
50 MHz
Y2
R60
560
D17
DONE
Q2
Q_NMOS_GSD
R54
10k
SW6
SW_Push
D19
CDBU5020
INO_RESET
U22
MAX40200AUK
U23
MAX40200AUK
C88
10 uF 6,3 V
C92
10 uF 6,3 V
C91
10 uF 6,3 V
R71
10k
R61
4,7k
R62
4,7k
Q3
Q_NMOS_GSD
R65
0
Do Not Place
R63
4,7k
R64
4,7k
Q4
Q_NMOS_GSD
R66
0
Do Not Place
C73
100nF 6,3 V
Arduino Uno like Header
with 5V signal level
J1
Conn_01x10
J2
Conn_01x08
J3
Conn_01x06
J4
Conn_01x08
U8
TXS0108EPW
U9
TXS0108EPW
FB7
330 Ohm
FB8
330 Ohm
Do Not Place
PWR_FLAG
C86
100nF 6,3 V
C87
10 uF 6,3 V
R55
270k 1%
R69
30k 1%
R70
1k
C80
100nF 6,3 V
U20
MAX11614
R31
4,7k
R32
4,7k
C26
100nF 6,3 V
C27
100nF 6,3 V
C28
100nF 6,3 V
C29
100nF 6,3 V
In the case MAX11614 is not avaible, MAX11615
can be placed. In this case, FB7 must not be placed,
but FB8 instead. Also the I2C levelshifter transistors and
the 5 V pull ups must no be placed.
Sheet: /Header/
File: header.sch
Title:
Size: A4
Date:
Rev:
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Id: 6/6