

Chapter 4: Atmel's AVR 8-bit Microcontroller

Part I – Assembly Programming

Prof. Ben Lee
Oregon State University
School of Electrical Engineering and Computer Science



Chapter Goals

- Understand how to program AVR assembly:
 - AVR architecture
 - Assembly syntax
 - Coding techniques
 - Relation between assembly and high-level language
- Bring us closer to processor hardware:
 - Assembly instructions to machine instructions
 - Binary code in memory

Contents

- 4.1 Introduction
- 4.2 General Characteristics
- 4.3 Addressing Modes
- 4.4 Instructions
- 4.5 Assembly to Machine Instruction Mapping
- 4.6 Assembler Directives
- 4.7 Expressions
- 4.8 Assembly Coding Techniques
- 4.9 Mapping Between Assembly and High-Level Language
- 4.10 Anatomy of an Assembly Program

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Part I - Assembly Programming

3

4.1 Introduction

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4

Why Microcontrollers?

- Ratio of Embedded Devices / Desktop PCs is greater than 100.
- The typical house may contain over 50 embedded processors.
- A high-end car can have over 50 embedded processors.
- **Embedded systems account for the most of the worlds production of microprocessors!**
- This chapter discusses one of the most popular microcontrollers - **Atmel's AVR 8-bit microcontrollers.**

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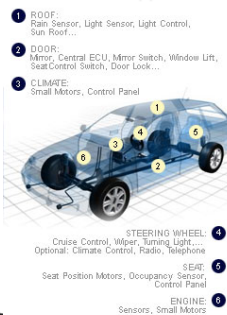
5

Some AVR-based Products

802.15.4/ZigBee LR-WPAN Devices



Automotive Applications



RFID



Motor Control



USB controller



Remote Access Controller



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6

4.2 General Characteristics

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7

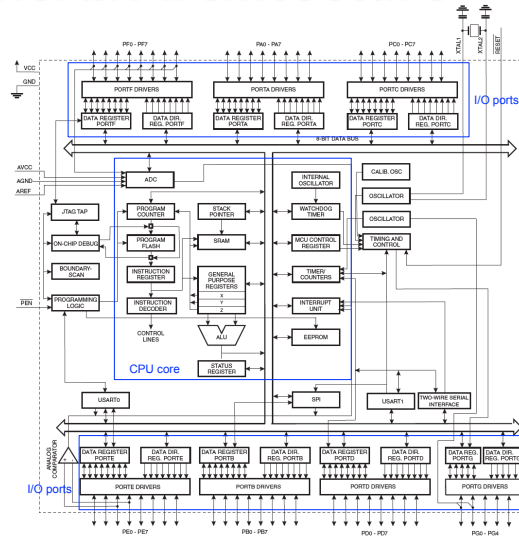
General Characteristics

- RISC (Reduced Instruction Set Computing) architecture.
 - Instructions same size
 - Load/store architecture
 - Only few addressing modes
 - Most instructions complete in 1 cycle
- 8-bit AVR Microcontroller
 - 8-bit data, 16-bit instruction
 - Used as embedded controller
 - Provides convenient instructions to allow easy control of I/O devices.
 - Provides extensive peripheral features
 - Timer/counter, USART, ADC, Serial interface, etc.

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8

General Architecture



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9

ATmega128

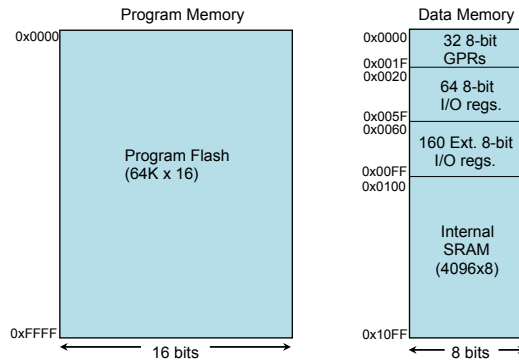
- Many versions of AVR processors.
- Our discussion based on ATmega128
 - See my textbook
 - See <http://www.atmel.com/atmel/acrobat/doc2467.pdf> (386 pages!)
- ATmega128 characteristics:
 - 128-Kbyte on-chip Program Memory
 - 4-Kbyte on-chip SRAM Data Memory (expandable to 64-Kbyte external)
 - 7 I/O ports

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10

Memory

- Separate **Program Memory** and **Data Memory**.
 - FLASH memory for program => non-volatile
 - SRAM for data => volatile



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11

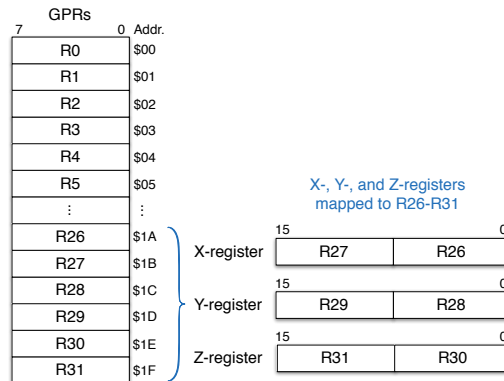
Registers

- 32 8-bit GPRs (General Purpose Registers)
 - R0 - R31
- 16-bit X-, Y-, and Z-register
 - Used as address pointers
- PC (Program Counter)
- 16-bit SP (Stack Pointer)
- 8-bit SREG (Status Register)
- 7 8-bit I/O registers (ports)

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Part 1 - Assembly Programming

12

GPRs and X,Y,Z Registers



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Part 1 - Assembly Programming

13

Status Register

Status Register (SREG)					I/O Register \$3F		
7	6	5	4	3	2	1	0
I	T	H	S	V	N	Z	C
R/W (0)	R/W (0)	R/W (0)	R/W (0)	R/W (0)	R/W (0)	R/W (0)	R/W (0)

Bit 7 - Global Interrupt Enable
 Bit 6 - Bit- Copy Storage
 Bit 5 - Half Carry Flag
 Bit 4 - Sign Bit
 Bit 3 - Two's Complement Overflow Flag
 Bit 2 - Negative Flag
 Bit 1 - Zero Flag
 Bit 0 - Carry Flag

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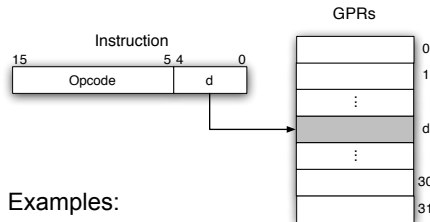
14

4.3 Addressing Modes

Addressing Modes

- Addressing mode defines the way operands are accessed.
 - Gives the programmer flexibility by providing facilities such as pointers to memory, counters for loop control, indexing of data, and program relocation
- Addressing modes in AVR:
 - Register (with 1 and 2 registers)
 - Direct
 - Indirect
 - w/Displacement (also referred to as indexed)
 - Pre-decrement
 - Post-increment
 - Program Memory Constant Addressing
 - Direct Program Memory Addressing
 - Indirect Program Memory Addressing
 - Relative Program Memory Addressing

Register Addressing (1 register)



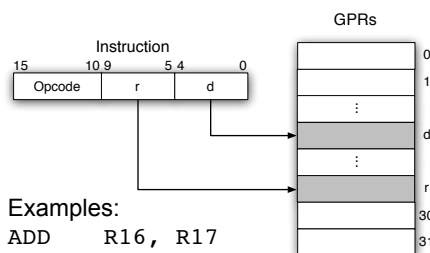
Examples:

```
INC    R16
DEC    R17
CLR    R22
```

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17

Register Addressing (2 registers)



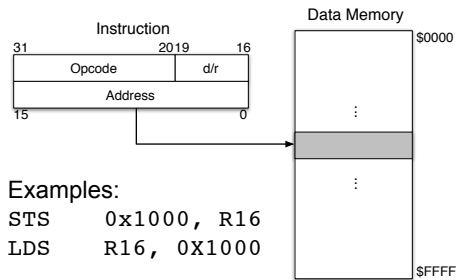
Examples:

```
ADD    R16, R17
CP     R22, R1
MOV    R0, R1
```

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Part I - Assembly Programming

18

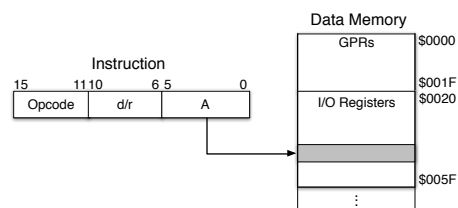
Direct Addressing



Examples:

```
STS 0x1000, R16
LDS R16, 0x1000
```

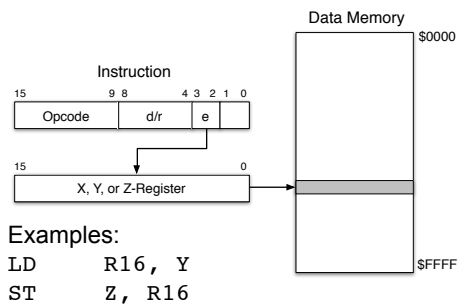
I/O Direct Addressing



Examples:

```
IN R16, PIND
OUT PORTC, R16
```

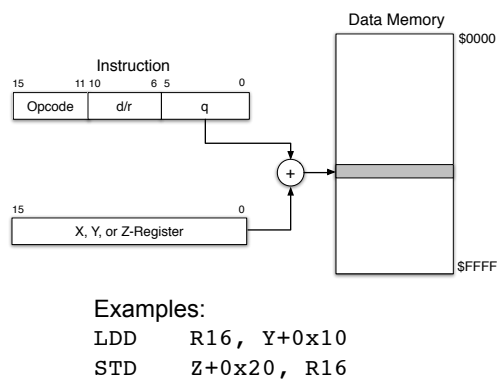
Indirect Addressing



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Part I - Assembly Programming

21

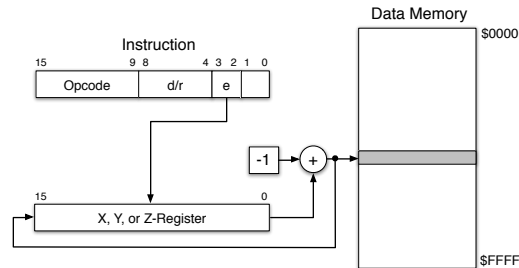
Indirect with Displacement



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22

Indirect with Pre-Decrement



Examples:

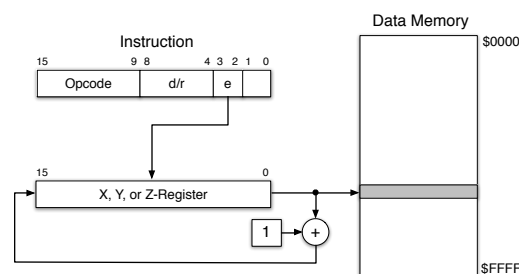
LD R16, -Z

ST -Z, R16

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23

Indirect with Post-Increment



Examples:

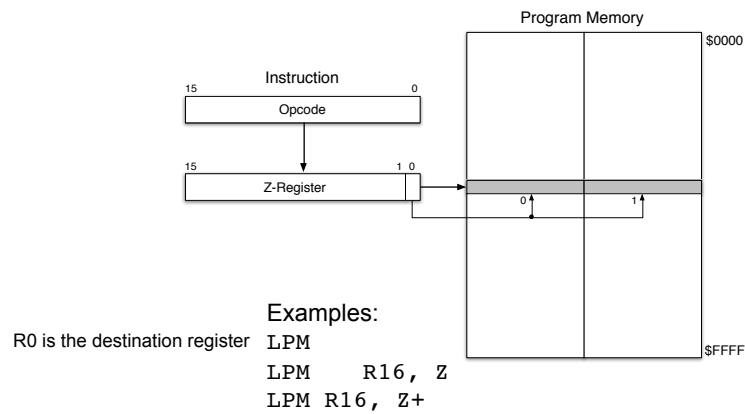
LD R16, Z+

ST Z+, R16

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Part I - Assembly Programming

24

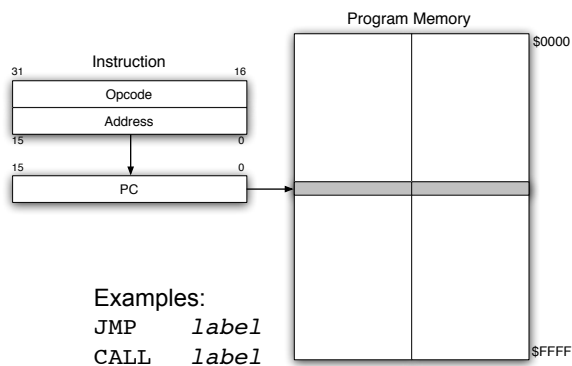
Program Memory Constant Addressing



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Part I - Assembly Programming

25

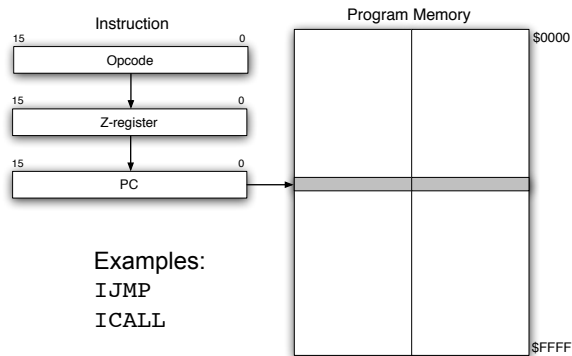
Direct Program Memory Addressing



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Part I - Assembly Programming

26

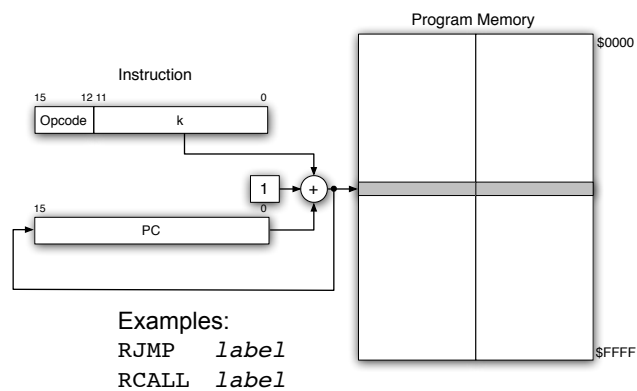
Indirect Program Memory Addressing



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Part I - Assembly Programming

27

Relative Program Memory Addressing



Called PC-relative jump

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28

4.4 Instructions

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Part I - Assembly Programming

29

AVR Instructions

- AVR has 134 different instructions
- Instruction types:
 - Data Transfer
 - Arithmetic and Logic
 - Control Transfer (branch/jump)
 - Bit and bit-test

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Part I - Assembly Programming

30

Data Transfer Instructions (1)

- MOV - transfers data between two registers (Register Addressing):
 - MOV Rd,Rr
 - d,r = 0, 1, ..., 31
- MOVW - transfers data between two pairs of registers.
 - MOVW Rd,Rr
 - d,r = 0, 2, ..., 30

- Example:

```
; AVR assembly code — Move Y to Z
MOVW R30, R28 ; Move R29:R28 (Y) to R31:R30 (Z)
```

Data Transfer Instructions (2)

- LD - loads data from memory or immediate value (Indirect Addressing):
 - LD Rd,src (Load Indirect)
 - d = 0, 1, ..., 31
 - src = X, X+, -X, Y, Y+, -Y, Z, Z+, -Z
 - LDD Rd,src (Load Indirect with Displacement)
 - d = 0, 1, ..., 31
 - src = Y+q, Z+q
 - q = 6-bit displacement ($0 \leq q \leq 63$)
 - LDI Rd, K (Load Immediate)
 - d = 16, 17, ..., 31
 - K = 8-bit constant ($0 \leq K \leq 255$)
 - Can be represented in decimal (e.g., 10), binary (e.g., 0b00001010), or Hexadecimal (e.g., 0x0A or \$0A)
 - LDS Rd, k (Load Direct from SRAM)
 - d = 0, 1, ..., 31
 - k = 16-bit address

Data Transfer Instructions (3)

- Example:

; AVR assembly code – Add constant to register

```
LDI R16, 24      ; Load 24 into R16
ADD R1, R16      ; Add it to R1
```

- Example:

; AVR assembly code – Load value from address \$0F10

```
LDI R29, $0F     ; Load upper byte of address to R29
LDI R28, $10     ; Load lower byte of address to R28
LD R16, Y        ; Load value
```

Data Transfer Instructions (4)

- ST - stores data to memory (Indirect Addressing):

- ST *dst*, Rr (Store Indirect)

- *dst* = X, X+, -X, Y, Y+, -Y, Z, Z+, -Z
- *r* = 0, 1, ..., 31

- STD *dst*, Rr (Store Indirect with Displacement)

- *dst* = Y+q, Z+q
- *r* = 0, 1, ..., 31
- *q* = 6-bit displacement ($0 \leq q \leq 63$)

- STS *k*, Rr (Store Direct from SRAM)

- *k* = 16-bit address
- *r* = 0, 1, ..., 31

- Example:

; AVR assembly code – Store value to element of structure

; Assume Y points to beginning of a structure

```
ADD R1, R2      ; Add two values
STD Y+4, R1     ; Store result to Y offset by 4 bytes
```

Data Transfer Instructions (5)

- LPM - load program memory
 - LPM Rd,src
 - d = 0, 1, ..., 31
 - src = Z, Z+
 - LPM
 - dest = R0 (implied)
 - src = Z (implied)
 - Useful for accessing constants stored in Program memory

Data Transfer Instructions (6)

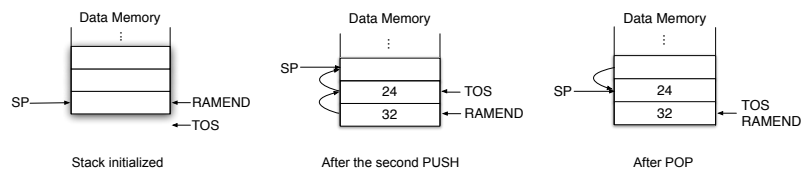
- IN/OUT – I/O instructions
 - IN Rd,A
 - d = 0, 1, ..., 31
 - A = 0, 1, ..., 63
 - OUT A, Rr
 - A = 0, 1, ..., 63
 - r = 0, 1, ..., 31
 - Will be discussed in more detail later
- PUSH/POP - stack operations
 - PUSH Rr
 - r = 0, 1, ..., 31
 - POP Rd
 - d = 0, 1, ..., 31

Data Transfer Instructions (7)

- Example:

; AVR assembly code – Push \$32 and \$24 onto the stack

```
LDI R22, $32 ; Load $32 into R22
PUSH R22      ; Push $32 on to the stack
LDI R22, $24 ; Load $24 into R22
PUSH R22      ; Push $24 to the stack
...
POP R22       ; Pop TOS (i.e., $24) to R22
```



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Part I - Assembly Programming

37

ALU Instructions (I)

Arithmetic instructions

- ADD/SUB
 - ADD Rd, Rr
 - d, r = 0, 1, ..., 31
 - Also ADC/SBC -> add/subtract with carry
- MUL - Multiply unsigned
 - MUL Rd, Rr
 - d, r = 0, 1, ..., 31
 - R1<-Result(high), R0<-Result(low)
 - Also Muls -> multiply signed
- INC/DEC - increment/decrement register
- CLR/SER - clear/set register

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Part I - Assembly Programming

38

ALU Instructions (2)

Logic instructions

- AND/OR - logical bitwise AND/OR & /w immediate
 - AND/OR Rd, Rr
 - d, r = 0, 1, ..., 31
 - ANDI/ORI Rd, K
 - d = 16, 17, ..., 31
 - K = 8-bit constant ($0 \leq K \leq 255$)
 - Can be represented in decimal (e.g., 10), binary (e.g., 0b00001010), or Hexadecimal (e.g., 0x0A or \$0A)
 - Also EOR -> Exclusive OR
- COM/NEG – one's/two's complement
 - COM Rd
 - d = 0, 1, ..., 31
- TST - test for zero or minus
 - TST Rd
 - d = 0, 1, ..., 31

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Part I - Assembly Programming

39

ALU Instructions (3)

- ADIW/SBIW – Add/subtract Immediate to/from Word
 - ADIW/SBIW Rd+I:Rd, K
 - d = 24, 26, 28, 30
 - K = 8-bit constant ($0 \leq K \leq 255$)
 - Can be represented in decimal (e.g., 10), binary (e.g., 0b00001010), or Hexadecimal (e.g., 0x0A or \$0A)
 - Useful for manipulating 16-bit pointers
 - Example


```
; AVR assembly code - Increment X by 4
          ADIW R27:R26, 4 ; Add 4 to R27:R26 (X)
```



```
; AVR assembly code - Without ADIW
          LDI R0, 4 ; Load 4
          CLR R1 ; Clear R1
          ADD R26, R0 ; Add 4 to lower byte of X
          ADC R27, R1 ; Add carry to upper byte of x
```

More instructions
are required!

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Part I - Assembly Programming

40

Branch Instructions

- **BRcond** - Branch on condition
 - **BRcond label**
 - *cond* = EQ, NE, GE, LT, CC, CS, PL, MI, VC, VS (and many more)
 - *label* = PC + 1 + *k*
 - *k* = 7-bit displacement ($-64 \leq k \leq 63$)
- **CP** - compare
 - CP Rd, Rr
 - CPI Rd, immediate
- Compare and conditional branch used together

Branch Instructions

- **Example:**
; AVR assembly code - Equivalent assembly for IF statement
CP R0, R1 ; Compare R0 with R1
BRGE NEXT ; Jump to NEXT if R0 >= R1
... ; If R0 < R1, do something
NEXT:
... ; Otherwise, continue on

Skip Instructions

- Skip if bit in register set(S)/cleared(C)

- SBRS/C Rd, bit
 - d = 16, 17, ..., 31
 - bit = 0, 1, ..., 7
- SBIS/C A, bit
 - A = 0, 1, ..., 63
 - bit = 0, 1, ..., 7

- Useful for testing flags

- Example:

; AVR assembly code - Test and loop on TOV0

LOOP:

```
SBIS $38, 0      ; Skip next inst. if TOV0 is set
RJMP LOOP        ; Jump back if not set
...              ; Do something if flag set
```

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Part I - Assembly Programming

43

Jump Instruction

- JMP instructions

- JMP label
 - label = k
 - k = 16-bit address
- RJMP label
 - label = PC + 1 + k
 - k = 7-bit displacement ($-64 \leq k \leq 63$)
- IJMP
 - label = Z

- CALL/RET - subroutine call/return

- CALL label
- RCALL label
- ICALL
- RET
- Stack implied
- Also RETI -> return from interrupt

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Part I - Assembly Programming

44

Jump Example

- Example

; AVR assembly code - Subroutine call and return

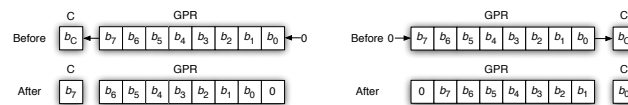
```
...
RCALL SUBR      ; First call to SUBR
...
RCALL SUBR      ; Second call to SUBR
...
SUBR:
...
...Do something... ; Subroutine
...
RET
```

Bit and Bit Test Instructions

- LSL/LSR - Logical Shift Left/Right

- LSL Rd

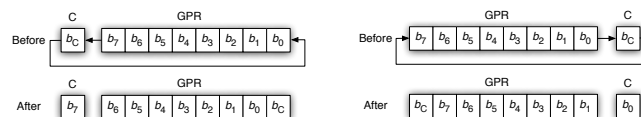
- d = 0, 1, ..., 31



- ROL/ROR - Rotate Left/Right through carry

- ROL R

- d = 0, 1, ..., 31



Bit and Bit Test Instructions

- SBI/CBI – Set/Clear Bit in I/O register
 - SBI/CBI *A*, *bit*
 - *A* = 0, 1, ..., 63
 - *bit* = 0, 1, ..., 7
- SEI/CLF - Set/Clear flag
 - *f* = C, N, Z, I, S, V, T, H
 - SEI => Turn on global interrupt

4.5 Assembly to Machine Instruction Mapping

Introduction

- Discussed assembly instructions using *mnemonics*.
 - Easier to remember names of instructions, registers, and memory locations.
- When computers were first developed, they were programmed using 0's and 1's via mechanical switches, i.e., *machine instructions*!
- Will discuss assembly to machine instruction mapping.
- Knowing how various information of instructions are encoded is crucial for understanding how to design and develop processor hardware.

ALU Instructions

- INC Rd
 - INC R1 ; R1 ← R1 + 1
- ADD Rd, Rr
 - ADD R15, R16 ; R15 ← R15 + R16

1001	010d	dddd	0011
------	------	------	------

d dddd = 0 0001

0000	11rd	dddd	rrrr
------	------	------	------

d dddd = 0 1111

r rrrr = 1 0000

Load Instructions (1)

- LD Rd,Y

- LD R16, Y ; R16 ← M(Y)
- Y is implied in the opcode

1001	000d	dddd	1000
------	------	------	------

d dddd = 1 0000

- LDI Rd,K

- LDI R30, 0xF0 ; R30 ← 0xF0
- Destination register can only be R16-R31
- 8-bit constant K ($0 \leq K \leq 255$)

1110	KKKK	dddd	KKKK
------	------	------	------

1 dddd = 1 1110

KKKK KKKK = 1111 0000

Ch. 4: Atmel's AVR 8-bit Microcontroller,
Part I - Assembly Programming

51

Load Instructions (2)

- LDD Rd,Y+q

- LDD R4, Y+2 ; R4 ← M(Y+2)
- Y is implied in the opcode
- 6-bit displacement q ($0 \leq q \leq 63$)

10q0	qq0d	dddd	1qqq
------	------	------	------

d dddd = 0 0100

q qq qq = 0 00 010

Ch. 4: Atmel's AVR 8-bit Microcontroller,
Part I - Assembly Programming

52

I/O Instructions

- IN Rd,A
 - IN R25, \$16 ; R25 ← I/O(\$16)
 - \$16 is an I/O register connected to Port B (PIN7-PIN0)
 - 6 bit A ($0 \leq A \leq 63$) ⇒ 64 I/O registers.

1011	0AA	d	ddd	AAAA
------	-----	---	-----	------

d dddd = 1 1001

AA AAAA = 01 0110

ALU Examples

- MUL Rd, Rr
 - MUL R15, R16 ; R1:R0 ← R15 × R16
 - Both operand unsigned (signed version ⇒ Muls)
 - Product high and low stored in R1 and R0, respectively.

1001	11	r	ddd	rrrr
------	----	---	-----	------

rrrr = 10000

ddd = 01111

Branch Instructions

- **BRcc label**
 - if (cc) then $PC \leftarrow PC + k + I$ (PC-relative)
 - Example:

Address	Code
0232	CP R0, R1 ; compare
0233	BREQ SKIP
0234	... ; Next inst.
...	...
0259	SKIP:...

$k = \$0259 - \$0234 = \$0025$

BREQ SKIP =>

1111	00kk	kkkk	k001
------	------	------	------

Address range => $kk\ kkkk\ k = 01\ 0010\ 1$
 $-64 \leq k \leq +63$

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Part I - Assembly Programming

55

Jump Instructions

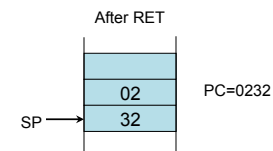
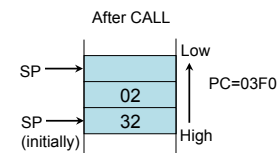
- **CALL label**
 - $PC \leftarrow k$

Address	Code
0230	CALL SUBR
0232	next inst.
...	...
03F0	SUBR:my subroutine... ... RET

- CALL is 32-bit instruction

1001	0100	0000	1110
kkkk	kkkk	kkkk	kkkk

$kkkk\ kkkk\ kkkk\ kkkk = 0000\ 0011\ 1111\ 0000$



Ch. 4: Atmel's AVR 8-bit Microcontroller;
Part I - Assembly Programming

56

4.6 Assembler Directives

AVR Assembly Directives

- Called pseudo opcodes
 - **ORG**: Tells the assembler where to put the instructions that follow it.
`.ORG 0x37`
 - **EXIT**: Tells the assembler to stop assembling the file
 - **EQU**: Assigns a value to a label.
Syntax: `.EQU label = expression`
`.EQU io_offset = 0x23`
 - **BYTE**: Reserves memory in data memory
Syntax: `label: .BYTE expression`
`var: .BYTE 1`
 - **DB**: Allows arbitrary bytes to be placed in the code.
Syntax: `label: .DB expressionlist`
`consts: .DB 0, 255, 0b01010101, -128, 0xaa`
`Text: .DB "This is a text."`
 - **DW**: Allows 16-bit words to be placed into the code
Syntax: `label: .DW expressionlist`
`varlist: .DW 0, 0xffff, 0b1001110001010101, -32768, 65535`
 - **INCLUDE**: Tells the assembler to read from the specified file.
Syntax: `.INCLUDE filename`
`.INCLUDE "m128def.inc"`

4.7 Expressions

AVR Assembly Expressions (I)

- Expression can consist of operands, operators, and functions:
- Operands can be
 - labels
 - Integer constants
 - Constants defined using .EQU
- Support all C/C++ type operators
- Provides predefined functions

AVR Assembly Expressions (2)

- Example:

```
; AVR assembly code - Example use of operators
.EQU RXEN1 = 4
.EQU TXEN1 = 3
.DEF mpr = R16
...
    LDI    mpr, (1<<RXEN1|1<<TXEN1)
```

After preprocessing this becomes
`LDI R16, 0b00011000`

- Example:

```
; AVR assembly code - Example use of functions
.DSEG
Array:
    .BYTE array_size
.CSEG
    LDI    R27, HIGH(Array)    ; Load high byte address to R27
    LDI    R26, LOW(Array)     ; Load low byte address to R26
    LD     R7, X
```

Ch. 4: Atmel's AVR 8-bit Microcontroller,
Part I - Assembly Programming

61

4.10 Anatomy of an Assembler Program

Ch. 4: Atmel's AVR 8-bit Microcontroller,
Part I - Assembly Programming

62

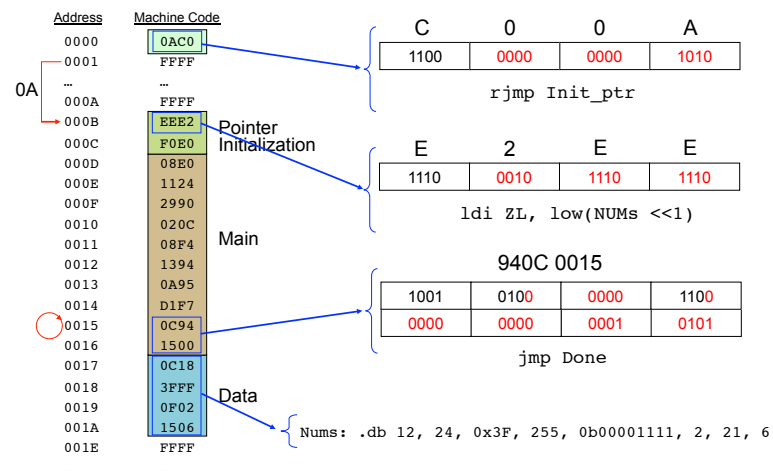
Addition of 8 Numbers

```
.include "m128def.inc"
.ORG $0000
Rjmp Init_ptr
.ORG $000B
Init_ptr:
    LDI ZL, low(Nums<<1) ;
    LDI ZH, high(Nums<<1) ; Z points to 12
Main: LDI R16, 8 ; Load loop count
    CLR R1 ; Clear accumulator R1:R0
    CLR R0 ;
Loop: LPM R2,Z+ ; Load data to R2 and post inc. pointer
    ADD R0, R2 ; Add R2 to R0(L)
    BRCC Skip ; No carry, skip next step
    INC R1 ; Add carry R1(H)
Skip: DEC R16 ; Count down the # words to add
    BRNE Loop ; If not done loop
Done: JMP Done ; Done. Loop forever.
Nums: .DB 12, 24, 0x3F, 255, 0b00001111, 2, 21, 6
```

Ch. 4: Atmel's AVR 8-bit Microcontroller;
Part I - Assembly Programming

63

Code in Program Memory



Ch. 4: Atmel's AVR 8-bit Microcontroller;
Part I - Assembly Programming

64

Main Loop

```
; Assume Z points to the first word
Main: LDI R16, 8      ; Load loop count
      CLR R1          ; Clear accumulator R1:R0
      CLR R0
Loop: LPM R2,Z+       ; Load data to R2 and post-inc ptr
      { ADD R0,R2      ; Add R2 to R0(L)
        BRCC Skip     ; No carry, skip next step
        INC R1        ; Add carry R1(H)
      }
Skip: DEC R16         ; Decrement loop count
      BRNE Loop       ; If not done loop
Done: JMP Done        ; Done. Loop forever.
```

Can be replaced by

```
{ CLR R3              ; Clear R3
  ...
  ADD R0,R2           ; Add R2 to R0(L)
  ADC R1,R3           ; Add carry
```

Ch. 4: Atmel's AVR 8-bit Microcontroller,
Part I - Assembly Programming

65

Pointer Initialization

- Where are the 8 numbers & number of words stored and how do we point to it?
- Depends on where data is stored: program memory or data memory.

Stored in Program memory as constants:

```
.ORG $000B
      LDI ZL, low(Nums<<1) ;
      LDI ZH, high(Nums<<1) ;Z points to 12
      ...
Nums: .DB 12, 24, 0x3F, 255, 0b00001111, 2, 21, 6
```

low() and **high()** are macros that extracts low and high byte
(defined in "m128def.inc")

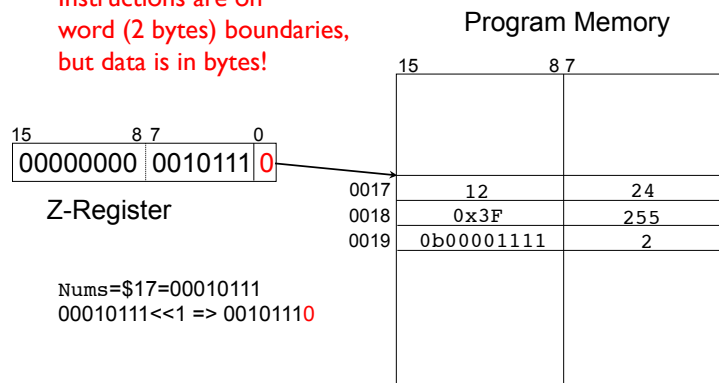
Ch. 4: Atmel's AVR 8-bit Microcontroller,
Part I - Assembly Programming

66

Pointer Initialization

- “<<” means shift left (multiply by 2)

Instructions are on
word (2 bytes) boundaries,
but data is in bytes!



Nums=\$17=00010111
00010111<<1 => 00101110

We could have also used `high(2*NUMS)` and `low(2*NUMS)`

Ch. 4: Atmel's AVR 8-bit Microcontroller,
Part I - Assembly Programming

67

Data Memory

- What if data is not predefined (i.e., constants)? Then, we need to allocate space in data memory using `.BYTE`.

Data memory:

```

Nums:
    .BYTE 8                ; Sets storage in data memory
Count:
    .BYTE 1                ; Data generated on the fly or read in

    ldi    YL,low(Count)    ;
    ldi    YH,high(Count)   ;
    ld     R16,Y            ; R16 =8
    ldi    YL,low(Nums)    ;
    ldi    YH,high(Nums)   ; Y points to first word
    ...
    ...
Loop:
    ld     R2,Y+            ; Load data & post inc. pointer
    ...
    
```

Ch. 4: Atmel's AVR 8-bit Microcontroller,
Part I - Assembly Programming

68

Result

- Registers R1 (H) and R0 (L) hold the result.

```
12
24
63 (3F)
255
15 (0b00001111)
2
21
+ 6
---
398 => 018E
```

R1=01 & R0=8E

Testing for Overflow

- Suppose we want to detect overflow and call a subroutine (e.g., to print error message)

```
...
Loop:
    lpm  R2,Z+      ; Load data to R2 & post inc. pointer
    add  R0, R2     ; Add R2 to R0(L)
    brcc Skip      ; No carry, skip next step
    inc  R1         ; Add carry R1(H)
    brvc Skip      ; If V=0 branch to skip
    rcall ERROR     ; We could also use CALL
Skip: ...
...
ERROR:
    ...            ; My subroutine would go here
    RET
```

Questions?



Ch. 4: Atmel's AVR 8-bit Microcontroller,
Part 1 - Assembly Programming

71