



Chapter 7: Digital Components

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Chapter Goals

- Review basic digital design concepts:
 - Designing basic digital components using logic gates and memory elements:
 - Decoders/encoders, multiplexers, counters, registers, memories, and Arithmetic and Logic Units (ALUs).
- Understand that these digital components represent fundamental building blocks for any digital system, especially processor (microarchitecture) design:
 - Modular design.

Contents

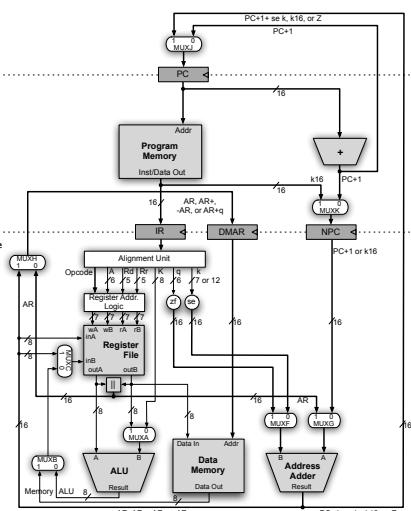
- 7.1 Introduction
- 7.2 Multiplexers
- 7.3 Decoders
- 7.4 Memory Elements
- 7.5 Registers
- 7.6 Register File

7.1 Introduction

Basic Digital Components

- Multiplexors
- Decoders/encoders
- Registers
- Memories
- ...later we will see Arithmetic and Logic Units (ALUs)

AVR Microarchitecture



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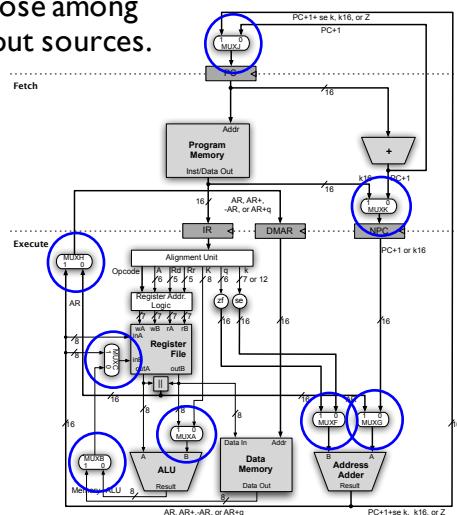
7.2 Multiplexer

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Multiplexors

Use to choose among multiple input sources.

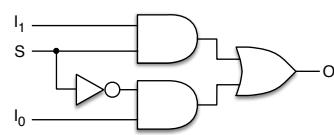
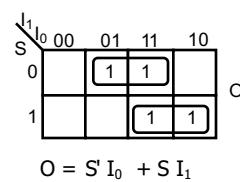
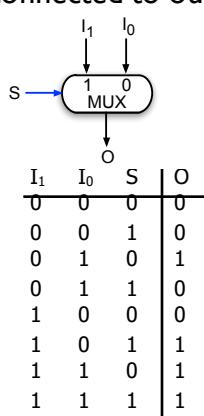


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Multiplexors

- 2^n data inputs, n control inputs, one output.
- Control signal pattern forms binary index of input connected to output.

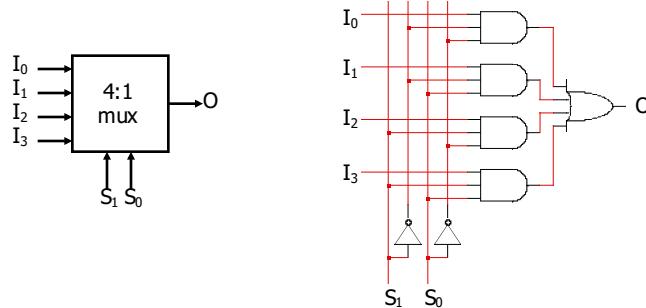


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Multiplexors (cont.)

- 2:1 MUX: $O = S' I_0 + S I_1$
- 4:1 MUX: $O = S_1' S_0' I_0 + S_1' S_0 I_1 + S_1 S_0' I_2 + S_1 S_0 I_3$
- 8:1 MUX: $O = S_2' S_1' S_0' I_0 + S_2' S_1' S_0 I_1 + S_2' S_1 S_0' I_2 + S_2' S_1 S_0 I_3 + S_2 S_1' S_0' I_4 + S_2 S_1' S_0 I_5 + S_2 S_1 S_0' I_6 + S_2 S_1 S_0 I_7$

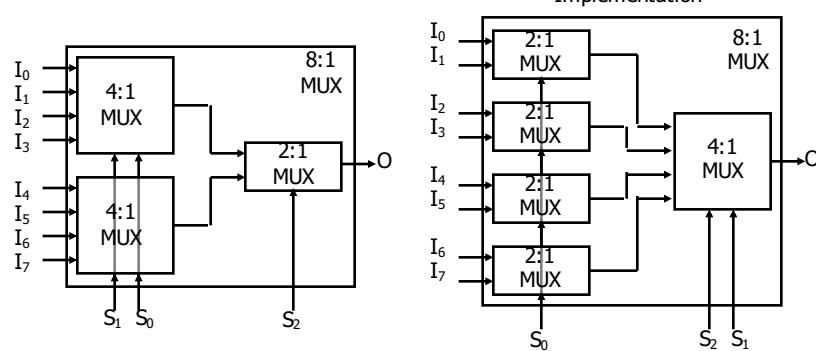


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Cascading Multiplexors

- Large multiplexers implemented by cascading smaller ones.



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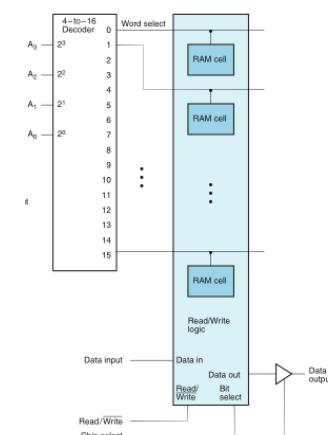
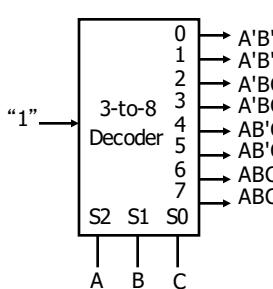
7.3 Decoder

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Decoders

- Single data input, k control inputs, 2^k outputs.
- Used to select one of 2^k components:
 - RAM cells in memory
 - Registers in register file



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2-to-4 Decoder

- Implementing a 2-to-4 decoder

Truth Table

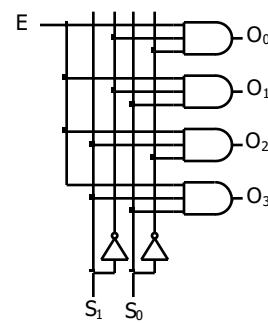
E	S ₁	S ₀	O ₃	O ₂	O ₁	O ₀
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

$$O_0 = E \cdot S_1' \cdot S_0'$$

$$O_1 = E \cdot S_1' \cdot S_0$$

$$O_2 = E \cdot S_1 \cdot S_0'$$

$$O_3 = E \cdot S_1 \cdot S_0$$

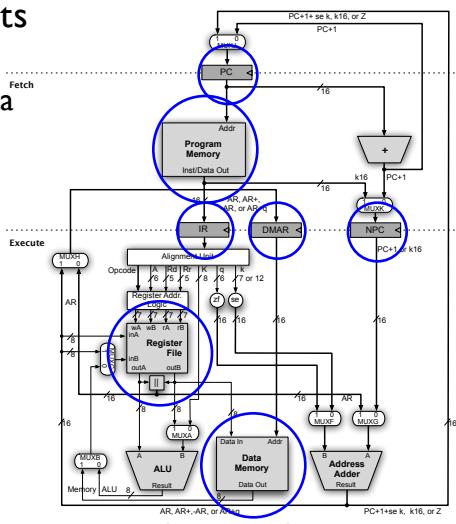


We can also implement active low enable

7.4 Memory Elements

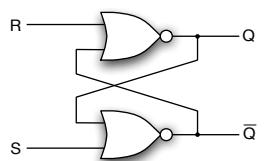
Memory Elements

- Bi-stable elements used in
 - Program and Data memories
 - Registers
 - Register File

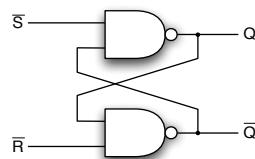


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Memory Element: S-R Latch



S	R	Q
0	0	hold
0	1	0
1	0	1
1	1	not allowed

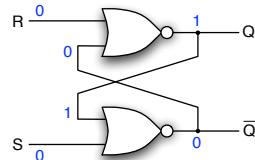


\overline{S}	\overline{R}	Q
0	0	not allowed
0	1	1
1	0	0
1	1	hold

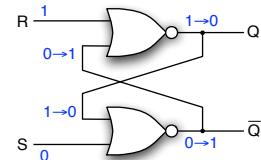
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S-R Latch Operation

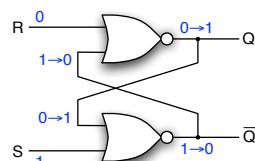
$S=0, R=0$ (hold), initially $Q=1$



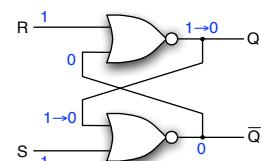
$S=0, R=1$ (reset), initially $Q=1$



$S=1, R=0$ (set), initially $Q=0$



$S=1, R=1$ (not allowed), initially $Q=1$

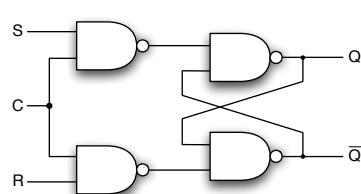


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S-R Latch with Enable

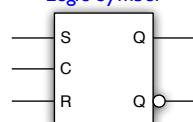
Circuit



Function Table

C	S	R	Q
0	X	X	No Change
1	0	0	No Change
1	0	1	0
1	1	0	1
1	1	1	Not allowed

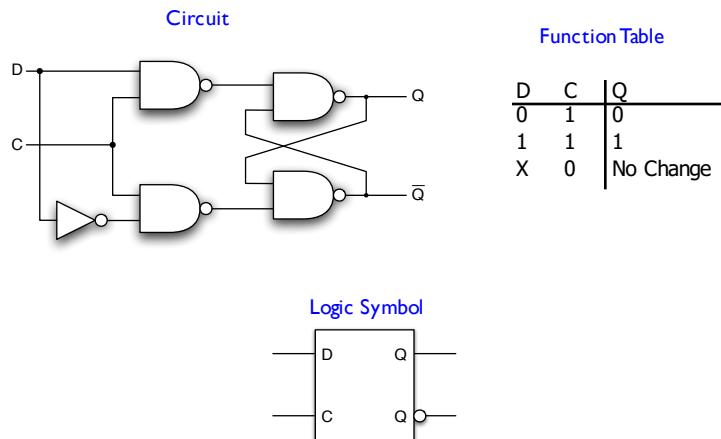
Logic Symbol



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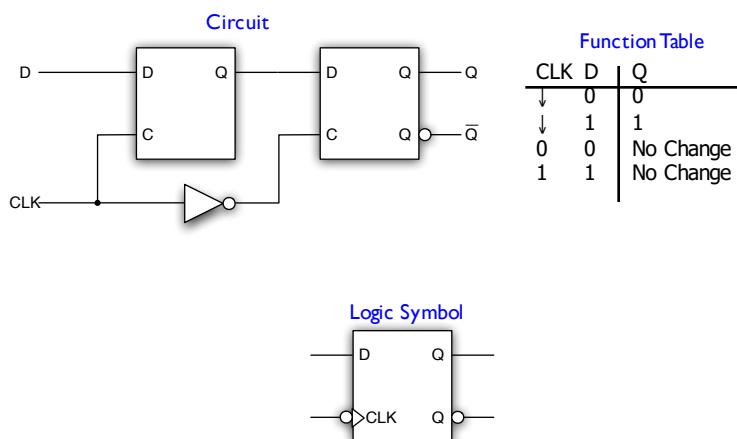
D Latch



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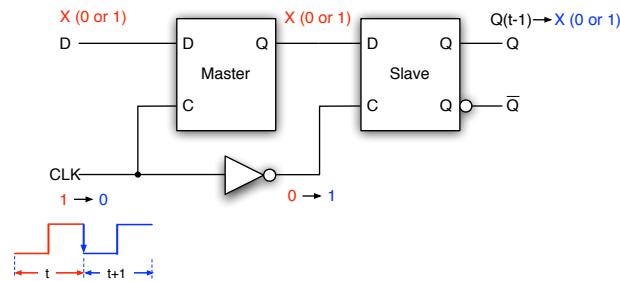
Negative Edge-Triggered D-FF



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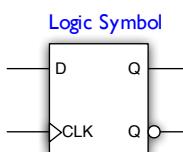
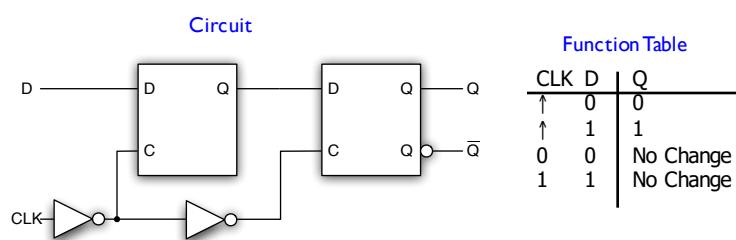
Negative Edge-Triggered D-FF Operation



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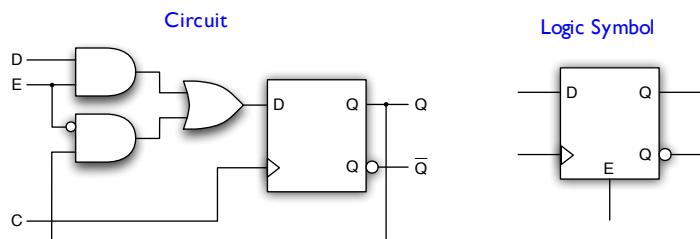
Positive Edge-Triggered D-FF



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Edge-Triggered D-FF /w Enable



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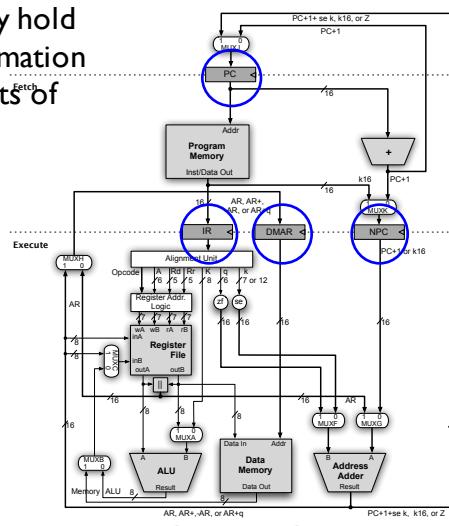
7.4 Registers

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Registers

- Used to temporary hold and separate information among various parts of the datapath.

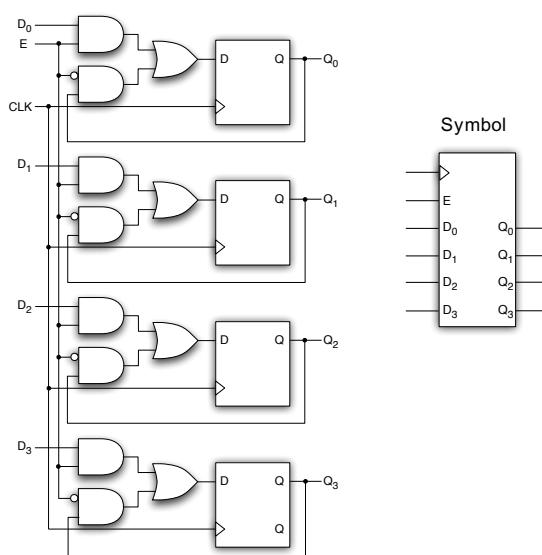


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***n*-bit Register /w Load Enable**

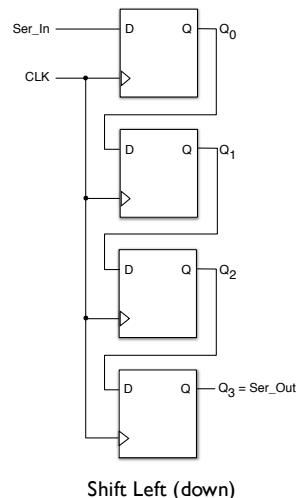
A set of
commonly
clocked
D flip-flops



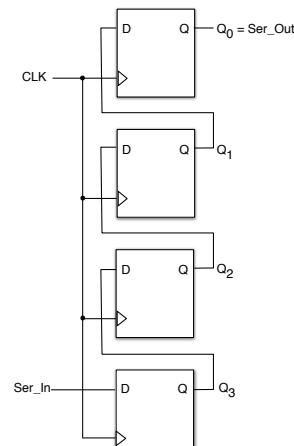
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Shift Registers



Shift Left (down)

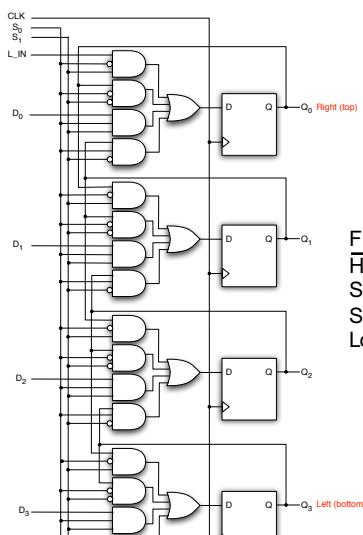


Shift Right (up)

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Bi-Directional Shift Register /w Parallel Load



Function	Control Input		Next State				
	S ₁	S ₀	Q ₃	Q ₂	Q ₁	Q ₀	
Hold	0	0	Q ₃	Q ₂	Q ₁	Q ₀	
Shift right	0	1	R_IN	Q ₃	Q ₂	Q ₁	
Shift left	1	0	Q ₂	Q ₁	Q ₀	L_IN	
Load	1	1	D ₃	D ₂	D ₁	D ₀	

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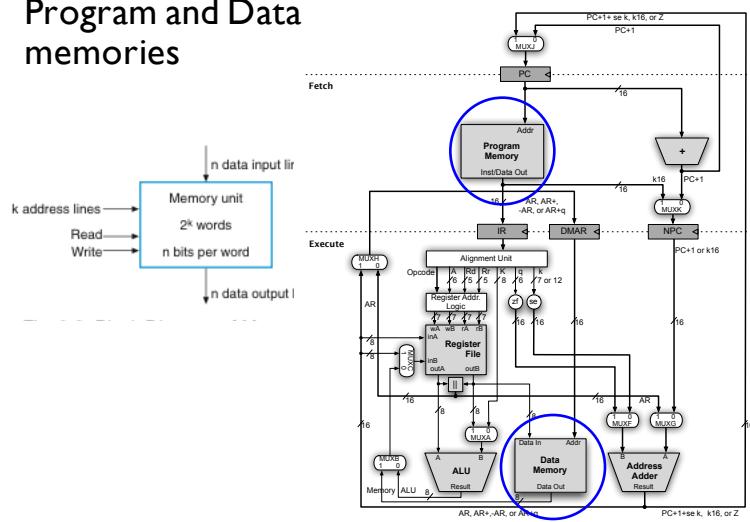
7.5 Memory

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Memory

Program and Data memories

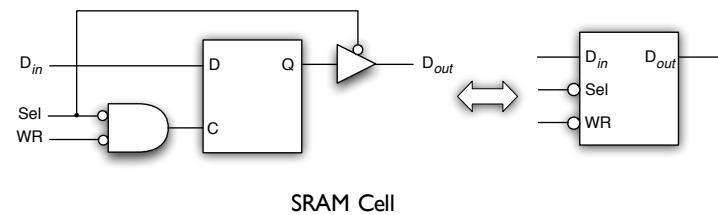


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Memory Cell

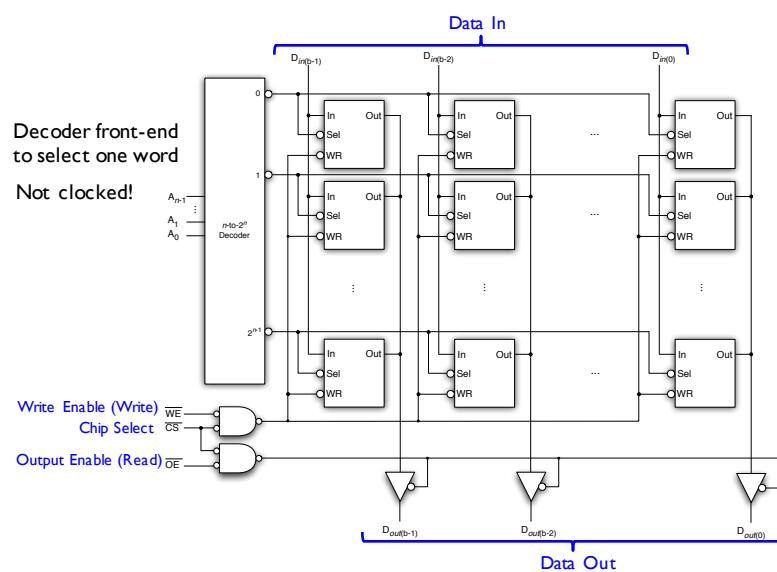
- Static RAM (SRAM)
 - Fast
 - Practically a D-FF.
 - Used in Registers and Instruction and Data Caches.
- Dynamic RAM (DRAM)
 - Need to be refreshed periodically.
 - Used in Main Memory



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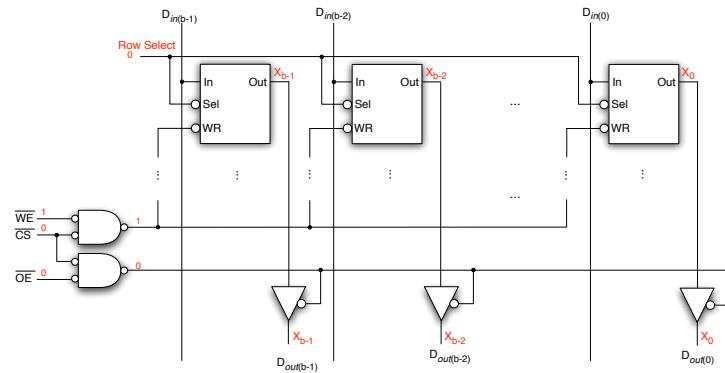
SRAM Structure



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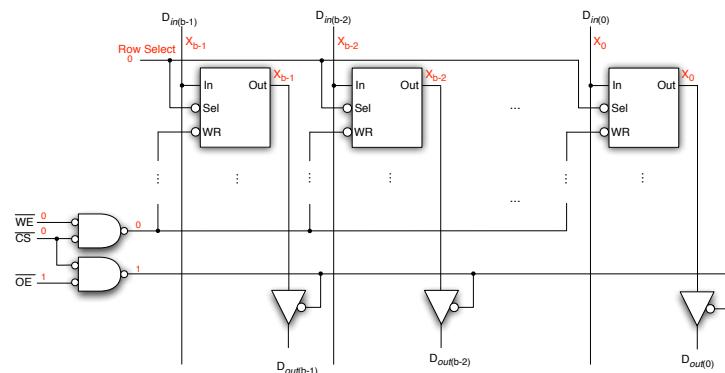
SRAM Operation: Read



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SRAM Operation: Write

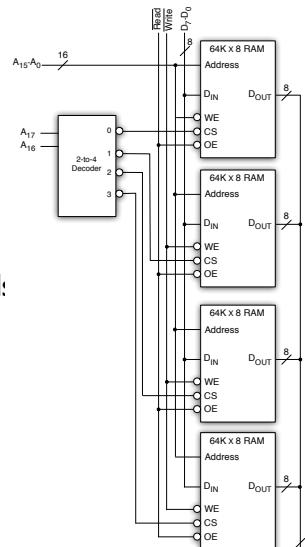


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Building Larger Memory

256K x 8 RAM
Using four 64K x 8 RAMs

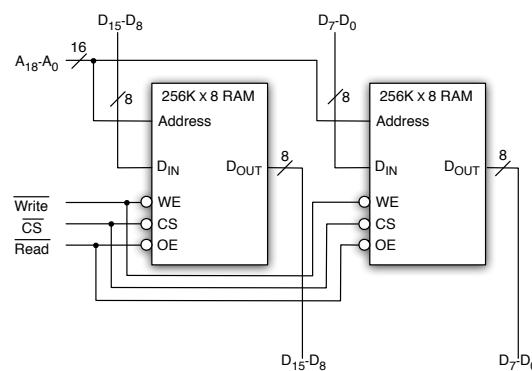


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Building Wider Memory

256K x 16 RAM
Using two 256K x 8 RAMs



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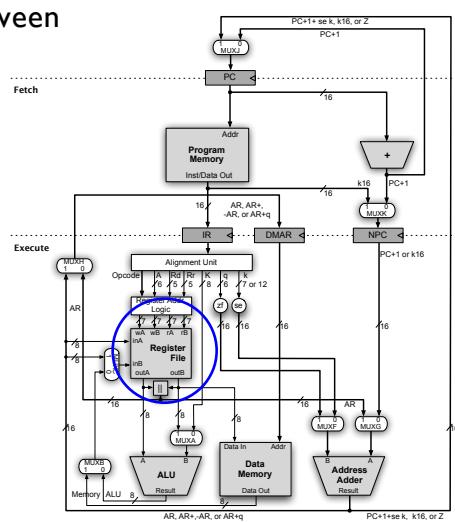
7.6 Register File

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Register File

Storage buffer between
ALU and Memory

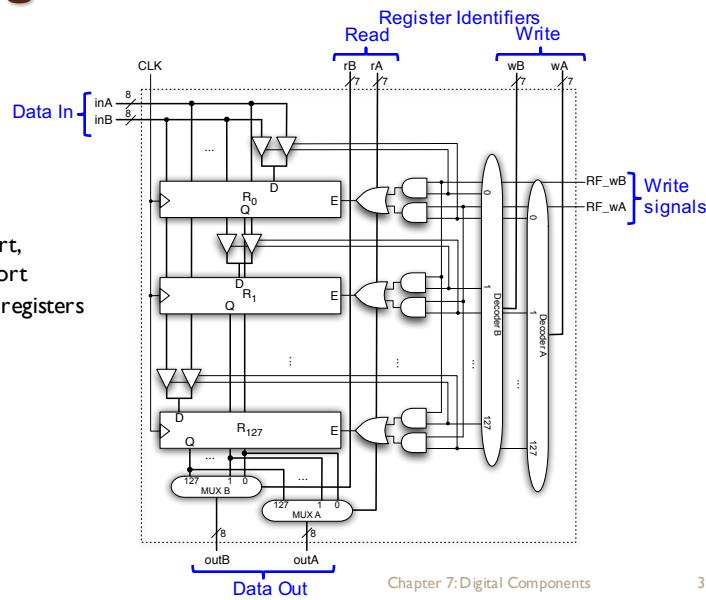


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Register File

2 Read-port,
2 Write-port
X, Y, & Z-registers



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Questions?



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