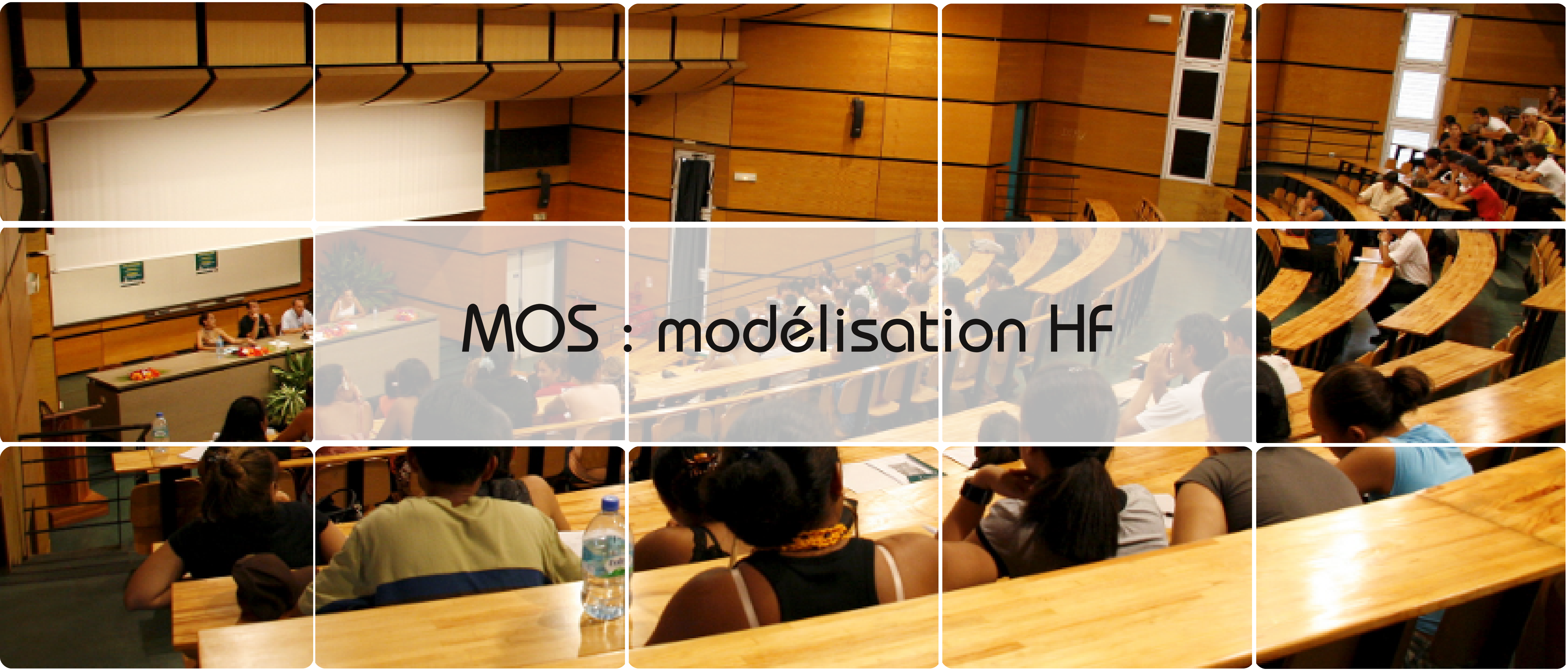
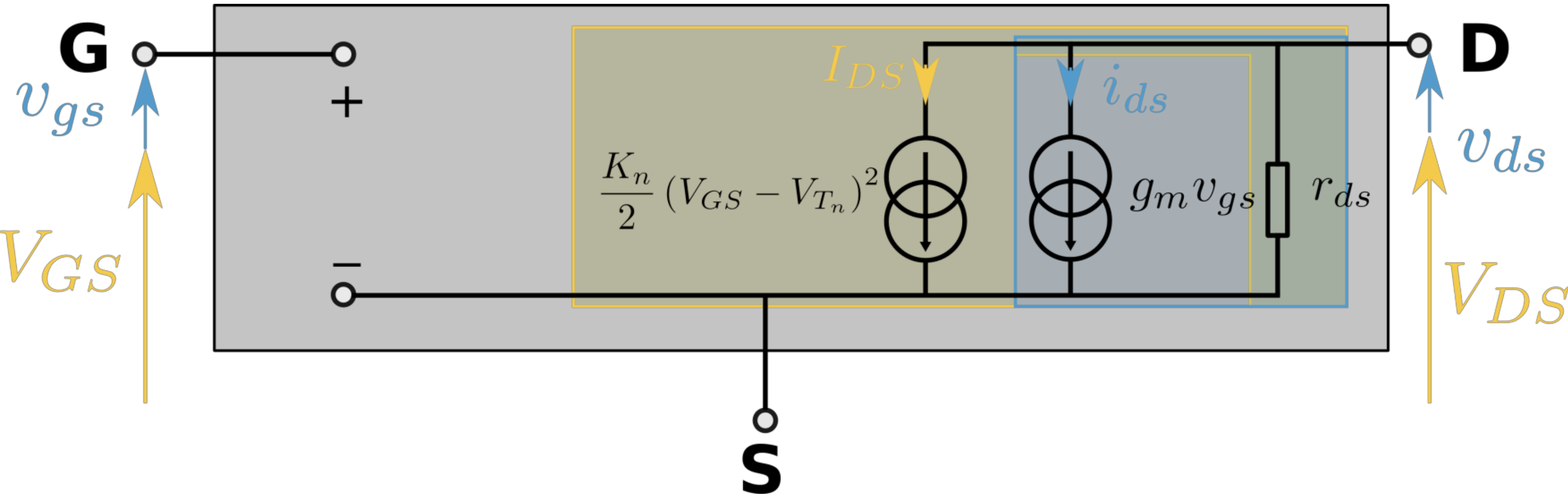
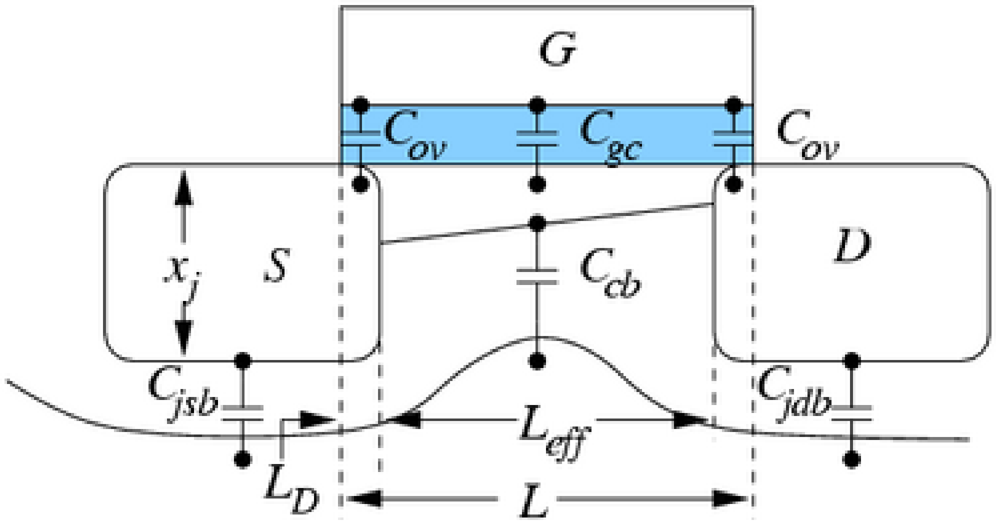


MOS : modélisation HF

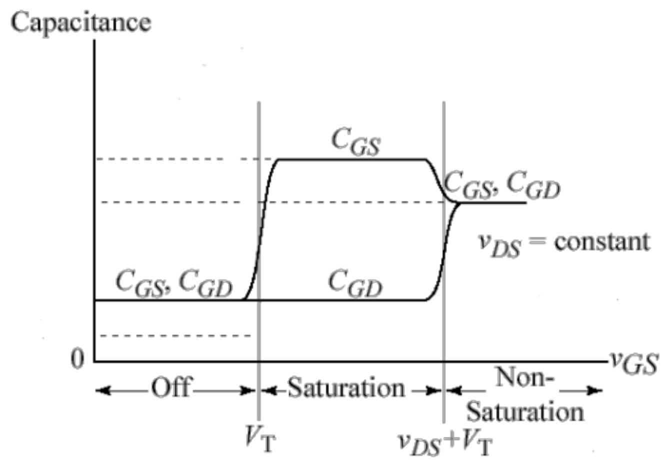
MOS : modélisation BF



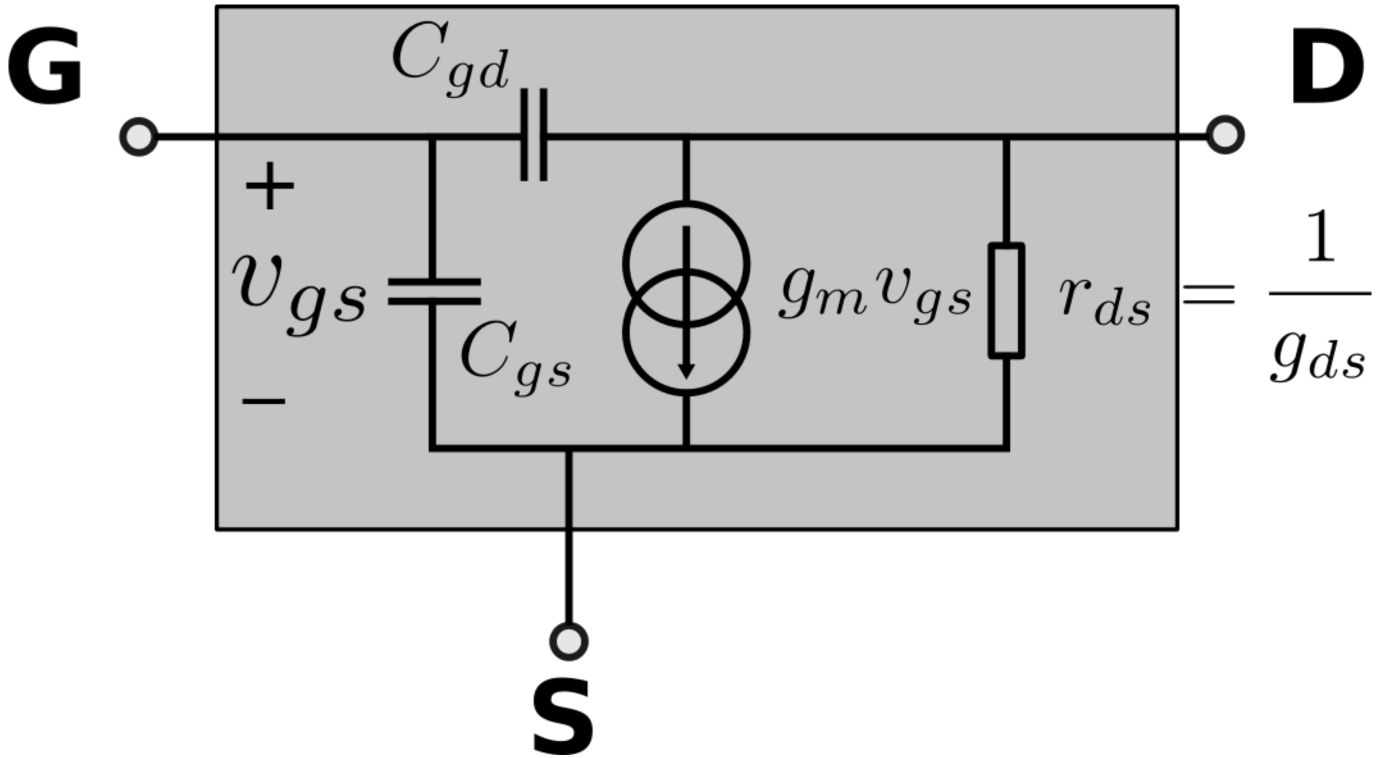
IRL



Et pour faire simple...

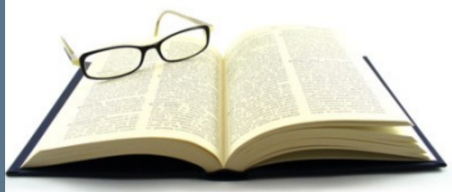


Modèle petit signal HF



Fréquence de transition

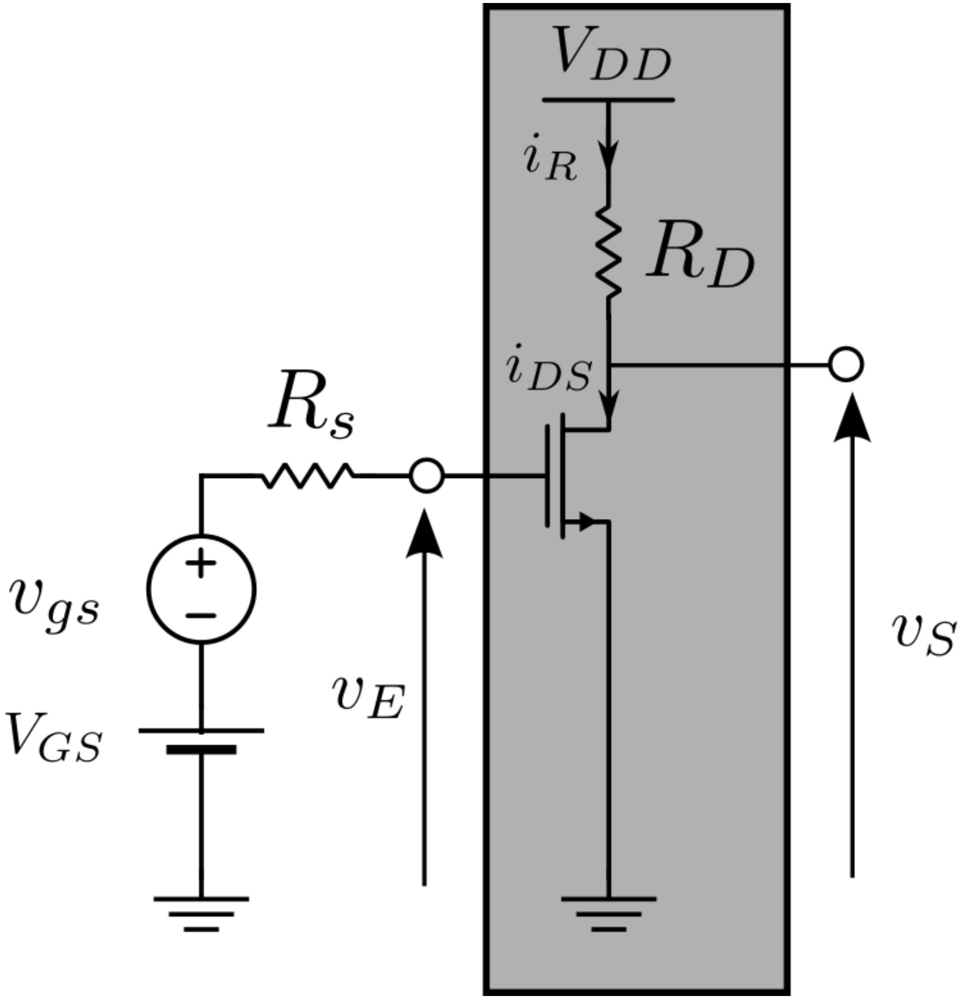
$$
\begin{aligned}
i_{in} &= v_{gs} \cdot j\omega \left(C_{gs} + C_{gd}\right) \\
i_{cc} &= v_{gs} \left(g_m - j\omega C_{gd}\right) \\
A_i &= \frac{i_{cc}}{i_{in}} = \frac{g_m - j\omega \cdot C_{gd}}{j\omega \left(C_{gs} + C_{gd}\right)}
\end{aligned}
$$



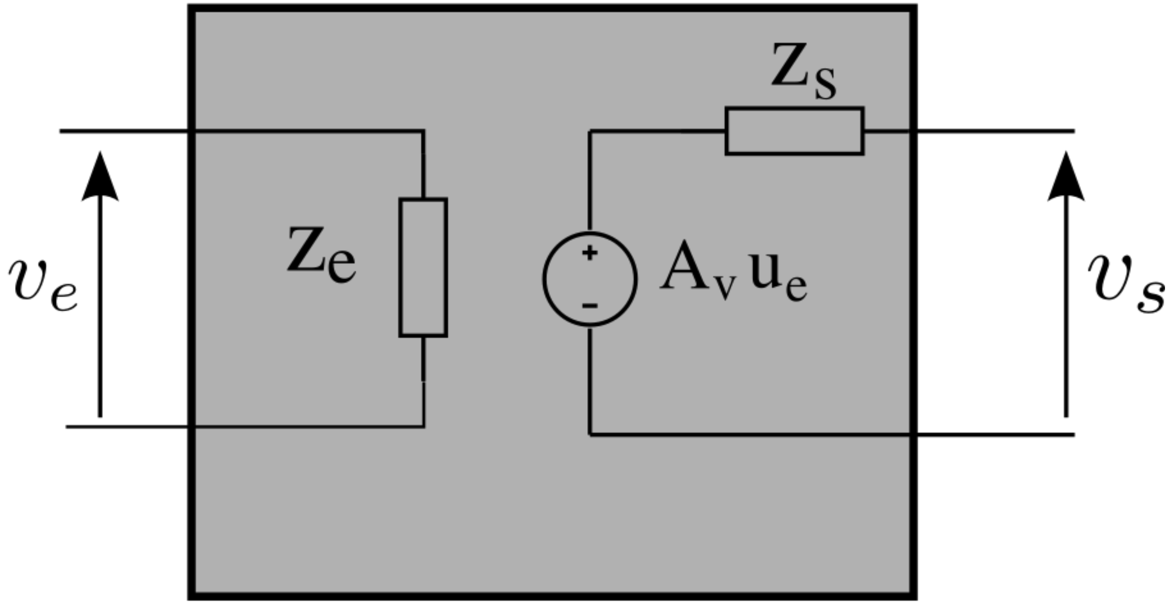
$$
\begin{aligned}
|A_i| &= \frac{\sqrt{g_m^2 + \omega^2 C_{gd}^2}}{\omega \left(C_{gs} + C_{gd}\right)} = 1 \\
f_T &= \frac{g_m}{2\pi \left(C_{gs} + C_{gd}\right)}
\end{aligned}
$$

$$
\frac{1}{2\pi f_T} \approx \frac{C_{gs}}{gm} = \frac{(2/3) W L C_{ox}}{K_n \underbrace{\left(V_{IQ} - V_T\right)}_{=V_{DSAT}}} = \frac{(2/3) L}{\underbrace{\mu_n \underbrace{V_{DSAT}/L}_{\overrightarrow{E_{DS}}}}_{Vitesse\ \acute{e}lectron}} \approx \tau_{transit}
$$

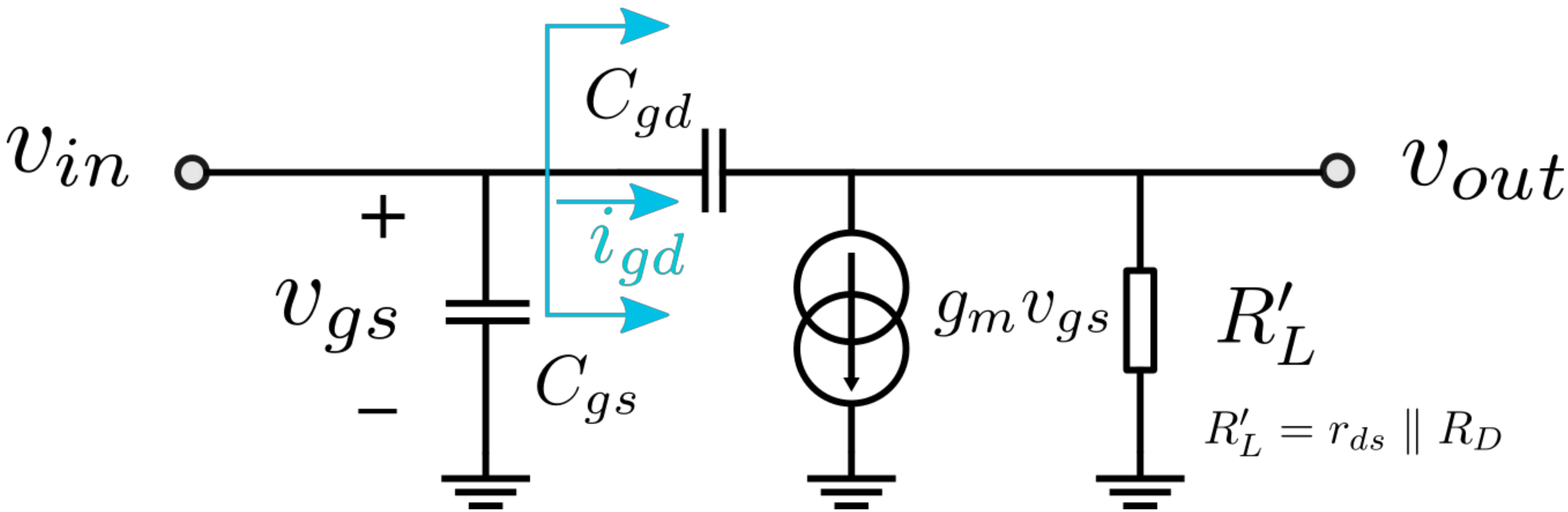
Montage SC : le remake



Autour d'un point polarisation



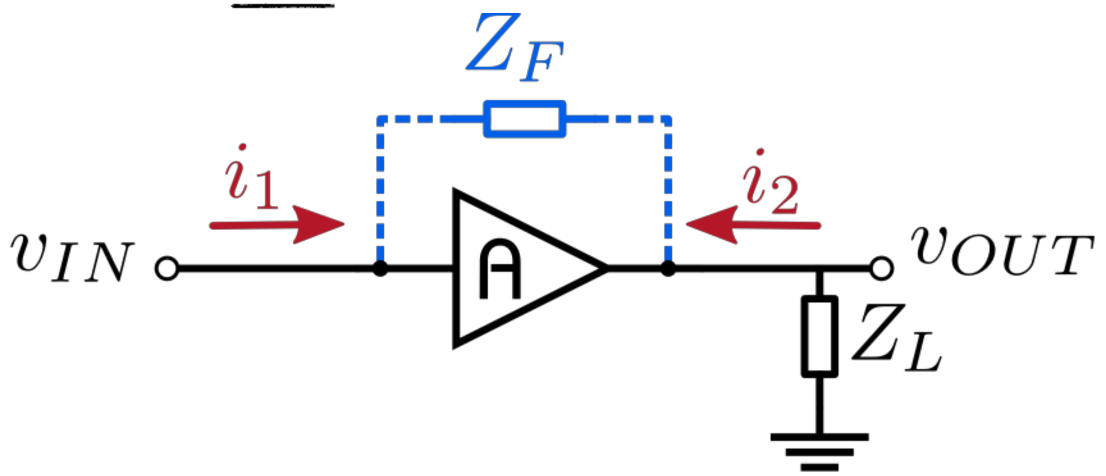
Montage SC : modèle petit signal



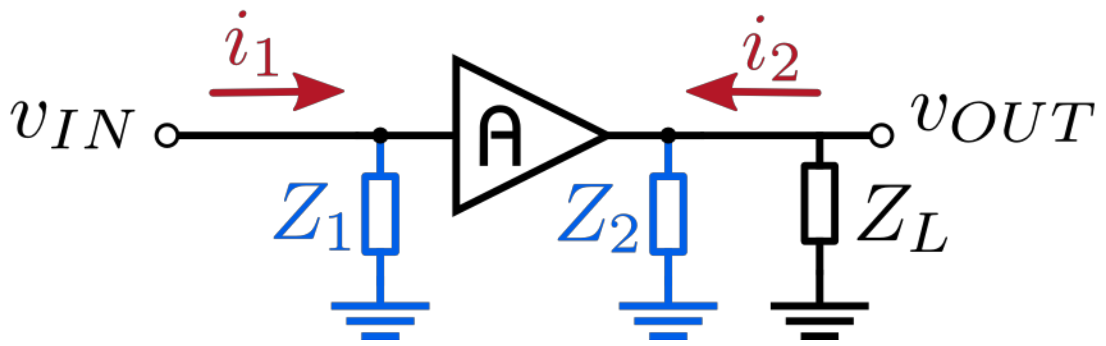
DEPENDENCE OF THE INPUT IMPEDANCE OF A THREE-ELECTRODE VACUUM TUBE UPON THE LOAD IN THE PLATE CIRCUIT

By John M. Miller

$$i_1 = \frac{v_{IN}(1-A)}{Z_F}$$



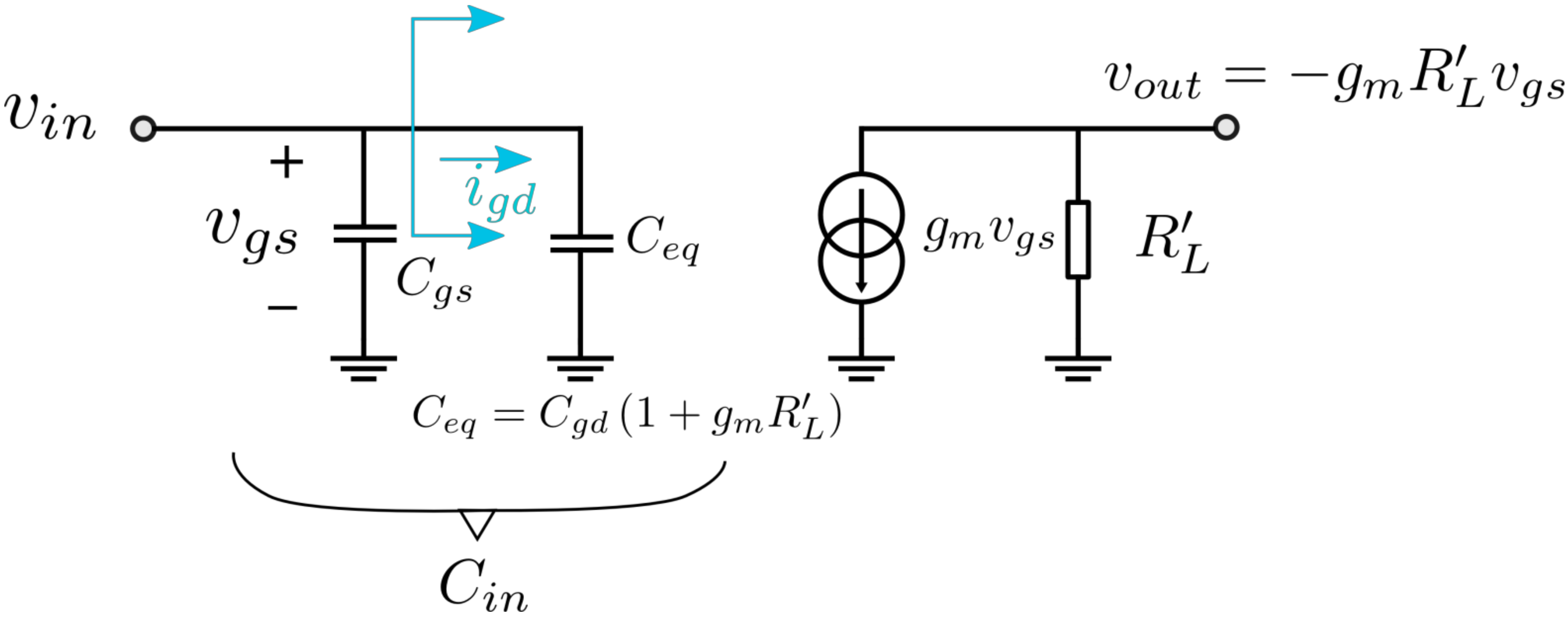
$$i_1 = \frac{v_{IN}}{Z_1}$$



$$Z_1 = \frac{1}{1-A} \cdot Z_F \approx -\frac{Z_F}{A}$$

$$Z_2 = \frac{A}{A-1} \cdot Z_F \approx Z_F$$

Montage SC : modèle petit signal HF



Montage SC : fréquence de coupure

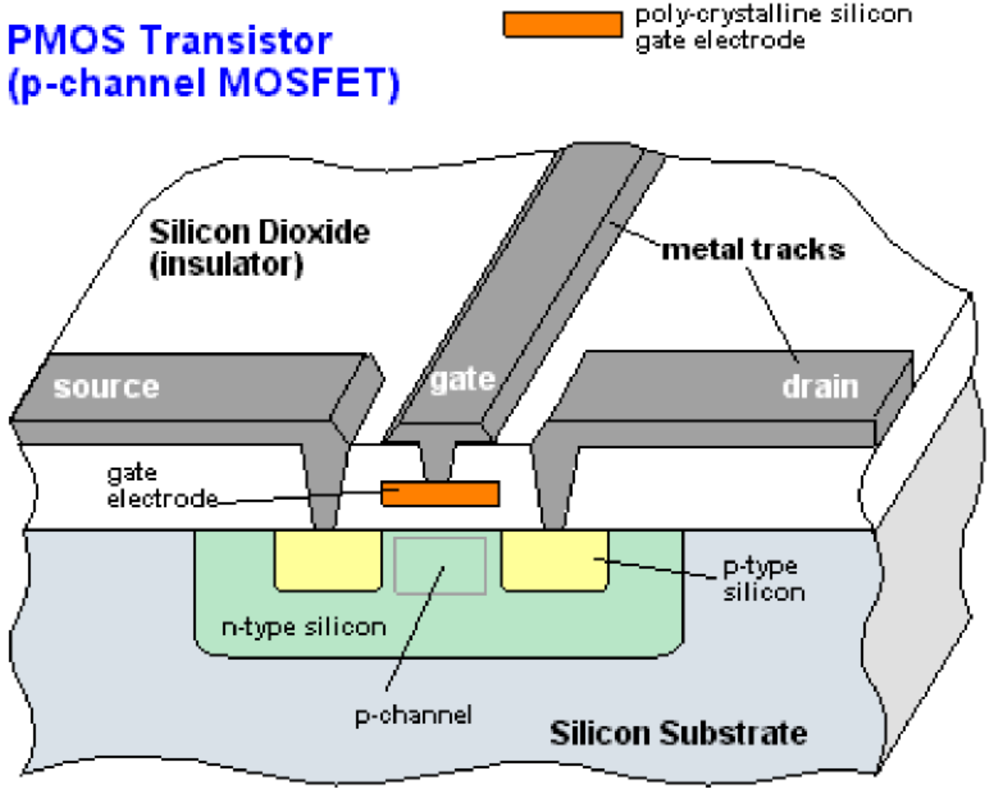
Tout se passe comme si on avait ajouté, à l'entrée du montage idéal, un filtre RC.

$$\frac{v_{out}}{v_{in}} = -g_m R'_L \cdot \frac{Z_e}{R_s + Z_e} = -\frac{g_m R'_L}{1 + j\omega R_s \left(C_{GS} + C_{eq}\right)}$$

Fréquence de coupure :

$$f_c = \frac{1}{2\pi R_s \left(C_{gs} + C_{eq}\right)} = \frac{1}{2\pi \left(C_{gs} + C_{gd}\left(1 + g_m R'_L\right)\right)}$$


Le transistor PMOS



Pour le PMOS : un courant de trous.

Le comportement du PMOS est l'opposé de celui du NMOS.

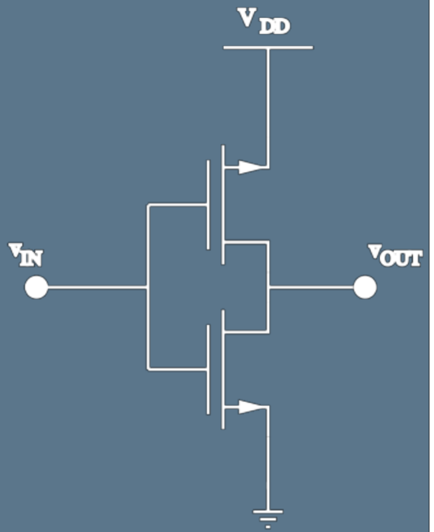
On utilise donc les formules du NMOS :

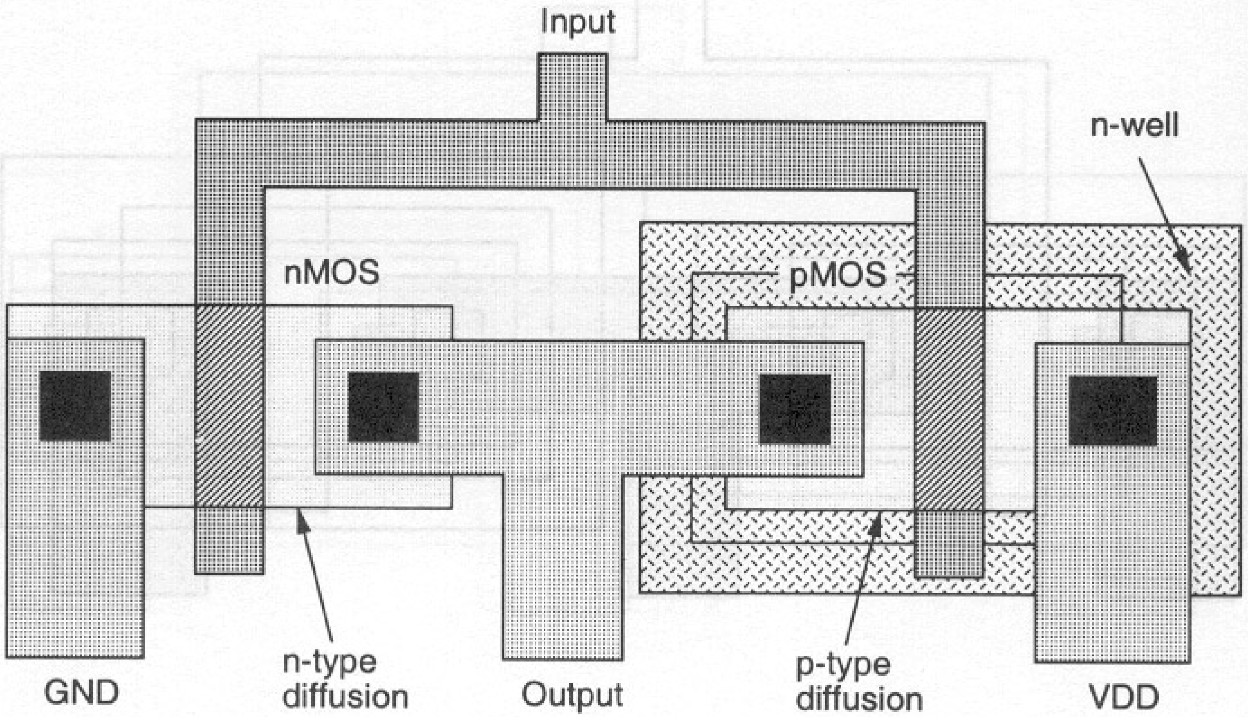
1) sachant que les tensions sont toutes négatives et que les inégalités sont inversées

OU

2) en inversant S et D ET S et G


Inverseur CMOS





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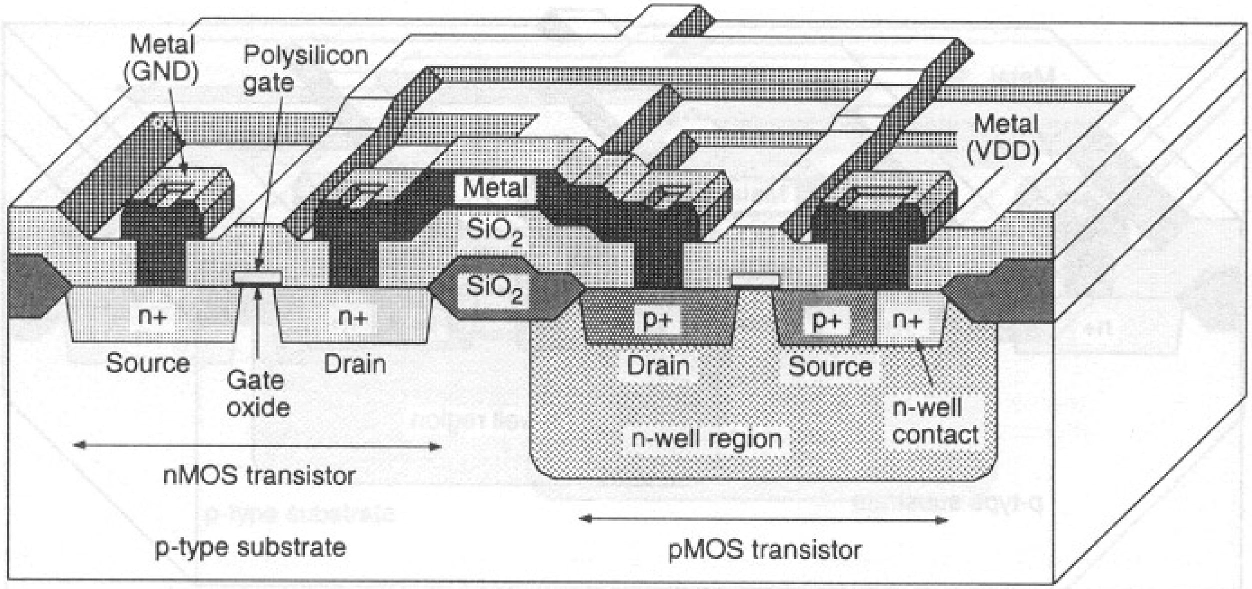
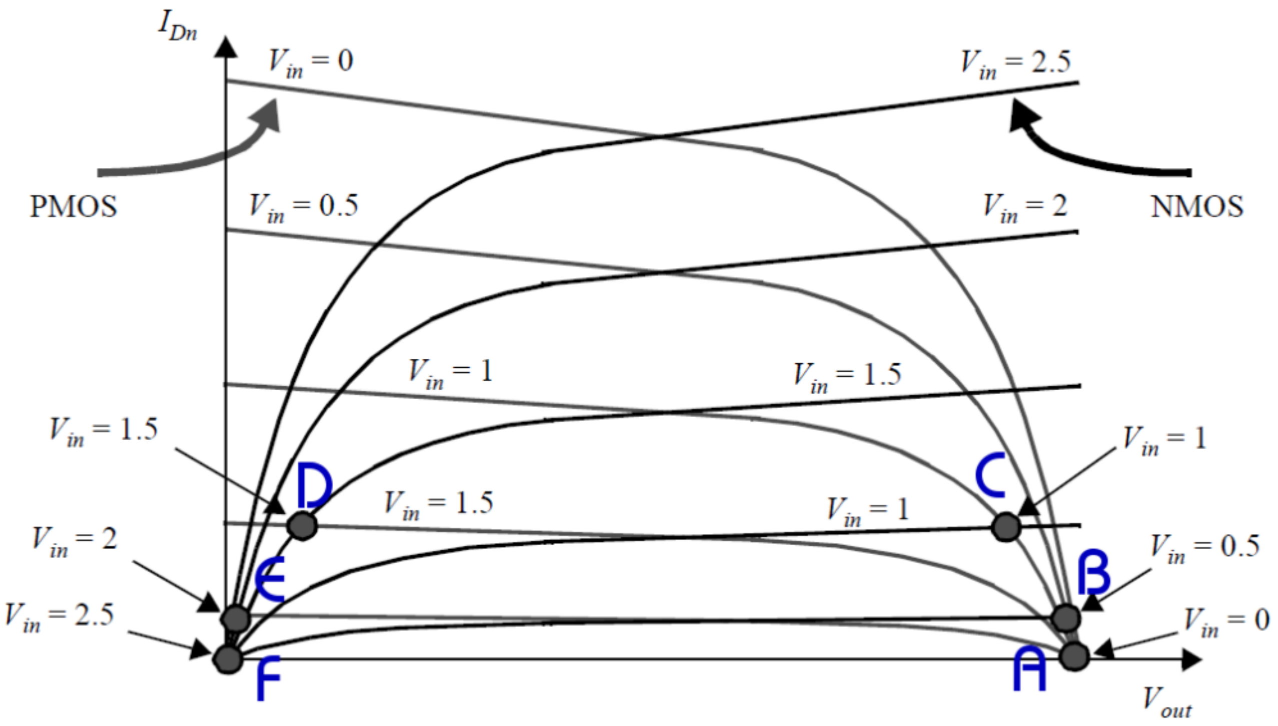
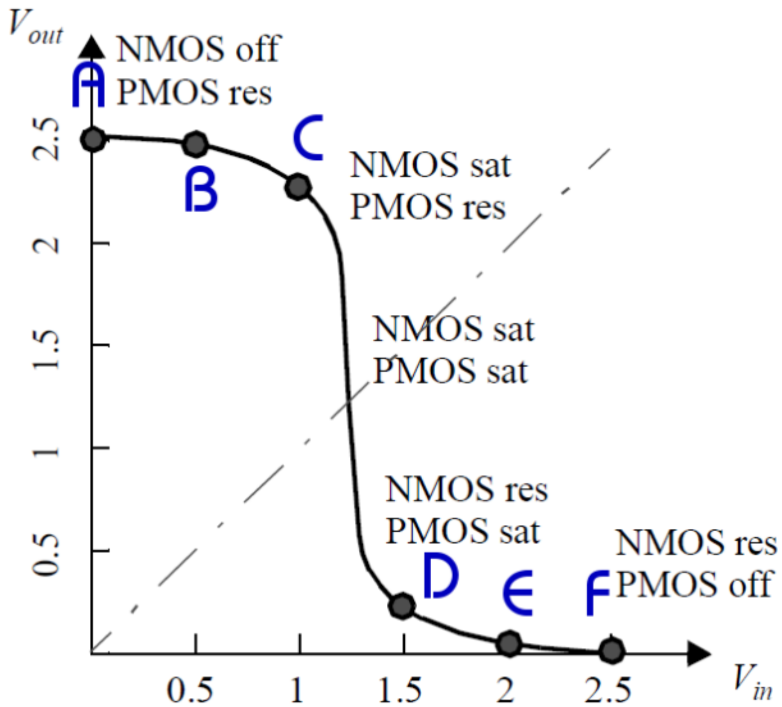


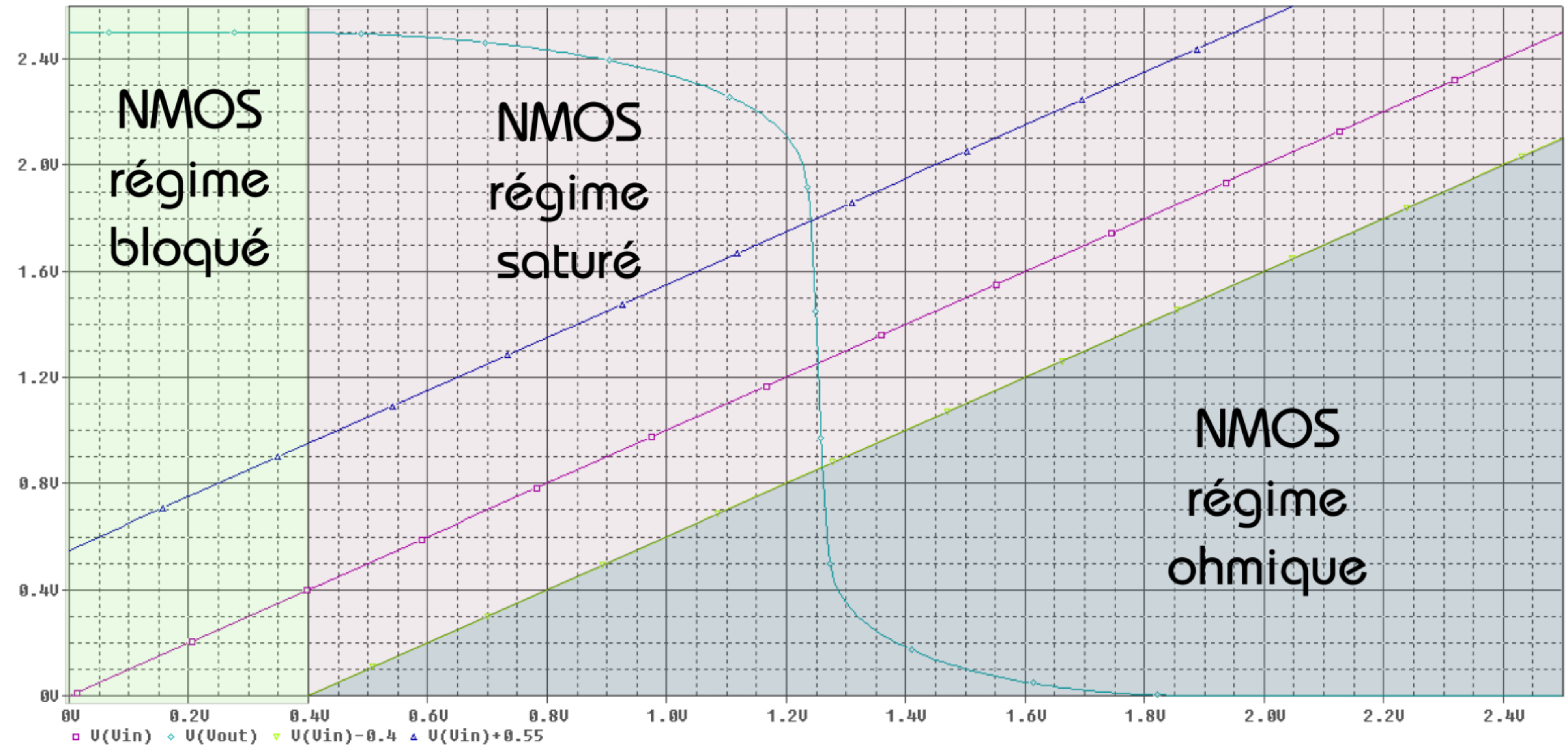
ÉCOLE CENTRALE LYON

Caractéristique de transfert



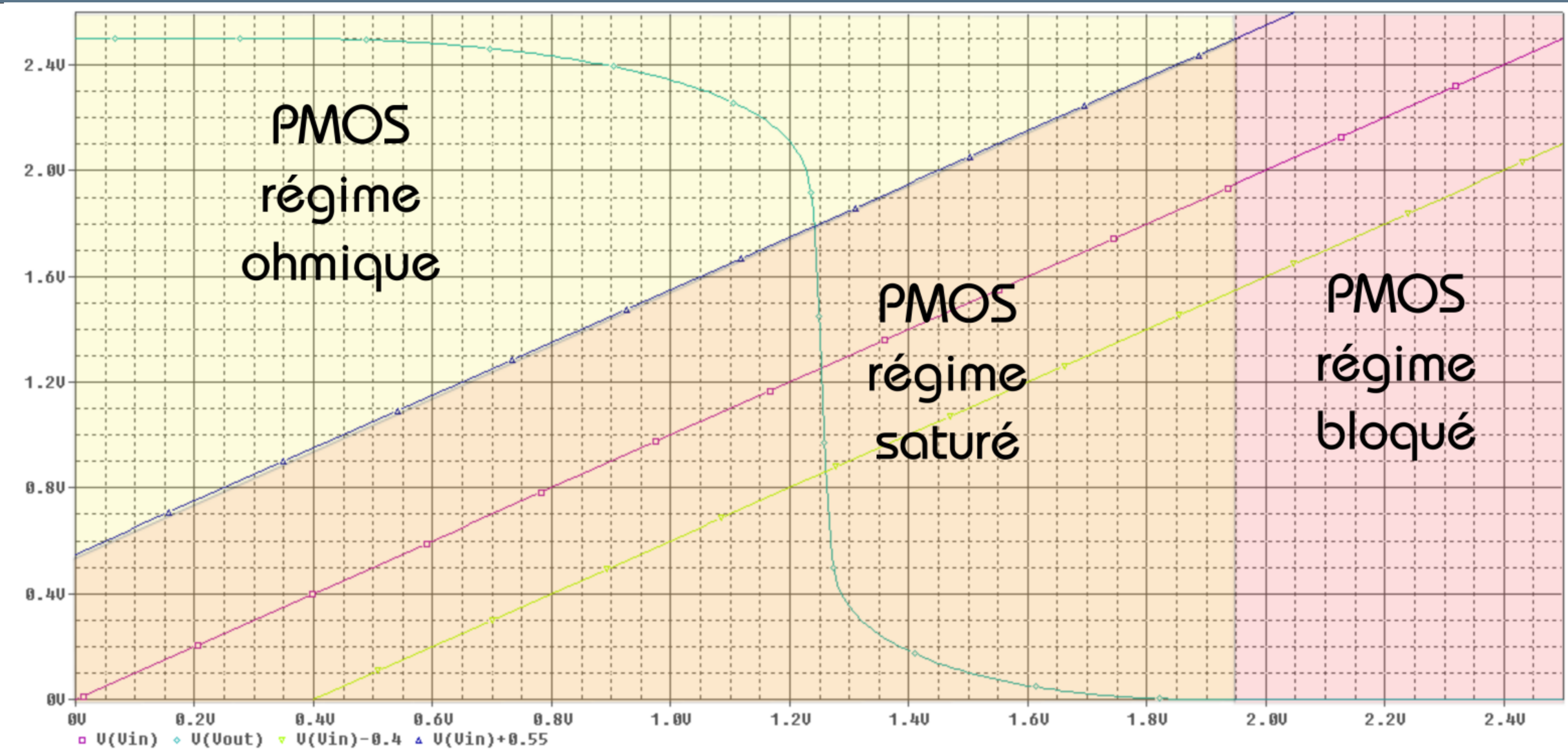


Le NMOS?



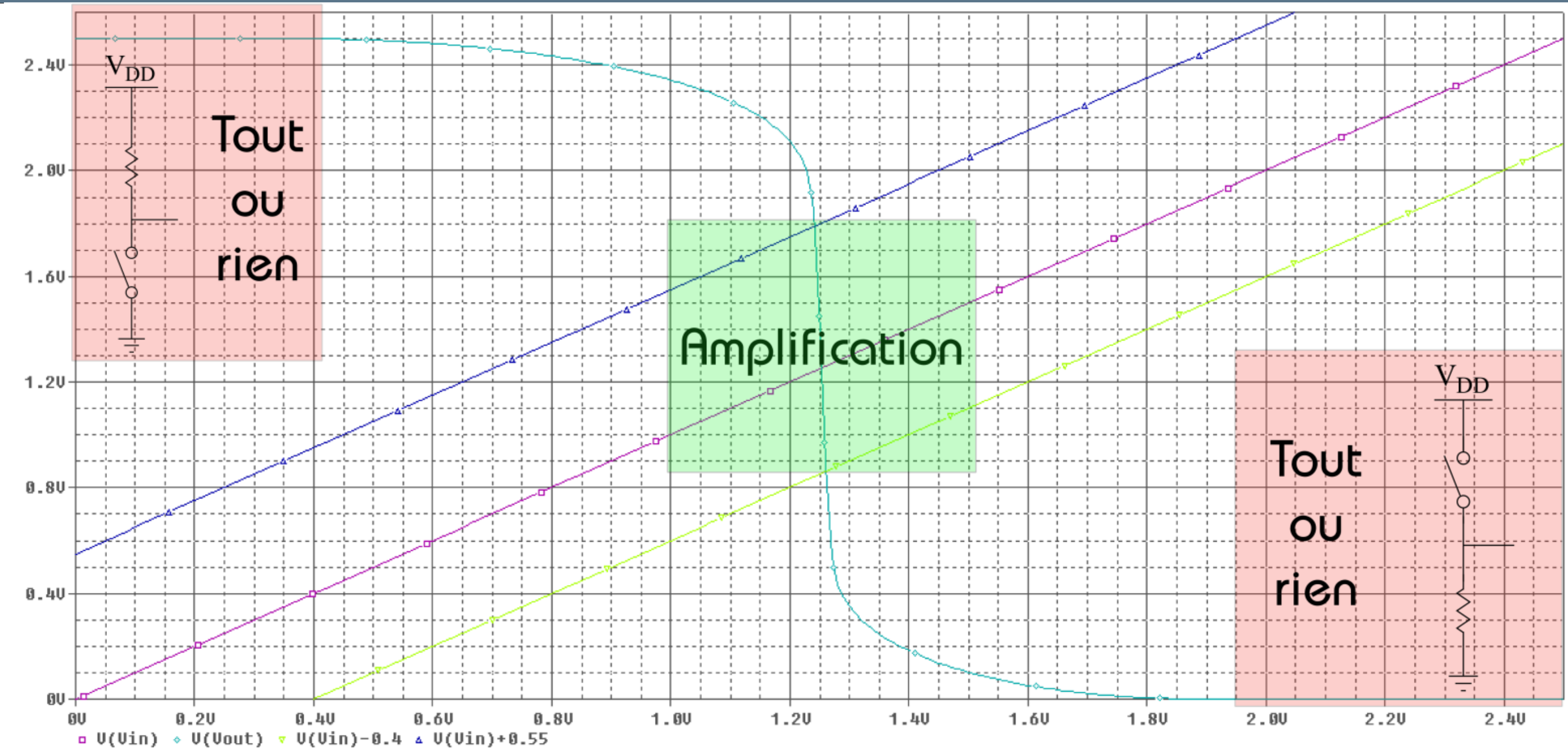
NMOS régime bloqué
NMOS régime saturé
NMOS régime ohmique
2.4V
2.0V
1.6V
1.2V
0.8V
0.4V
0V
0V 0.2V 0.4V 0.6V 0.8V 1.0V 1.2V 1.4V 1.6V 1.8V 2.0V 2.2V 2.4V
V(Vin) V(Vout) V(Vin)-0.4 V(Vin)+0.55

Le PMOS?

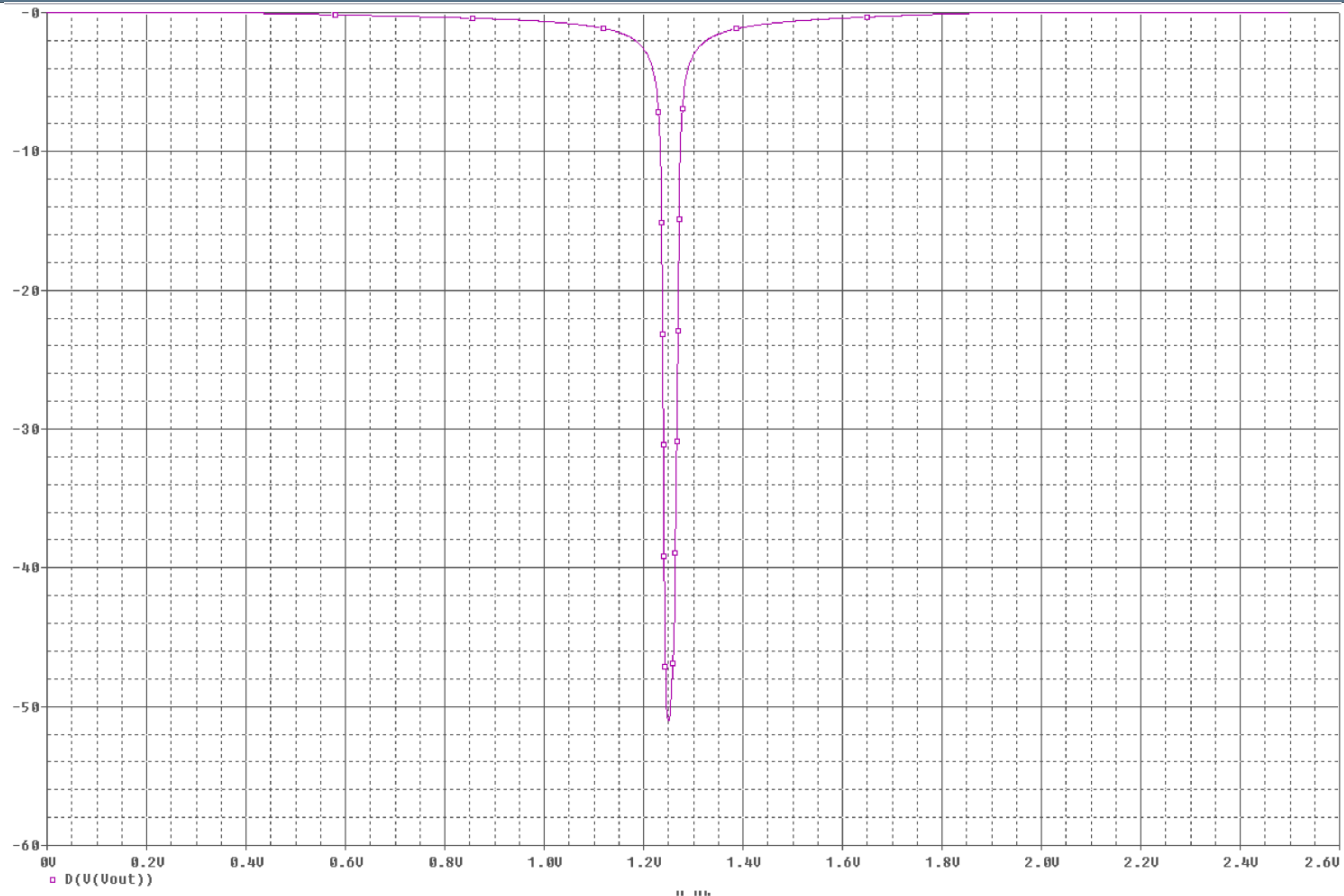


ÉCOLE CENTRALE LYON

Deux régimes de fonctionnement



Dérivons I_{ds} par rapport à V_{DS}



Point de fonctionnement idéal

Égalité des courants

$$I_{DSn} = \frac{K_n}{2}(V_{GSn} - V_{Tn})^2 \cdot (1 + \lambda \cdot V_{DSn}) = I_{DSp} = \frac{K_p}{2}(V_{SGp} - |V_{Tp}|)^2 \cdot (1 + \lambda \cdot V_{SDp})$$

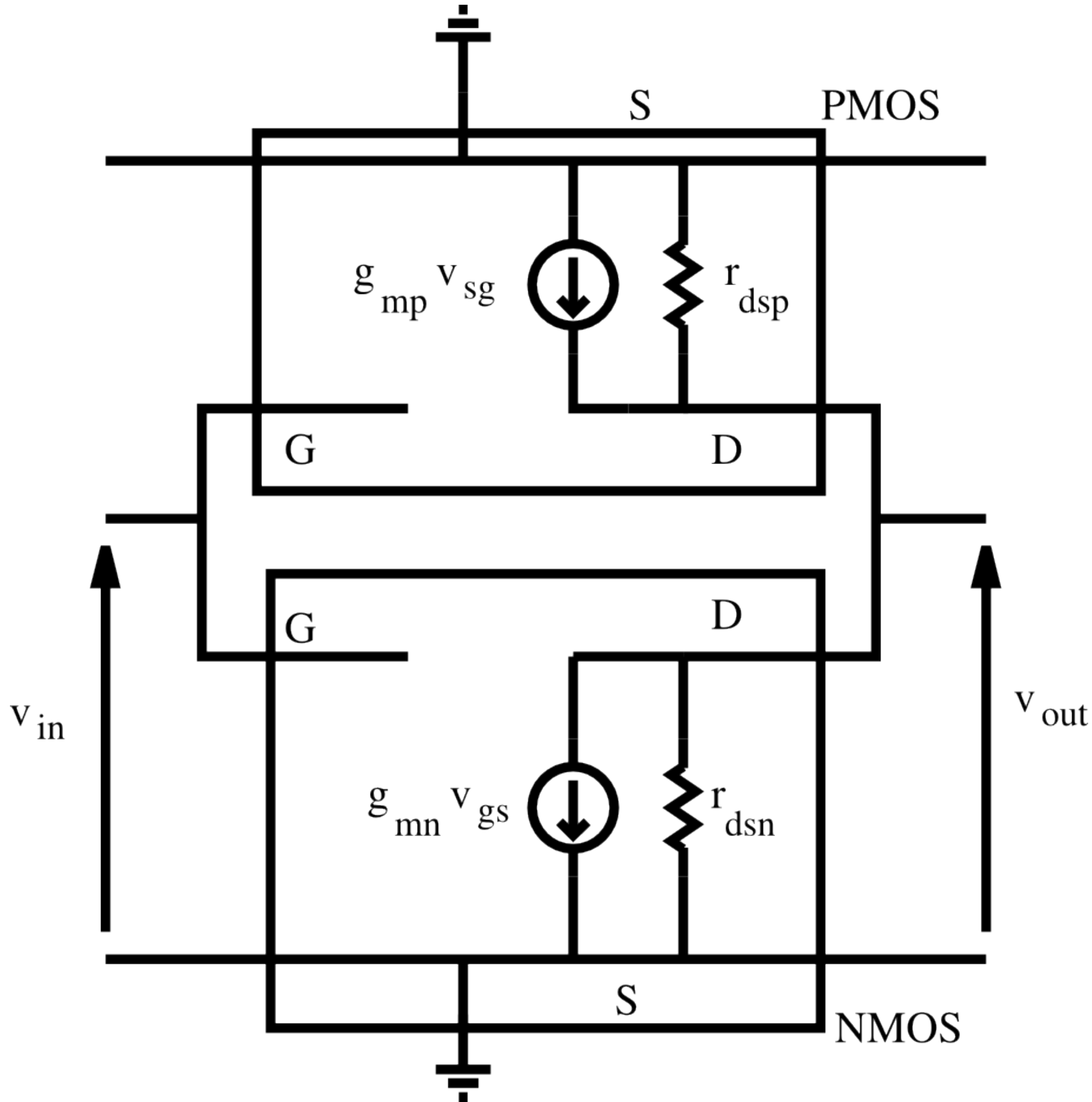
Équation Équation Équation

Redéfinissons le problème : $V_{IN} = \frac{V_{DD}}{2}$

$$K_n \left(\frac{V_{DD}}{2} - V_{Tn}\right)^2 \cdot (1 + \lambda \cdot V_{OUT}) = K_p \left(V_{DD} - \frac{V_{DD}}{2} - |V_{Tp}|\right)^2 \cdot (1 + \lambda \cdot (V_{DD} - V_{OUT}))$$

Considérons un cas particulier : $V_{OUT} = V_{IN} = \frac{V_{DD}}{2}$ $\Rightarrow \frac{\frac{W_n}{L_n}}{\frac{W_p}{L_p}} = \frac{\mu_p}{\mu_n}$

Modèle petit signal de l'inverseur CMOS



Modèle quadripolaire