

Pynqrypt

A FPGA-accelerated encryption library for PYNQ

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FPGA101 - Politecnico di Milano

January 9, 2023

The Hardware

PYNQ

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Encryption Algorithms

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AES-CTR

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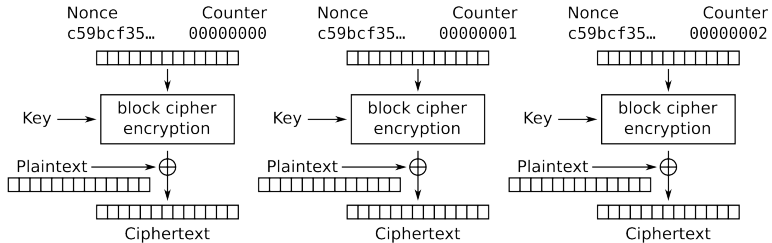
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AES-CTR

AES-CTR is a mode of operation for the AES block cipher. It is a highly-parallelizable and efficient encryption algorithm, well suited for hardware acceleration.

AES-CTR



Counter (CTR) mode encryption

Performance Considerations

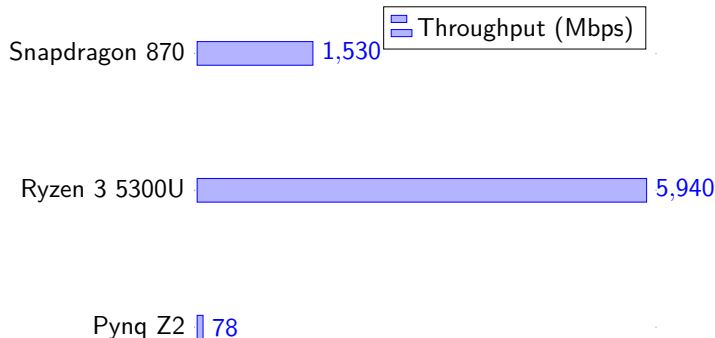
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Performance Comparison

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Throughput (Mbps)

Snapdragon 870 1,530

Ryzen 3 5300U 5,940

Pynq Z2 - Pynqrypt 441

Pynq Z2 - CPU 78

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```
data = np.frombuffer(... , np.uint8)
```

```
pynqrypt.set_key(...)
pynqrypt.set_nonce(...)
pynqrypt.set_length(len(data))
```

Usage

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```
input_buffer = pynqrypt.get_input_array()  
output_buffer = pynqrypt.get_output_array()  
  
input_buffer[:] = data[:]  
  
pynqrypt.prepare()  
pynqrypt.run_blocking()
```

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input_buffer = pynqrypt.get_input_array()  
output_buffer = pynqrypt.get_output_array()
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```
input_buffer[:] = data[:]
```

```
pynqrypt.prepare()  
pynqrypt.run_blocking()
```

```
output_buffer.invalidate()
```

```
... = bytes(output_buffer)
```

```
pynqrypt.cleanup()
```

USBCrypt: let's see it in action!

Issues Encountered

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Maybe rewatch the lesson?

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- On-the-fly reconfigurability allows for multiple libraries to share the same hardware

Drawbacks

- Not every task is suitable for an FPGA, and some platform-specific optimization is required for best results
- Hardware accelerated libraries might not always be a drop-in replacement, some code refactoring might be required

Personal Thoughts

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- Vitis HLS is magical, and makes it easy to write software for FPGAs...
... but it is also broken, badly documented and finicky to use.
- Pynq is a great platform for development and prototyping, but it is not intuitive to use and the documentation is lacking.
- Sometimes I felt like I was just throwing things at the wall and hoping they would stick.

The End

Thanks for your attention!