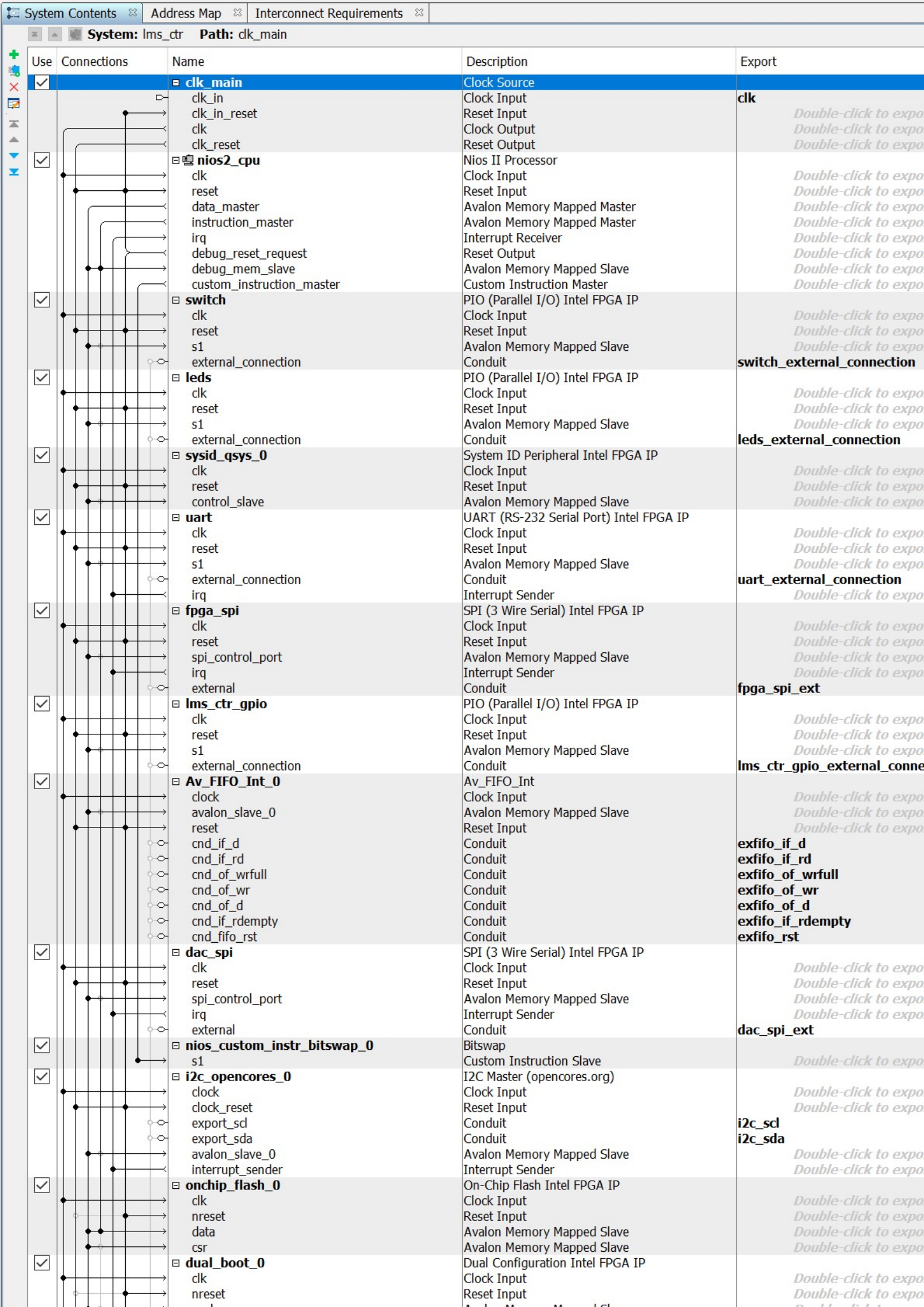
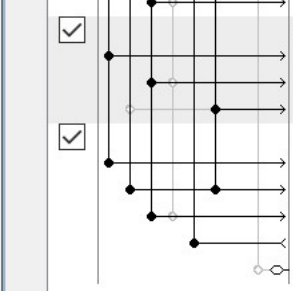
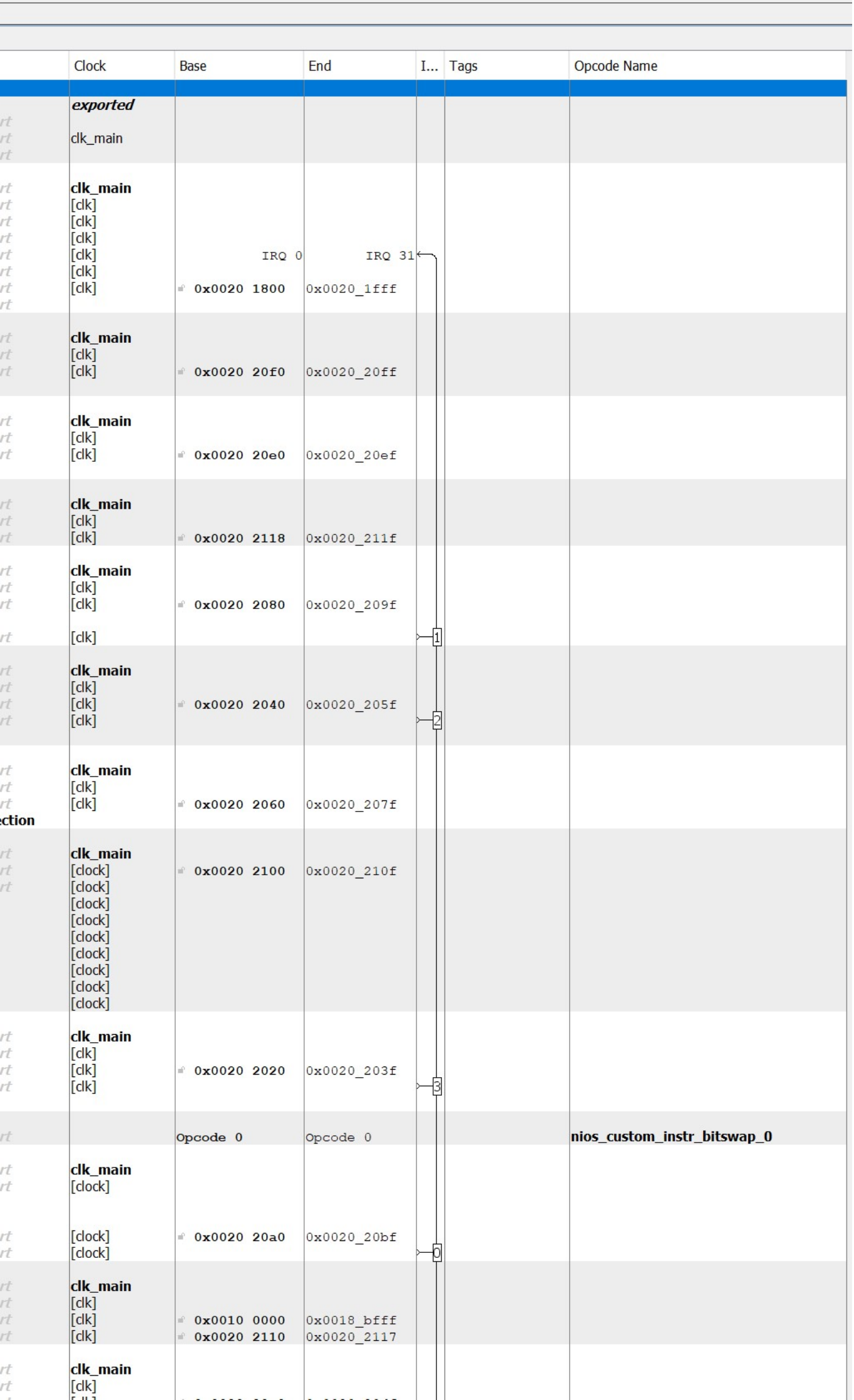

System Contents
Address Map
Interconnect Requirements
System: lms_ctr Path: clk_main
Use
Connections
Name
Description
Export
clk_main
Clock Source
clk_in
Clock Input
clk
clk_in_reset
Reset Input
clk
Clock Output
clk_reset
Reset Output
nios2_cpu
Nios II Processor
clk
Clock Input
reset
Reset Input
data_master
Avalon Memory Mapped Master
instruction_master
Avalon Memory Mapped Master
irq
Interrupt Receiver
debug_reset_request
Reset Output
debug_mem_slave
Avalon Memory Mapped Slave
custom_instruction_master
Custom Instruction Master
switch
PIO (Parallel I/O) Intel FPGA IP
clk
Clock Input
reset
Reset Input
s1
Avalon Memory Mapped Slave
external_connection
Conduit
switch_external_connection
leds
PIO (Parallel I/O) Intel FPGA IP
clk
Clock Input
reset
Reset Input
s1
Avalon Memory Mapped Slave
external_connection
Conduit
leds_external_connection
sysid_qsys_0
System ID Peripheral Intel FPGA IP
clk
Clock Input
reset
Reset Input
control_slave
Avalon Memory Mapped Slave
uart
UART (RS-232 Serial Port) Intel FPGA IP
clk
Clock Input
reset
Reset Input
s1
Avalon Memory Mapped Slave
external_connection
Conduit
uart_external_connection
irq
Interrupt Sender
fpga_spi
SPI (3 Wire Serial) Intel FPGA IP
clk
Clock Input
reset
Reset Input
spi_control_port
Avalon Memory Mapped Slave
irq
Interrupt Sender
external
Conduit
fpga_spi_ext
lms_ctr_gpio
PIO (Parallel I/O) Intel FPGA IP
clk
Clock Input
reset
Reset Input
s1
Avalon Memory Mapped Slave
external_connection
Conduit
lms_ctr_gpio_external_conne
Av_FIFO_Int_0
Av_FIFO_Int
clock
Clock Input
avalon_slave_0
Avalon Memory Mapped Slave
reset
Reset Input
cnd_if_d
Conduit
exfifo_if_d
cnd_if_rd
Conduit
exfifo_if_rd
cnd_of_wrfull
Conduit
exfifo_of_wrfull
cnd_of_wr
Conduit
exfifo_of_wr
cnd_of_d
Conduit
exfifo_of_d
cnd_if_rdempty
Conduit
exfifo_if_rdempty
cnd_fifo_rst
Conduit
exfifo_rst
dac_spi
SPI (3 Wire Serial) Intel FPGA IP
clk
Clock Input
reset
Reset Input
spi_control_port
Avalon Memory Mapped Slave
irq
Interrupt Sender
external
Conduit
dac_spi_ext
nios_custom_instr_bitswap_0
Bitswap
s1
Custom Instruction Slave
i2c_opencores_0
I2C Master (opencores.org)
clock
Clock Input
clock_reset
Reset Input
export_scl
Conduit
i2c_scl
export_sda
Conduit
i2c_sda
avalon_slave_0
Avalon Memory Mapped Slave
interrupt_sender
Interrupt Sender
onchip_flash_0
On-Chip Flash Intel FPGA IP
clk
Clock Input
nreset
Reset Input
data
Avalon Memory Mapped Slave
csr
Avalon Memory Mapped Slave
dual_boot_0
Dual Configuration Intel FPGA IP
clk
Clock Input
nreset
Reset Input
Double-click to expo



	avalon	Avalon Memory Mapped Slave	Double-click to expo
☑	**onchip_memory2_0**	On-Chip Memory (RAM or ROM) Intel FPGA IP	
	clk1	Clock Input	Double-click to expo
	s1	Avalon Memory Mapped Slave	Double-click to expo
	reset1	Reset Input	Double-click to expo
☑	**flash_spi**	SPI (3 Wire Serial) Intel FPGA IP	
	clk	Clock Input	Double-click to expo
	reset	Reset Input	Double-click to expo
	spi_control_port	Avalon Memory Mapped Slave	Double-click to expo
	irq	Interrupt Sender	Double-click to expo
	external	Conduit	**flash_spi**


Clock
Base
End
I...
Tags
Opcode Name
exported
clk_main
clk_main
[clk]
[clk]
[clk]
[clk]
[clk]
[clk]
IRQ 0
IRQ 31
0x0020 1800
0x0020_1fff
clk_main
[clk]
[clk]
0x0020 20f0
0x0020_20ff
clk_main
[clk]
[clk]
0x0020 20e0
0x0020_20ef
clk_main
[clk]
[clk]
0x0020 2118
0x0020_211f
clk_main
[clk]
[clk]
0x0020 2080
0x0020_209f
[clk]
1
clk_main
[clk]
[clk]
0x0020 2040
0x0020_205f
[clk]
2
clk_main
[clk]
[clk]
0x0020 2060
0x0020_207f
clk_main
[clock]
[clock]
[clock]
[clock]
[clock]
[clock]
[clock]
[clock]
[clock]
0x0020 2100
0x0020_210f
clk_main
[clk]
[clk]
0x0020 2020
0x0020_203f
[clk]
3
Opcode 0
Opcode 0
nios_custom_instr_bitswap_0
clk_main
[clock]
[clock]
[clock]
0x0020 20a0
0x0020_20bf
0
clk_main
[clk]
[clk]
[clk]
0x0010 0000
0x0018_bfff
0x0020 2110
0x0020_2117
clk_main
[clk]

[clk]	0x0020 20c0	0x0020_20df
clk_main		
[clk1]	0x0020 0000	0x0020_0fff
[clk1]		
clk_main		
[clk]		
[clk]	0x0020 2000	0x0020_201f
[clk]