1. General Description

The Pico Timer/Counter (pTC) consists of an 8-bit synchronous counter that counts cycles of an externally-supplied signal. As such, it can be used to count both clock pulses and events. It also includes a match register to generate interrupt events at specified counter values.

2. Applications

- Free running timer
- Interval timer
- Event counter

3. Features

- 8-bit up counter
- Synchronous counting
- Programmable match register
- Interrupt event on compare match
- Available in 24-pin SPDIP
- Single 5V Power Supply
- TTL-compatible inputs and outputs

4. Architecture

The logic block diagram of the pTC is shown in Figure 1.

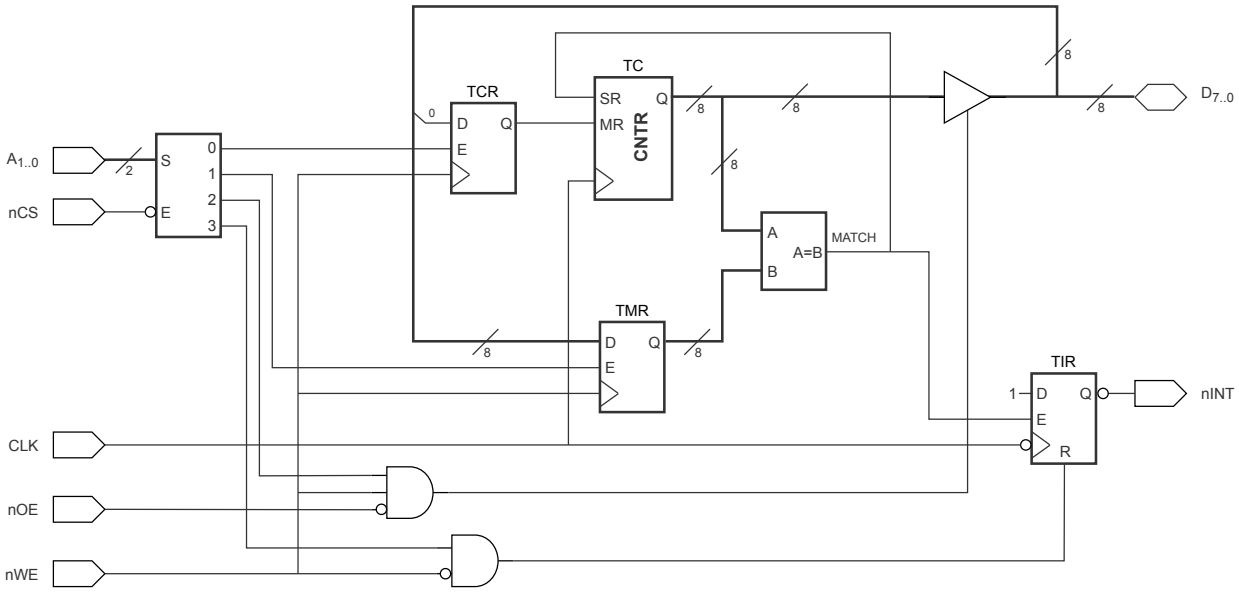

Figure 1: Logic block diagram

5. Functional Description

The pTC counts in modulo-8 binary sequence. From value `0x00` it increments to value `0xFF` and then rools over to the value `0x00`. The clock inputs of all the counter flip-flops are driven in parallel through a clock buffer. Thus, all changes of the Timer Counter (TC) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CLK input signal.

The circuit has three fundamental modes of operation, in order of precedence: asynchronous reset and hold, synchronous reset, and count-up. The current mode of operation is determined by two control signals. A HIGH signal on MR inhibits counting and forces the value `0x00` to the TC. A HIGH signal on SR overrides counting and causes the TC to go to the value `0x00` on the next rising edge of CLK. Counting is permitted when both MR and SR are LOW.

The counter value is continuously compared to the Timer Match Register (TMR) to determine whether the counter has reached that user-defined value. On a comparison match, an interrupt is generated on the Timer Interrupt Register (TIR) on the next falling edge of CLK. The TIR can be written to clear these interrupts. A comparison match also makes the counter go to the value `0x00` in the next rising edge of CLK. Hence, the value of the TMR and the frequency of the CLK input signal determine the maximum time resolution achievable with the pTC.

The nCS and A input signals are used in conjunction with the nOE input signal to read the TC value. Both signals are also used in conjunction with the nWE input signal to write commands into the Timer Control Register (TCR) and TIR, as well as data values into the TMR. A LOW signal on nCS enables such reading and writing operations. Still, no reading or writing will occur unless the nOE or the nWE are LOW, respectively.

6. Pin configuration

The pin configuration of the pTC when implemented using an ATMEL ATF750C CPLD is shown in Figure 2.

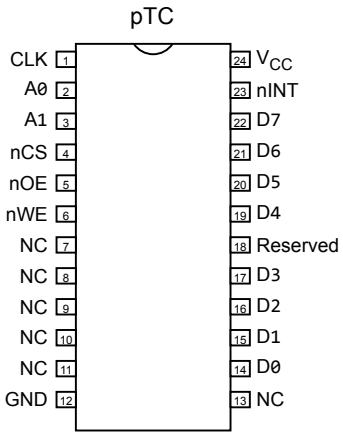

Figure 2: Pin configuration for SPDIP (NC means no internal connection)

7. Pin description

Table 1 gives a brief summary of each of the pTC related pins.

Table 1: Pin description

Pin	Name	Type	Description
1	CLK	I	Clock input
2,3	A	I	Address input
4	nCS	I	Chip select input
5	nOE	I	Output enable input
6	nWE	I	Write enable input
12	GND	S	Ground
14, 15, 16, 17, 19, 20, 21, 22	D	I/O	Bidirectional data bus
23	nINT	O	Interrupt output
24	VCC	S	Power supply +5 V

Note: I = Input, O = Output, S = Supply

8. Register Descriptions

The pTC contains the registers shown in Table 2. More detailed descriptions are presented in the following subsections.

Table 2: Register map

Name	Description	Access Type	Reset Value	Address
TCR	The Timer Control Register is used to control the counter operation.	WO	0	0
TMR	The Timer Match Register holds the match value.	WO	0	1
TC	The Timer Counter register contains the current counter value.	RO	0	2
TIR	The Timer Interrupt Register identifies a pending match interrupt.	WO	0	3

Note: RO = Read only, WO = Write only.

8.1. Timer Control Register (TCR)

The 1-bit TCR is used to control the operation of the pTC. When TCR is set to HIGH, the counter is stopped and the TC is asynchronously cleared. Counting remains disabled and the TC value is fixed at `0x00` until the TCR bit is returned to zero.

8.2. Timer Match Register (TMR)

The 8-bit TMR value is continuously compared to the TC value. When the two values are equal, two actions are triggered automatically: (i) an interrupt is generated and (ii) the TC is reset in the following rising edge of CLK.

8.3. Timer Counter (TC)

The 8-bit TC is incremented on every cycle of CLK. When the counting reaches the TMR value, the counter is set to zero in the next rising edge of CLK. This event also sets the interrupt flag in the TIR, which can be used to detect a counting overflow if needed.

The TC operation is controlled through the TCR.

8.4. Timer Interrupt Register (TIR)

The TIR consists of an 1-bit register for the match interrupt. Whenever an interrupt is generated this bit is set HIGH. Writing to TIR clears the pending interrupt.

9. Waveforms

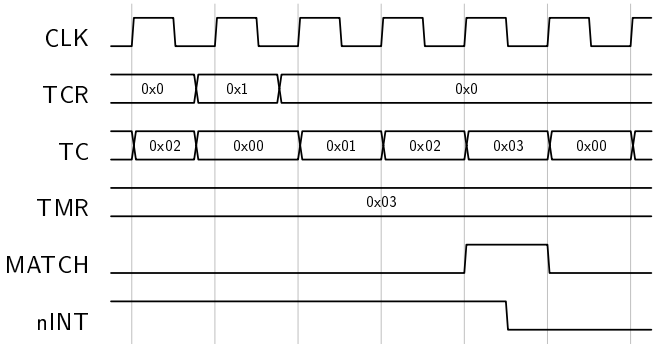

Figure 3: Counting with a match event

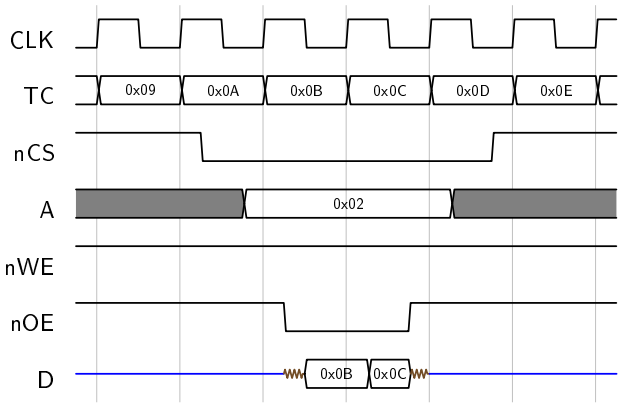

Figure 4: Reading the value of the TC

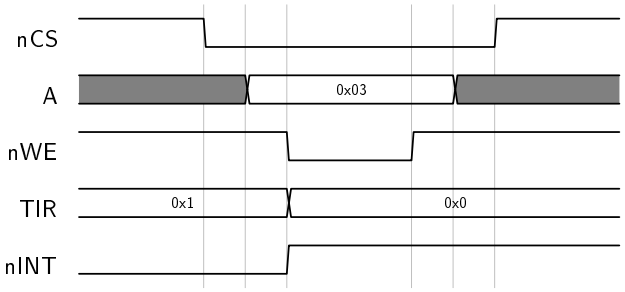

Figure 5: Writing to TIR to clear an interrupt

10. Abbreviations

pTC	Pico Timer/Counter
SPDIP	Skinny Plastic Dual In-line Package
TC	Timer Counter
TCR	Timer Control Register
TIR	Timer Interrupt Register
TMR	Timer Match Register

11. Revision history

Revision	Date	Description
1.0	May 2021	Initial release.
1.1	Jun 2021	Updated the description in section 8.3 and figures 1, 2, 3, 4 and 5.

12. Legal information

12.1. Disclaimers

Limited warranty and liability – Information in this document is provided only for your convenience and may be superseded by updates. We believe the information to be accurate and reliable. However, we do not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes – We reserve the right to make changes to information published in this document at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

12.2. Trademarks

All referenced brands, product names, service names and trademarks are the property of their respective owners.

Contents