





## **Design Rules Verification Report**

Filename: C:\ProgramData\Altium\CircuitMaker {382DEE72-D86A-42B9-BAC2-0111D092FF90}\Projects\848933AC-9F1C-44E3-8F1 C-68CEACBCBD93\65a71a72-7911-418c-9cee-440acca976dc\bph.CMPcbDoc

Warnings 0 Rule Violations 0

L oto	
Total Total	

Rule Violations	
Unpoured Polygon (Allow unpoured: False)	0
Net Antennae (Tolerance=0mm) (All)	0
Silk primitive without silk layer	0
Silk to Silk (Clearance=0.051mm) (All),(All)	0
Silk To Solder Mask (Clearance=0.051mm) (IsPad),(All)	0
Minimum Solder Mask Sliver (Gap=0.025mm) (All),(All)	0
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Hole Size Constraint (Min=0.025mm) (Max=2.54mm) (All)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Width Constraint (Min=0.254mm) (Max=0.508mm) (Preferred=0.254mm) (All)	0
Power Plane Connect Rule(Relief Connect )(Expansion=0.508mm) (Conductor Width=0.254mm)	0
Clearance Constraint (Gap=0.203mm) (All),(All)	0
Un-Routed Net Constraint ( (All) )	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Clearance Constraint (Gap=0.305mm) (InPolygon),(All)	0
Total	0

Monday 10 Jun 2019 4:36:44 PM Page 1 of 1

## **Electrical Rules Check Report**

Class	Document	Message
		Successful Compile for bph.PrjPcb