





Electrical Rules Check Report

Class	Document	Message
		Successful Compile for bph.PrjPcb

Design Rules Verification Report

Filename: C:\ProgramData\Altium\CircuitMaker {8EBB6731-1AD7-46CA-96B8-AC039FD36340}\Projects\848933AC-9F1C-44E3-8F1C-68CEACBCBD93\65a71a72-7911-418c-9cee-440acca976dc\bph.CMPcbDoc

Warnings 0 Rule Violations 0

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=12mil) (InPolygon),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Clearance Constraint (Gap=8mil) (All),(All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=20mil) (Conductor Width=10mil) (Air	0
Width Constraint (Min=10mil) (Max=20mil) (Preferred=10mil) (All)	0
Height Constraint (Min=0mil) (Max=1000mil) (Prefered=500mil) (All)	0
Hole Size Constraint (Min=1mil) (Max=100mil) (All)	0
Hole To Hole Clearance (Gap=10mil) (All),(All)	0
Minimum Solder Mask Sliver (Gap=1mil) (All),(All)	0
Silk To Solder Mask (Clearance=2mil) (IsPad),(All)	0
Silk to Silk (Clearance=2mil) (All),(All)	0
Silk primitive without silk layer	0
Net Antennae (Tolerance=0mil) (All)	0
Unpoured Polygon (Allow unpoured: False)	0
Total	0