CS 223

Digital Design

Section 5 Lab 4

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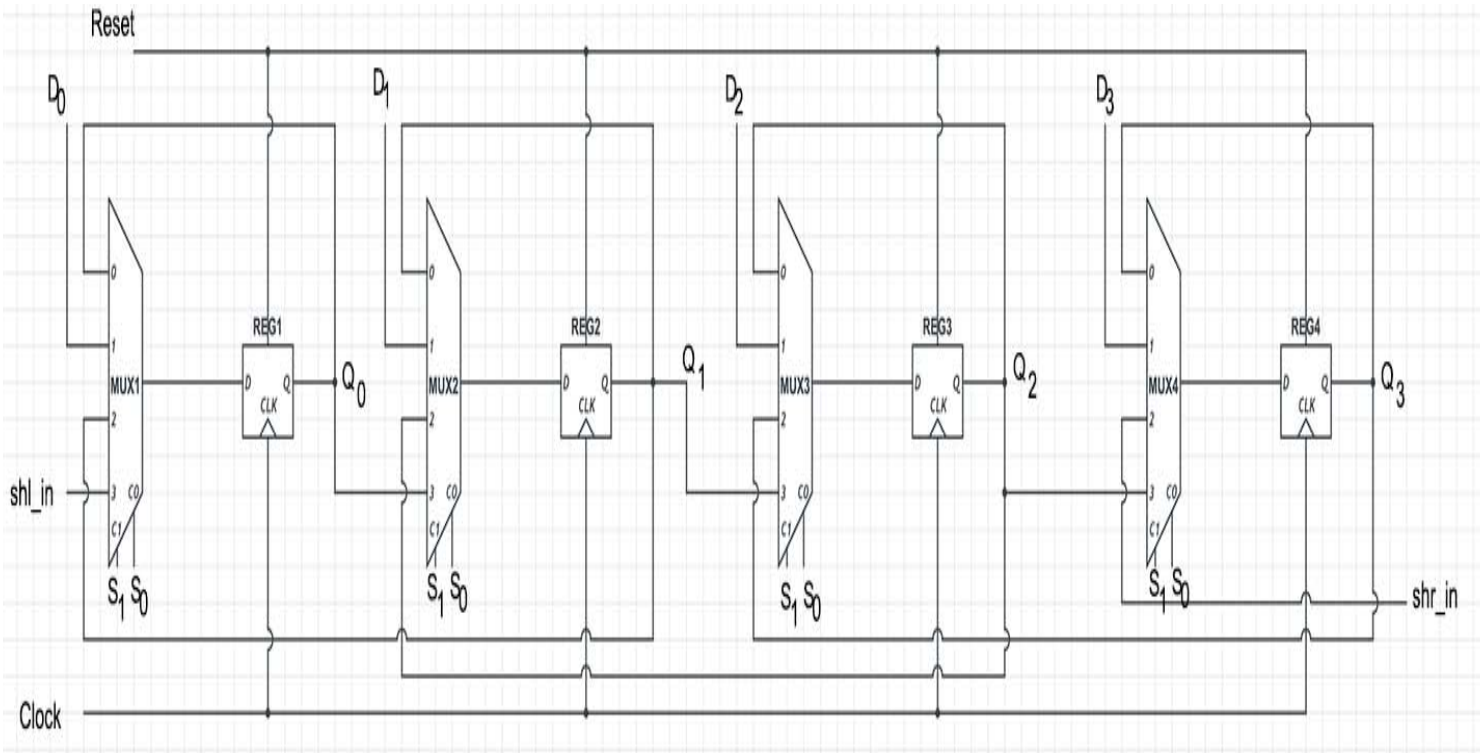
b)System Verilog Module For Synchronously Resettable D flip-flop

```
module resettableflop(
    input logic clk,
    input logic reset,
    input logic d,
    output logic q
    );
    //sync reset
    always_ff @(posedge clk)
        if(reset) q <= 1'b0;
        else q <= d;
endmodule
```

c) Circuit schematic for the internal design of the multifunction register by using 4:1 multiplexers and synchronously resettable D flip-flops.



***d)* Structural SystemVerilog module for the multifunction register designed in part (c) and a testbench for it.**

```
module multifunctionreg(
    input logic clk,
    input logic reset,
    input logic shl_in,
    input logic shr_in,
    input logic [1:0] s,
    input logic [3:0] D,
    output logic [3:0] Q
    );
        logic m1, m2, m3, m4;

        mux4to1 firstMux(Q[2], shr_in, D[3], Q[3], s, m1);
        resettableflop r1(clk, reset, m1, Q[3]);

        mux4to1 secondMux(Q[1], Q[3], D[2], Q[2], s, m2);
        resettableflop r2(clk, reset, m2, Q[2]);

        mux4to1 thirdMux(Q[0], Q[2], D[1], Q[1], s, m3);
        resettableflop r3(clk, reset, m3, Q[1]);

        mux4to1 fourthMux(shl_in, Q[1], D[0], Q[0], s, m4);
        resettableflop r4(clk, reset, m4, Q[0]);

endmodule
```

```
module mux2to1(
    input d1,
    input d0,
    input s,
    output y
    );
    assign y = s ? d1 : d0;
endmodule
```

```
module mux4to1(
    input d3,
    input d2,
    input d1,
    input d0,
    input [1:0] s,
    output y
    );
    logic [1:0] middle;
    mux2to1 lowmux2(d1, d0, s[0], middle[0]);
    mux2to1 highmux2(d3, d2, s[0], middle[1]);
    mux2to1 finalmux2( middle[1],middle[0], s[1], y);
endmodule
```

```
module multifunction_register_testbench();
    logic clk;
    logic reset;
    logic shl_in;
    logic shr_in;
    logic [1:0] s;
    logic [3:0] D;
    logic [3:0] Q;
    multifunctionreg r(clk, reset, shl_in, shr_in, s, D, Q);

    initial begin
        clk <= 0;
        s[0] = 1;
        s[1] = 0;
        D = 0;
        shr_in = 0;
        reset = 0;
        shl_in = 0;

        for(int i = 0; i < 4; i = i + 1)begin
            s[0] = i;
            s[1] = i / 2;
            for(int i = 0; i < 128; i = i + 1)begin
                {shl_in, shr_in, reset, D[3], D[2], D[1], D[0]} = i; #1;
                // above code puts 1 ps delay so that synchronous working can be seen in simulation
            end
            #1;
        end
    end
    // set clk tik to 2ps
    always #2 clk <= ~clk;
endmodule
```

I want you to sadly inform that I thought I could see the shifting on Basys3, but I didn't realize that I couldn't actually see it because the clock was so fast, all the output suddenly becomes shl_in or shr_in. That's why I'm uploading late. Please, I would be very happy if you would take that into consideration when looking at my report.