

Algoritmo de Tomasulo

Maio de 2021

Movimentação da memória

31	20 19	15 14	12 11	7 6	0
imm[11:0]	rs1	funct3	rd	opcode	
12	5	3	5	7	
offset[11:0]	base	width	dest	LOAD	

Operações aritméticas

31	25 24	20 19	15 14	12 11	7 6	0
funct7	rs2	rs1	funct3	rd	opcode	
7	5	5	3	5	7	
MULDIV	divisor	dividend	DIV	dest	OP	

Operações aritméticas

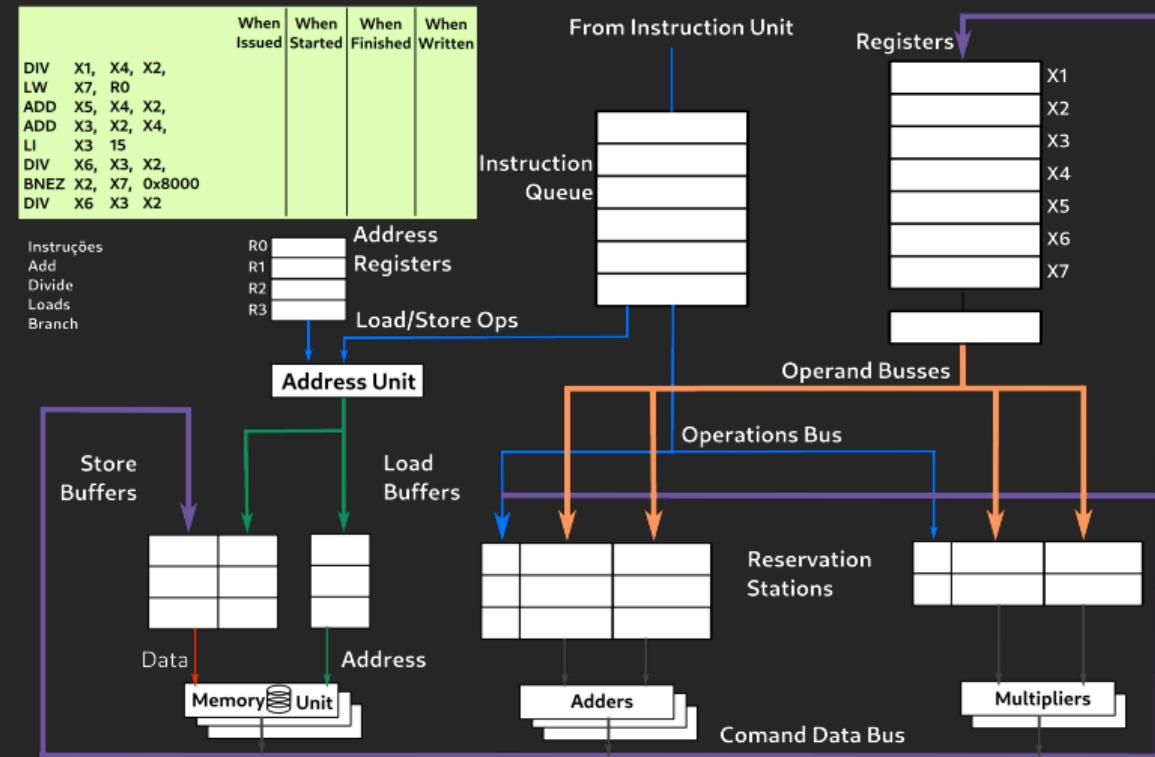
31	20 19	15 14	12 11	7 6	0
imm[11:0]	rs1	funct3	rd	opcode	
12 I-immediate[11:0]	5 src	3 ADD	5 dest	7 OP-IMM	

Desvio condicional

15	13 12	10 9	7 6	2 1	0
funct3	imm	rs1	imm	op	
3	3	3	5	2	
BNEZ	offset[8 4:3]	src	offset	CI	

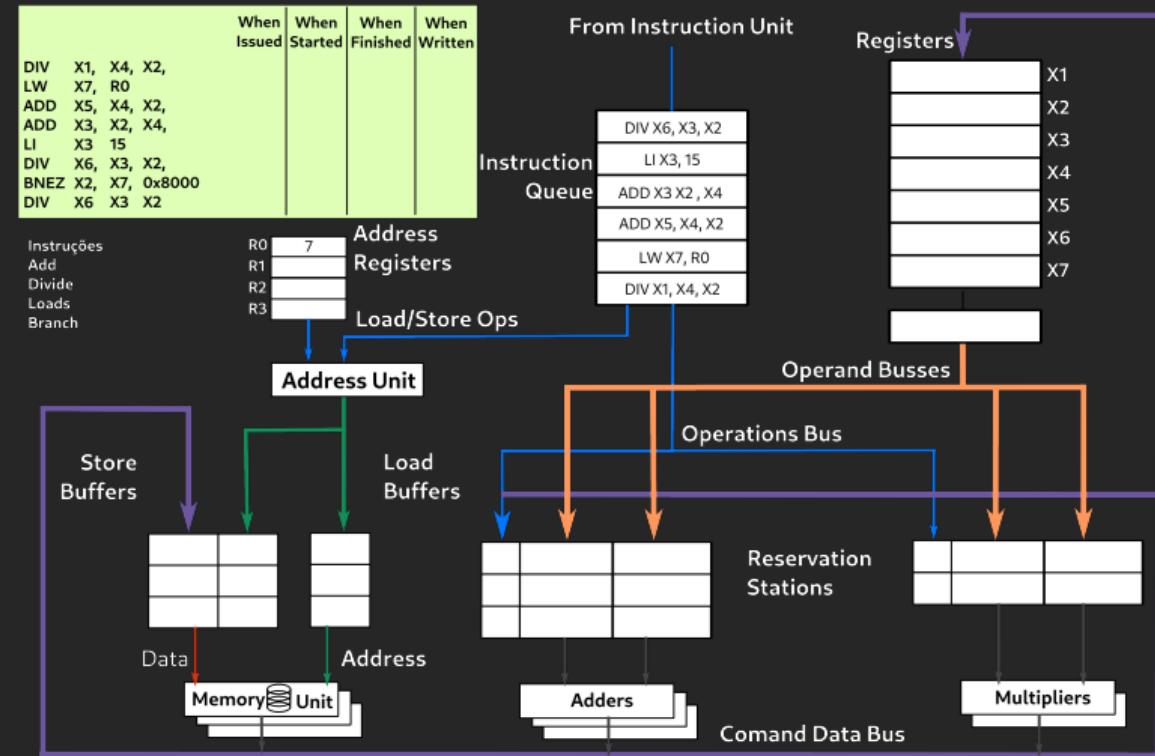
Simulação

Clock cycle: 0



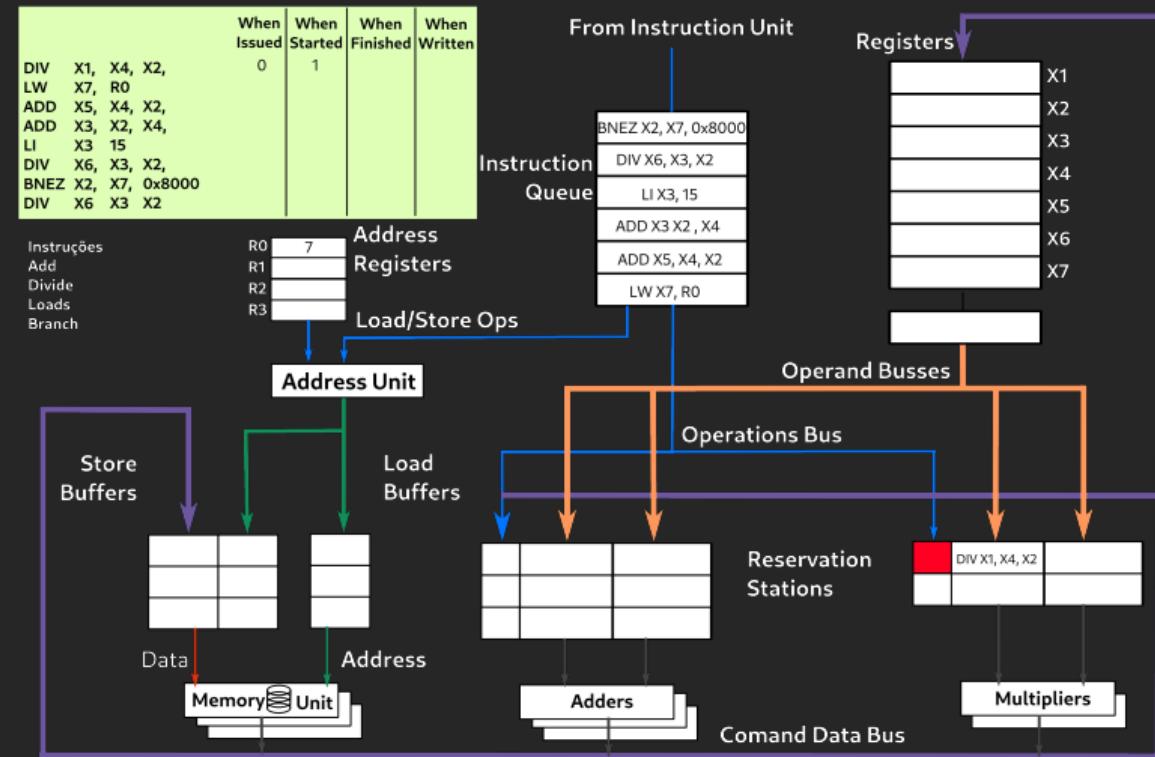
Simulação

Clock cycle: 0



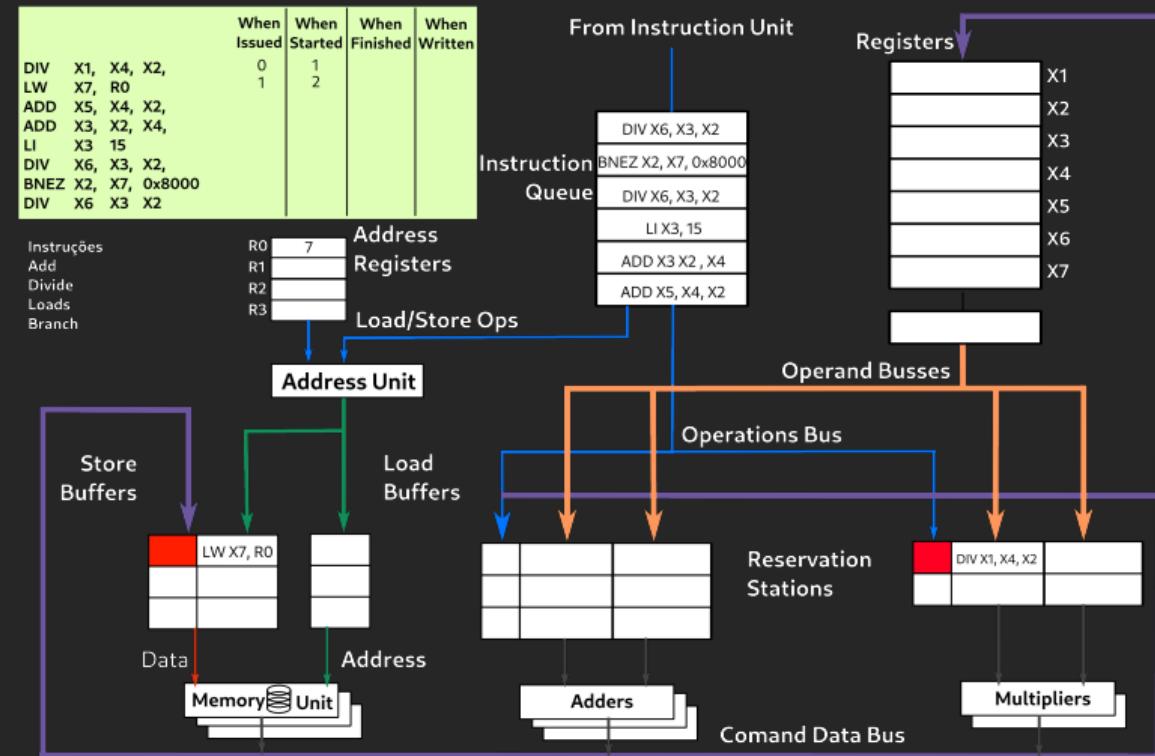
Simulação

Clock cycle: 1



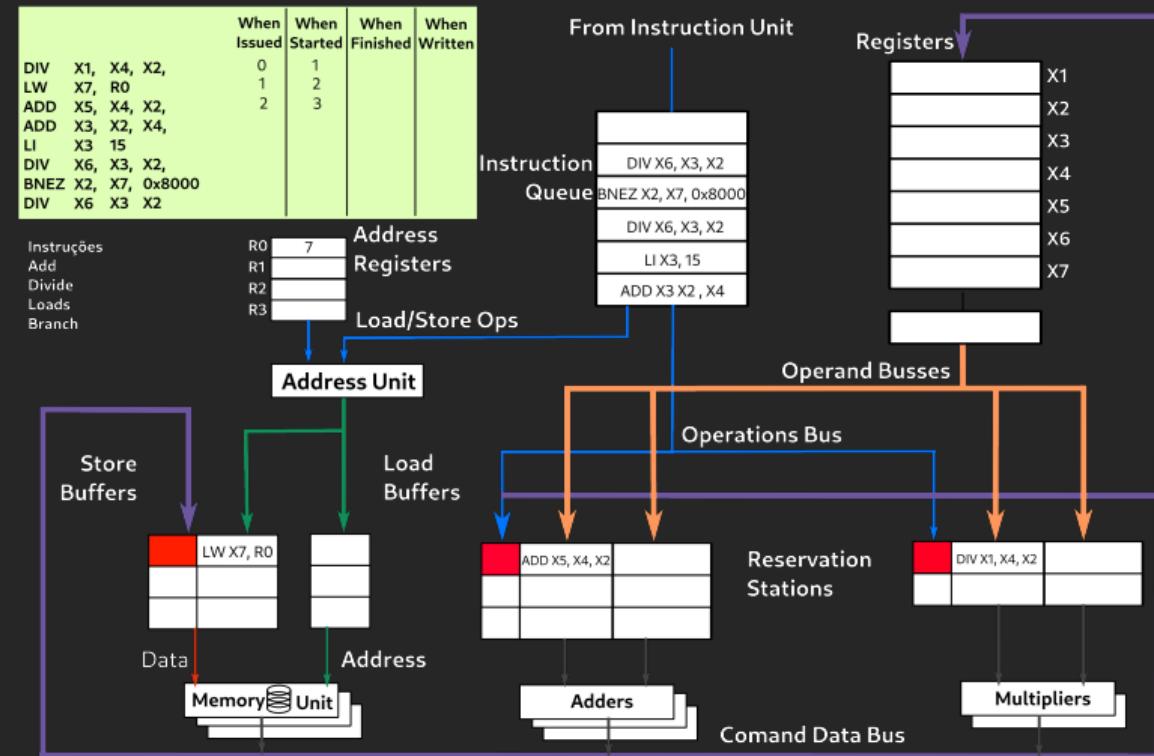
Simulação

Clock cycle: 2



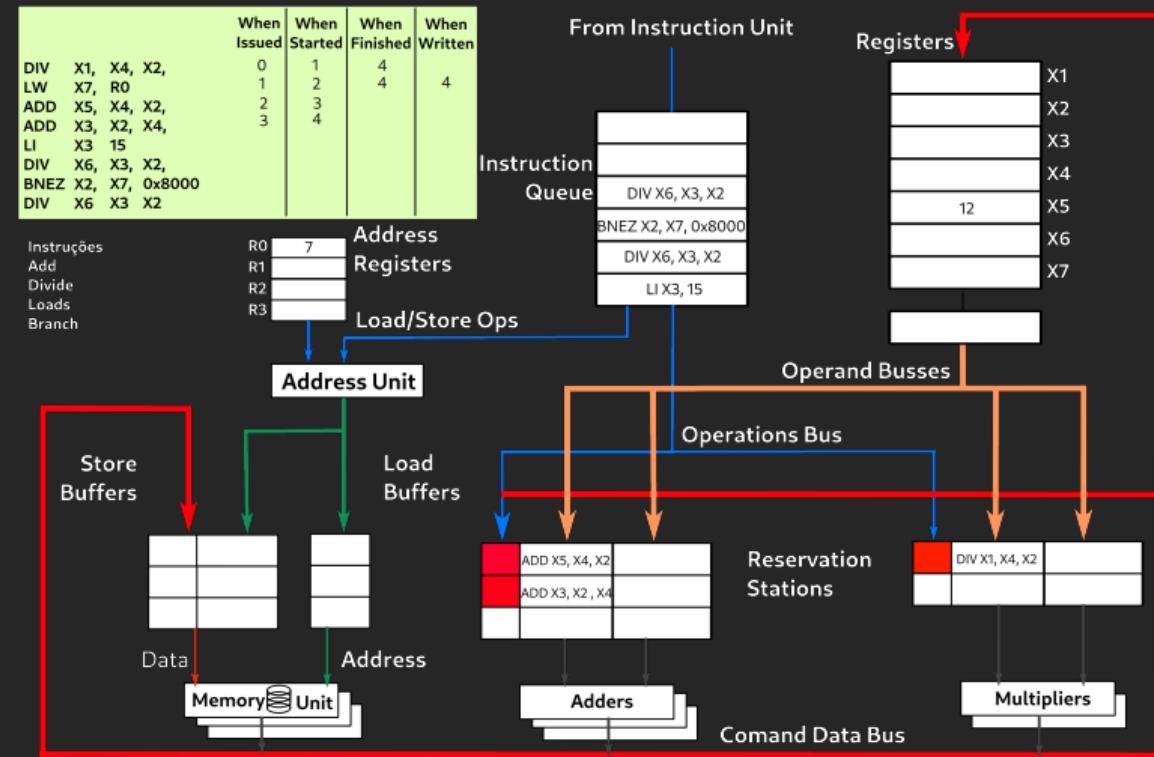
Simulação

Clock cycle: 3



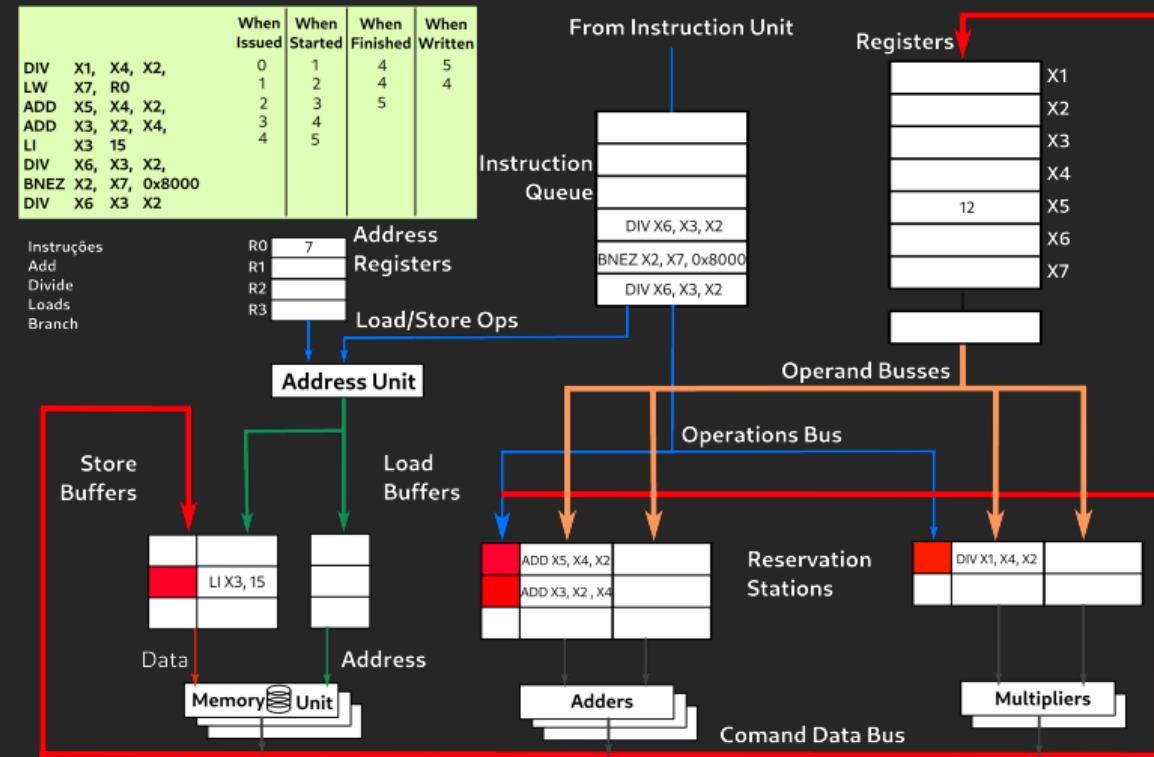
Simulação

Clock cycle: 4



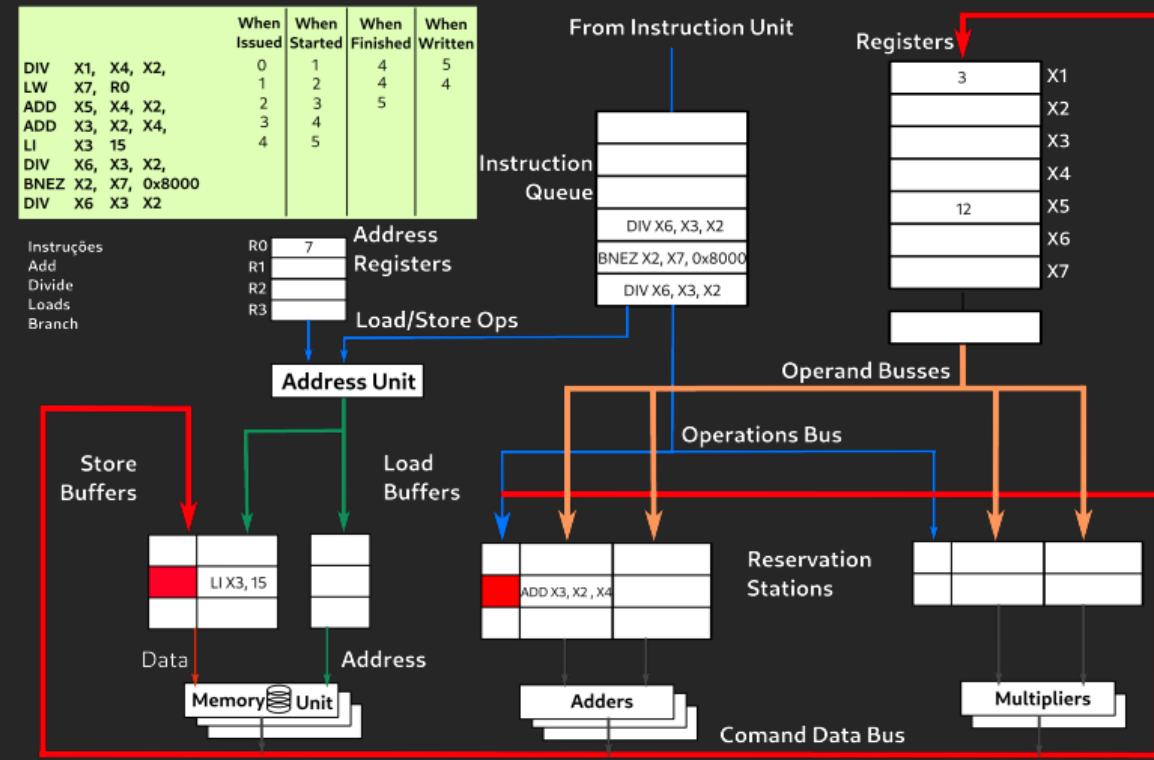
Simulação

Clock cycle: 5



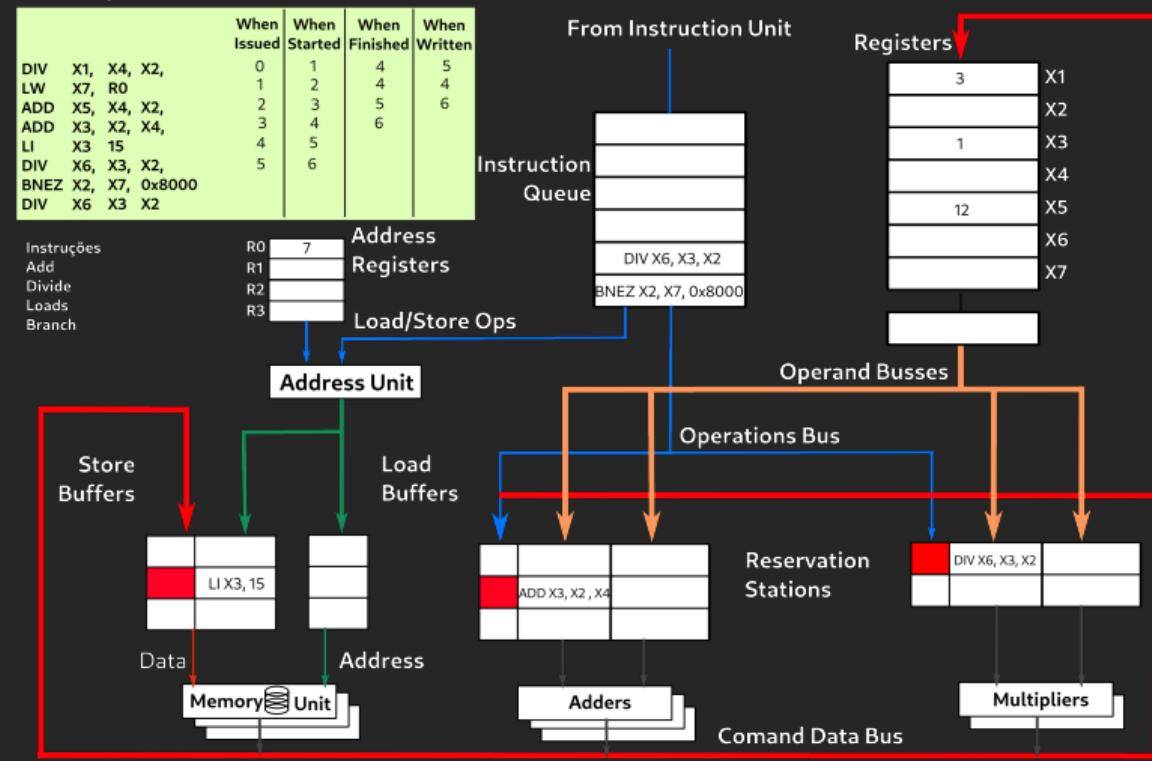
Simulação

Clock cycle: 5



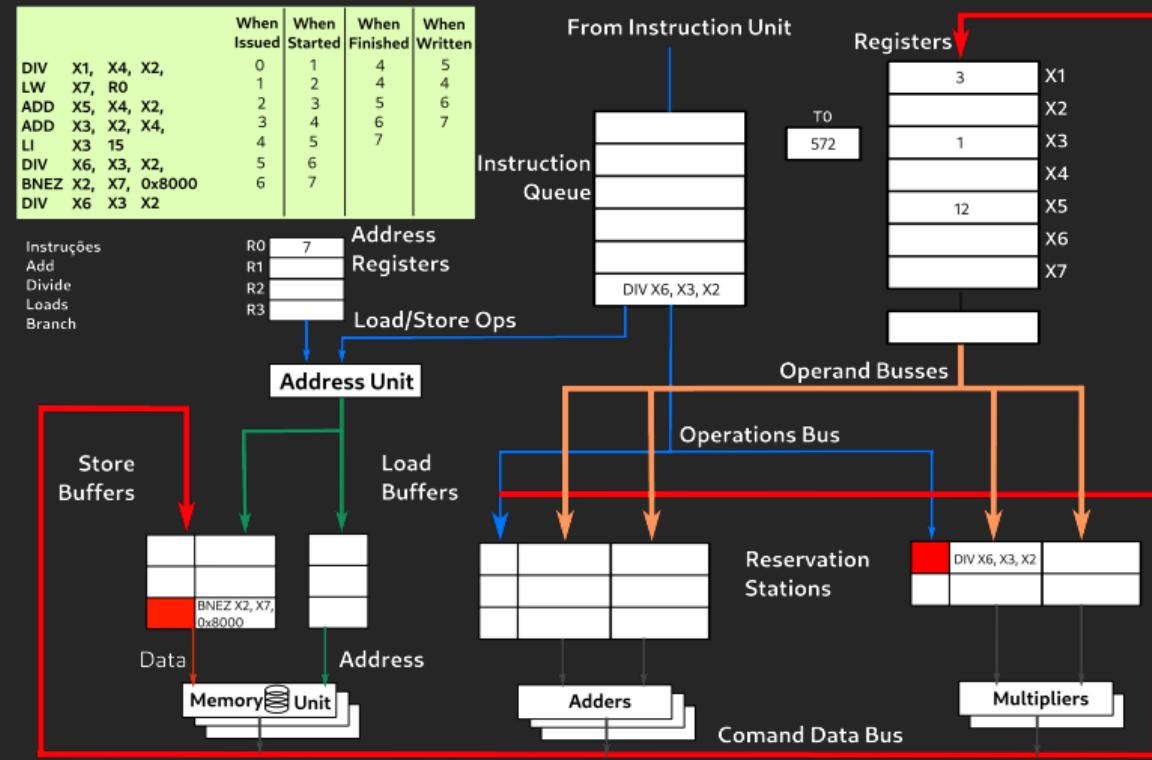
Simulação

Clock cycle: 6



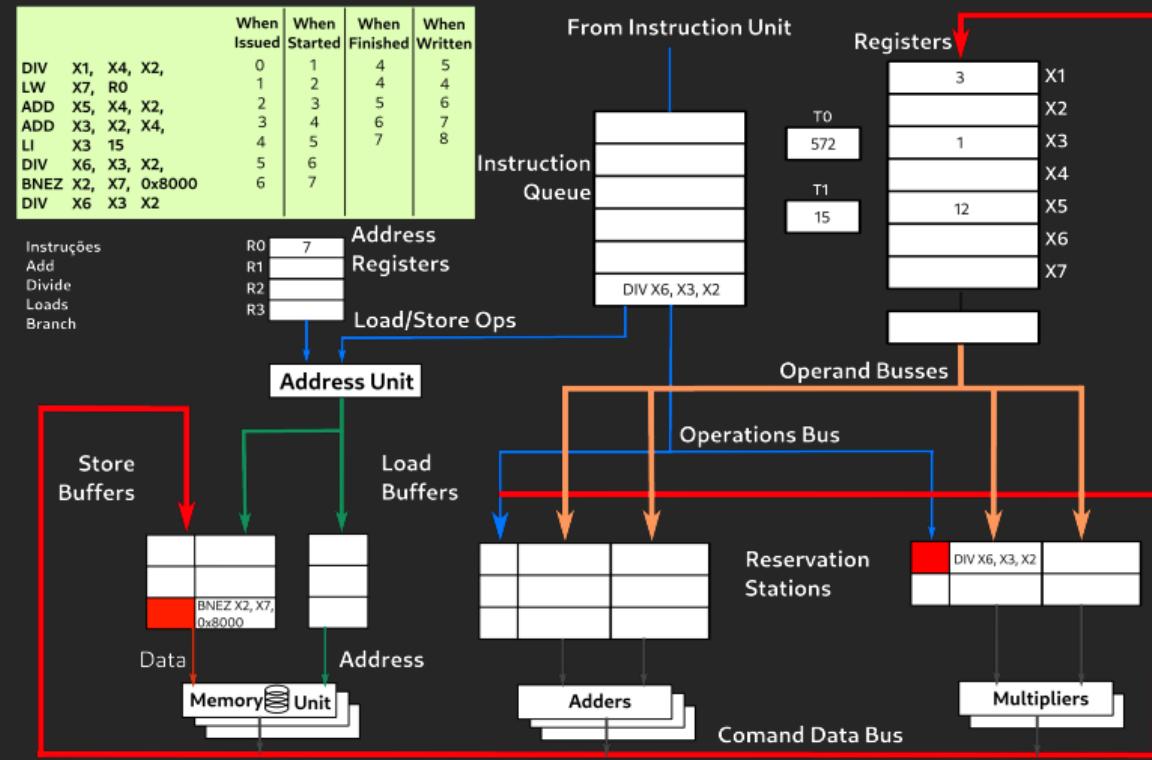
Simulação

Clock cycle: 7



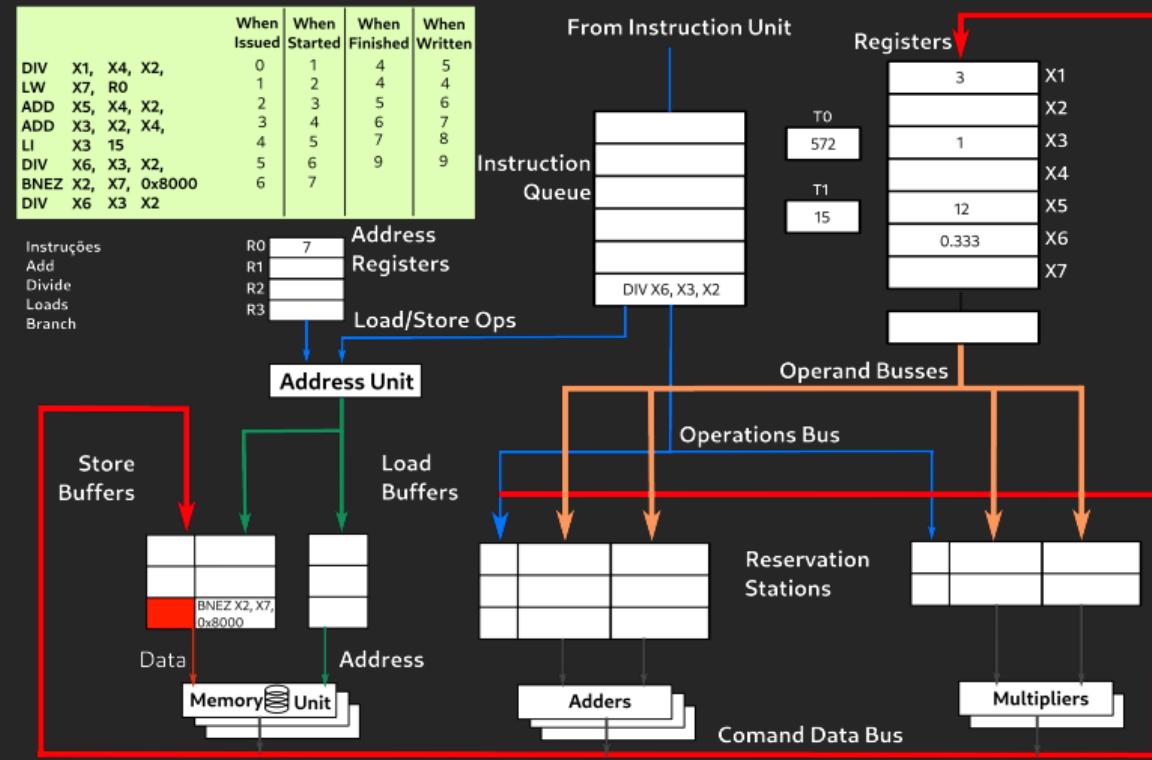
Simulação

Clock cycle: 8



Simulação

Clock cycle: 9



Simulação

Clock cycle: 10

		When Issued	When Started	When Finished	When Written
DIV	X1, X4, X2,	0	1	4	5
LW	X7, R0	1	2	4	4
ADD	X5, X4, X2,	2	3	5	6
ADD	X3, X2, X4,	3	4	6	7
LI	X3 15	4	5	7	8
DIV	X6, X3, X2,	5	6	9	9
BNEZ	X2, X7, 0x8000	6	7	10	
DIV	X6 X3 X2				

