

Algoritmo de Tomasulo

Maio de 2021

| 31 | 20 19 | 15 14 | 12 11 | 7 6 | 0 |
|--------------------|-----------|------------|-----------|-----------|---|
| imm[11:0] | rs1 | funct3 | rd | opcode | |
| 12 offset[11:0] | 5 base | 3 width | 5 dest | 7 LOAD | |

Operações de divisão

| 31 | 25 24 | 20 19 | 15 14 | 12 11 | 7 6 | 0 |
|--------|---------|----------|--------|-------|--------|---|
| funct7 | rs2 | rs1 | funct3 | rd | opcode | |
| 7 | 5 | 5 | 3 | 5 | 7 | |
| MULDIV | divisor | dividend | DIV | dest | OP | |

Integer Register-Immediate Instructions

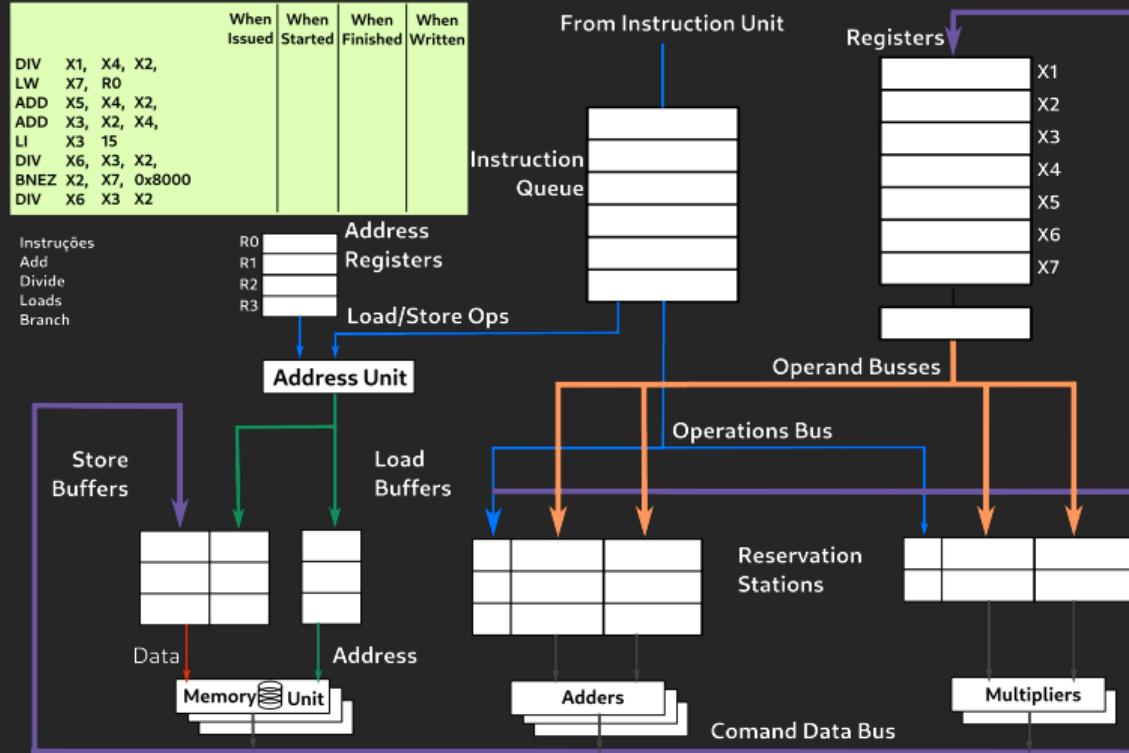
| 31 | 20 19 | 15 14 | 12 11 | 7 6 | 0 |
|-------------------------|----------|-----------|-----------|-------------|---|
| imm[11:0] | rs1 | funct3 | rd | opcode | |
| 12 I-immediate[11:0] | 5 src | 3 ADDI | 5 dest | 7 OP-IMM | |

Integer Register-Immediate Instructions

| 15 | 13 12 | 10 9 | 7 6 | 2 1 | 0 |
|-----------|--------------------|----------|-------------|---------|---|
| funct3 | imm | rs1 | imm | op | |
| 3 BNEZ | 3 offset[8 4:3] | 3 src | 5 offset | 2 CI | |

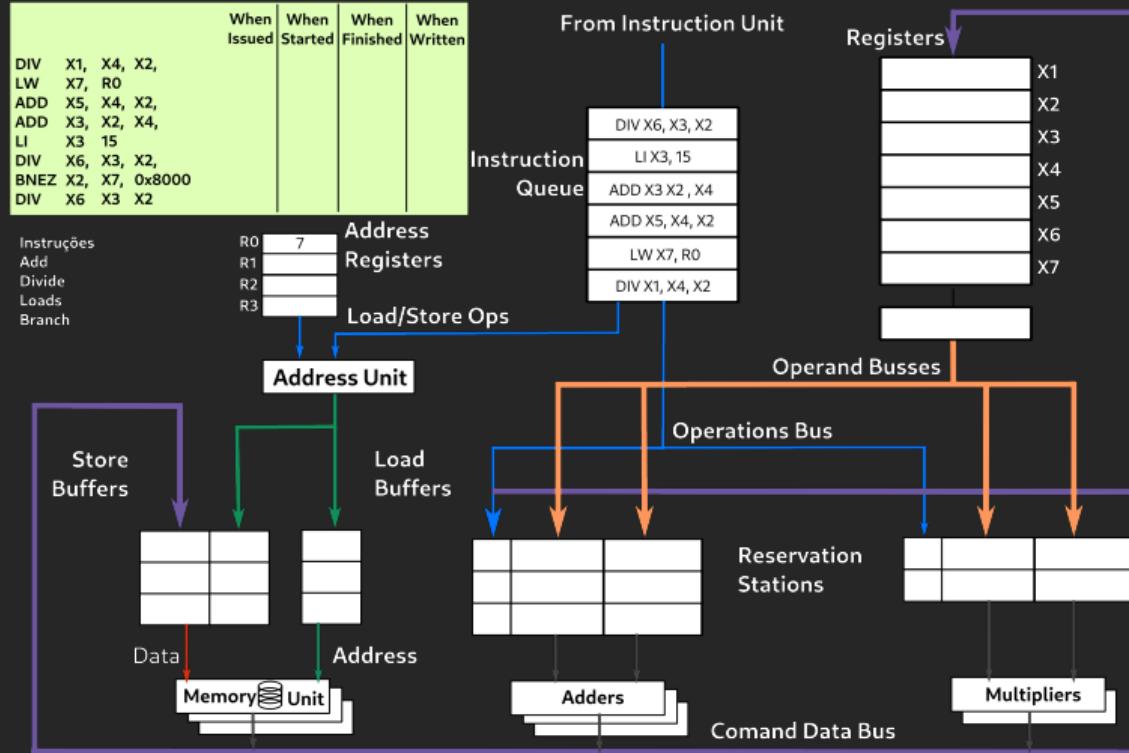
Simulação

Clock cycle: 0



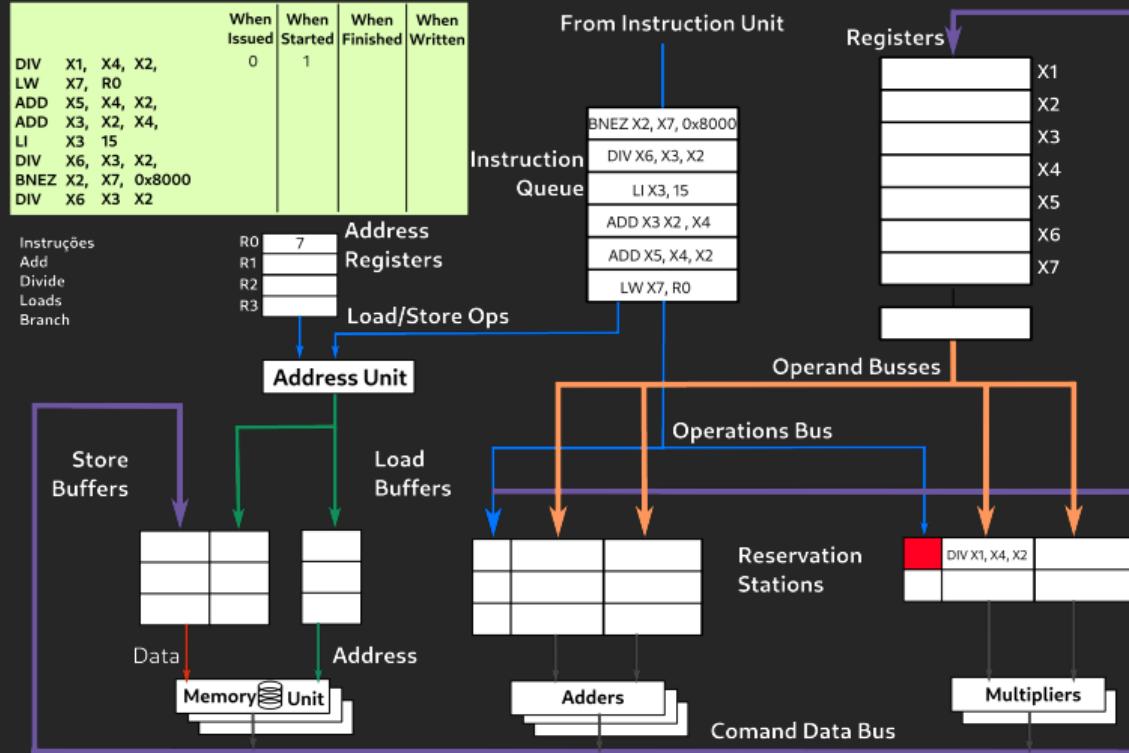
Simulação

Clock cycle: 0



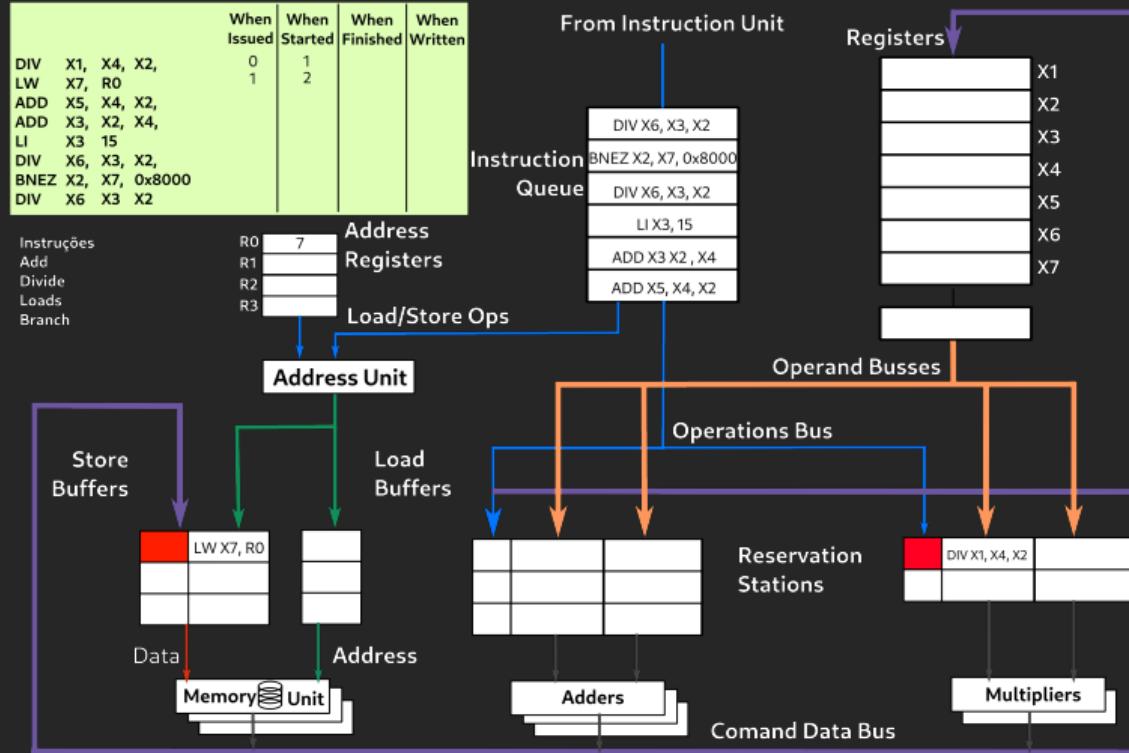
Simulação

Clock cycle: 1



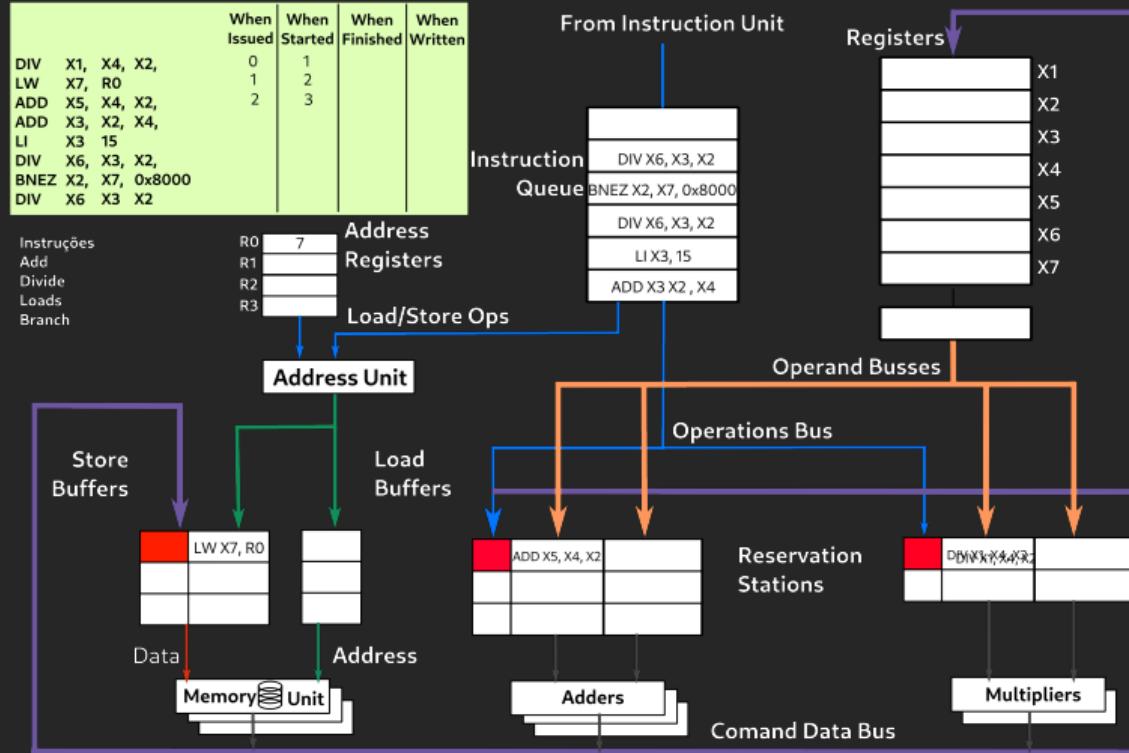
Simulação

Clock cycle: 2



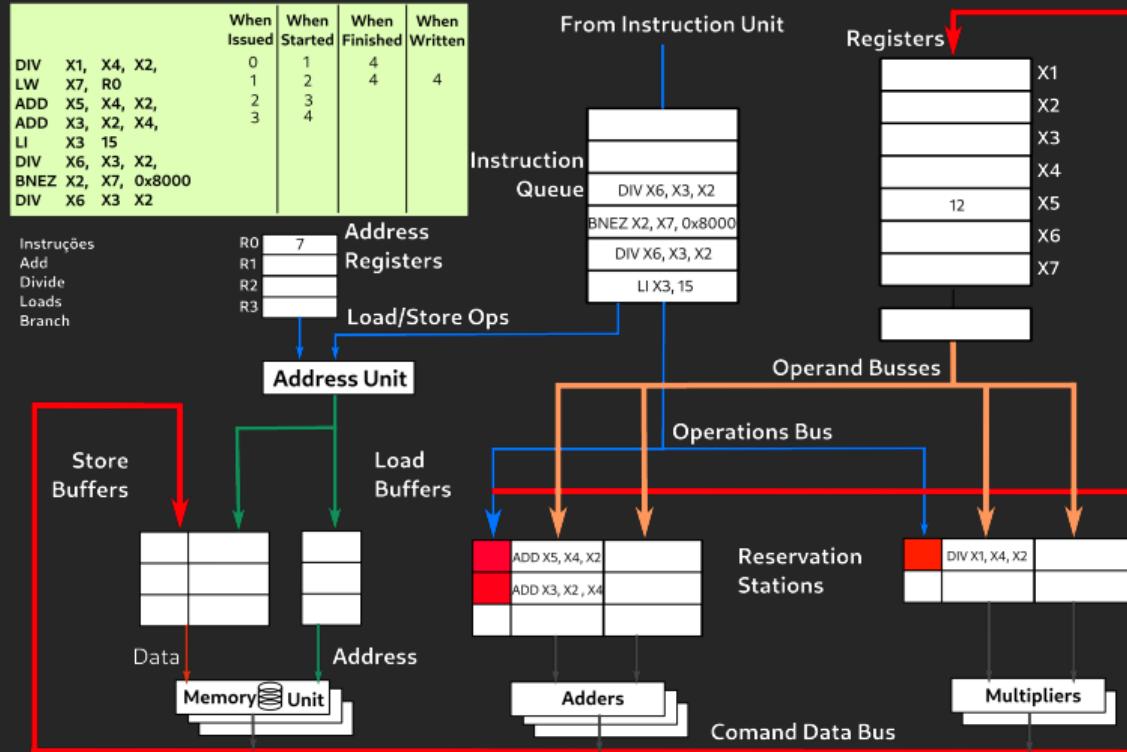
Simulação

Clock cycle: 3



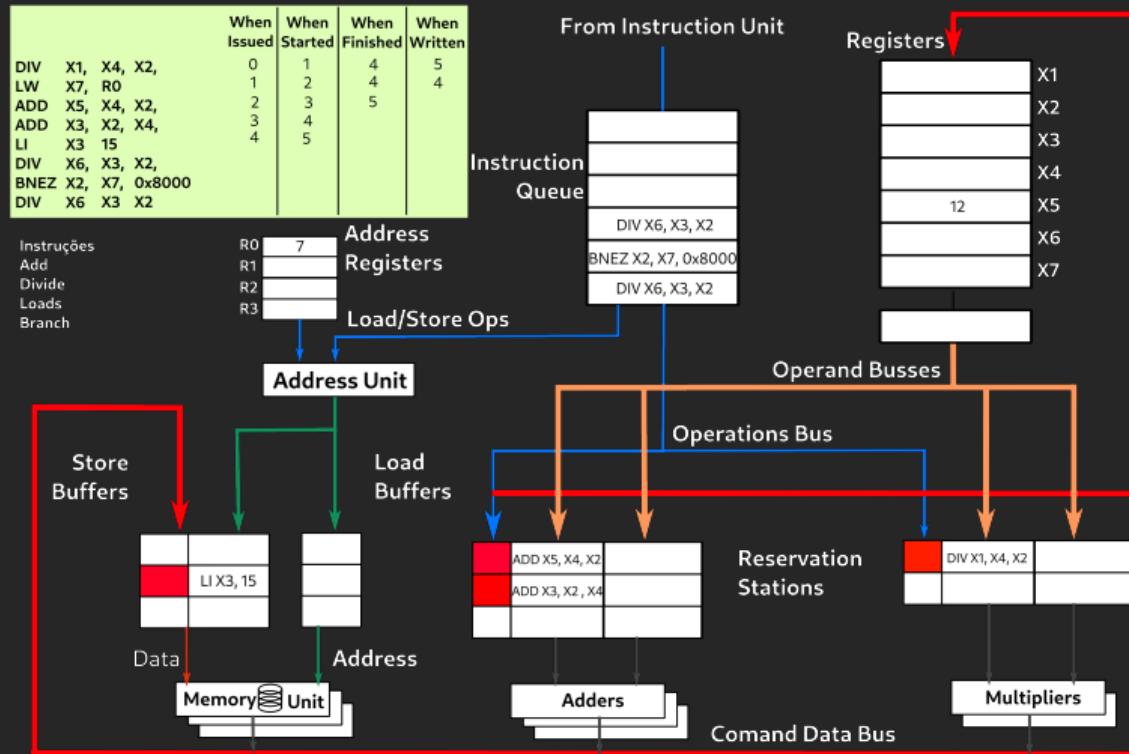
Simulação

Clock cycle: 4



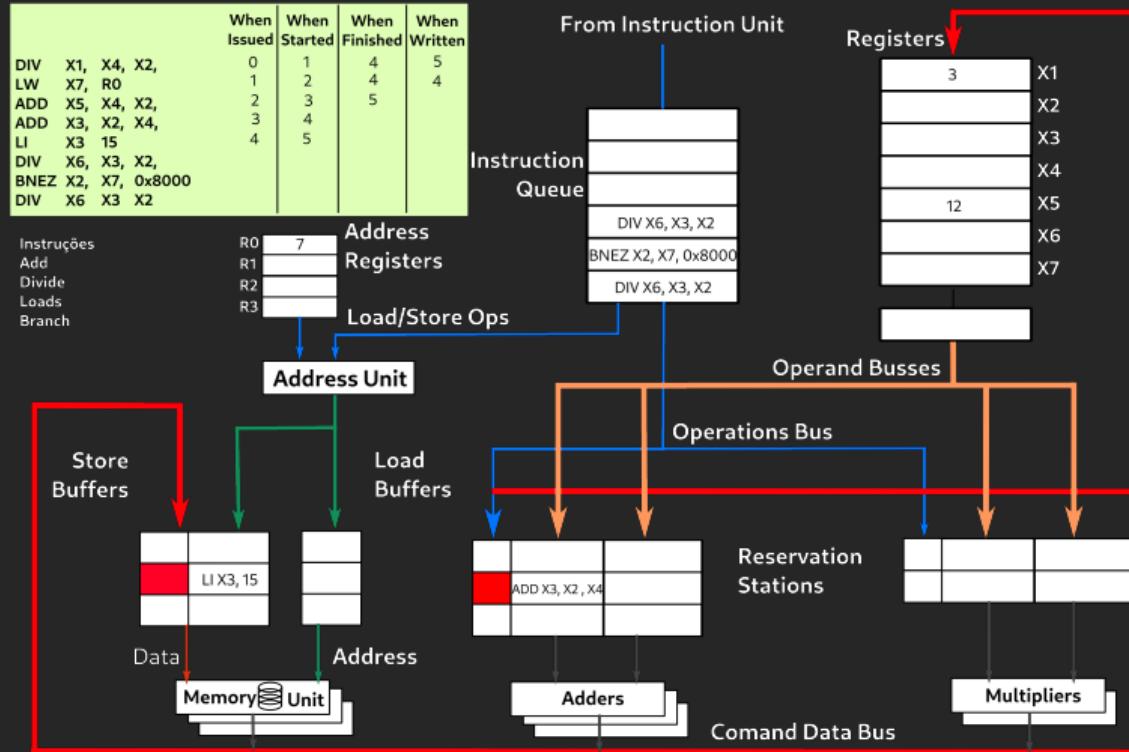
Simulação

Clock cycle: 5



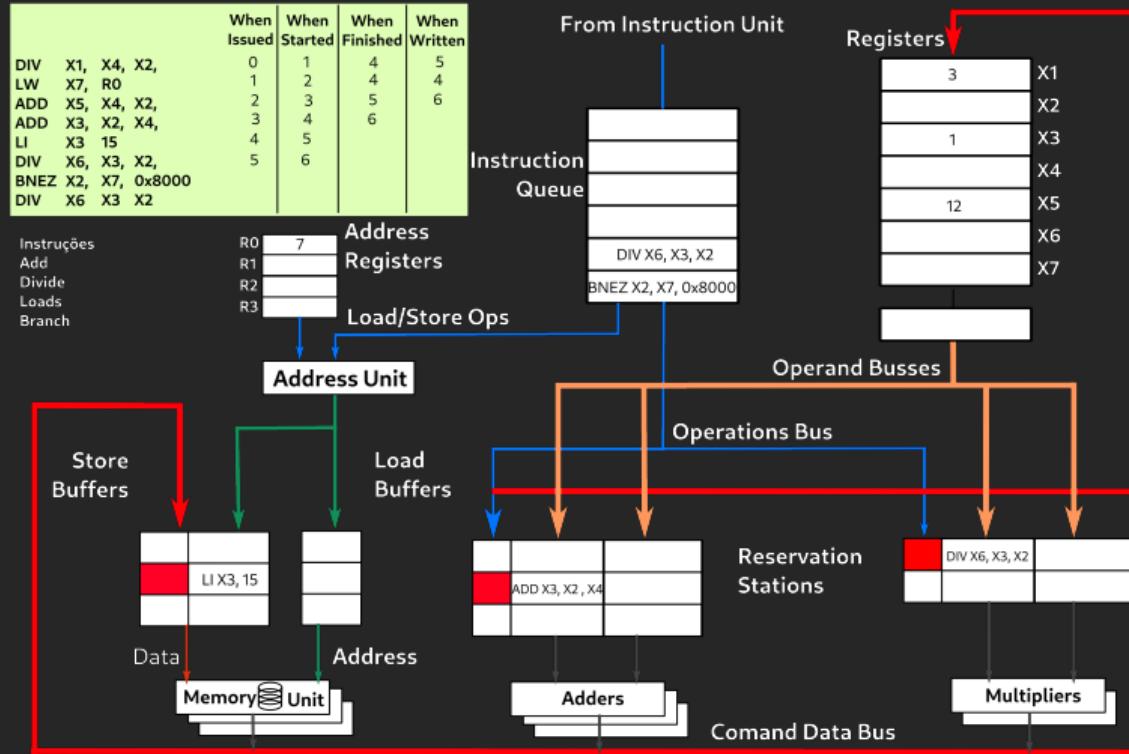
Simulação

Clock cycle: 5



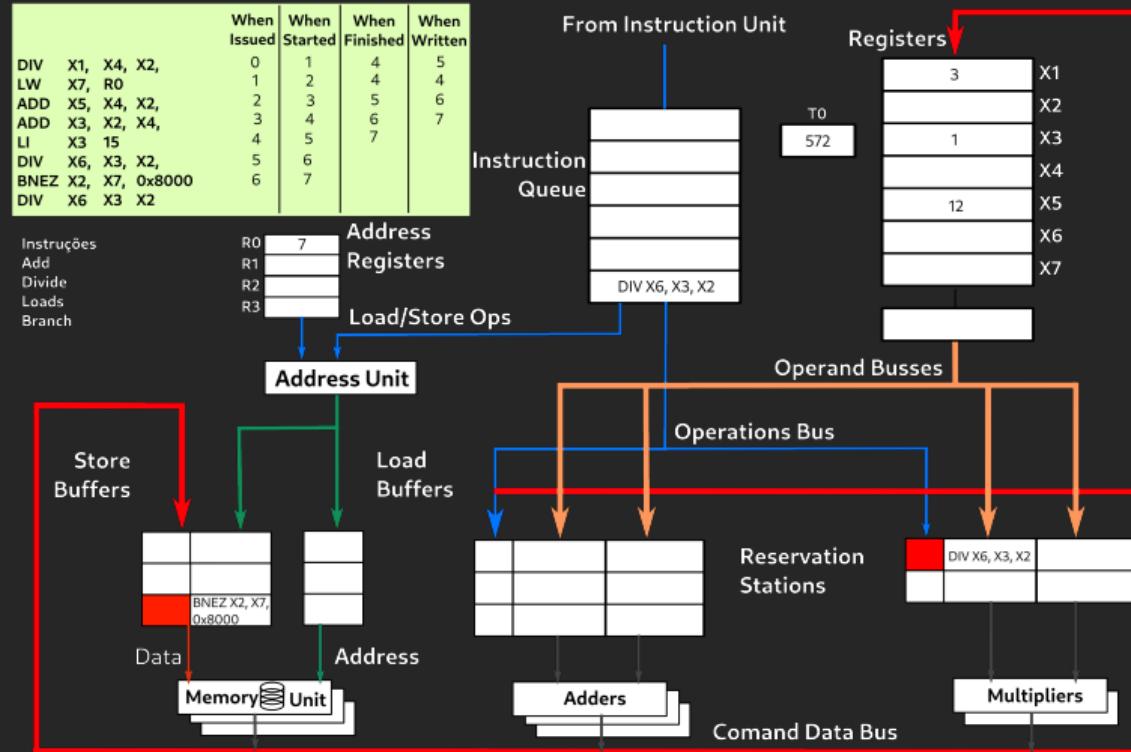
Simulação

Clock cycle: 6



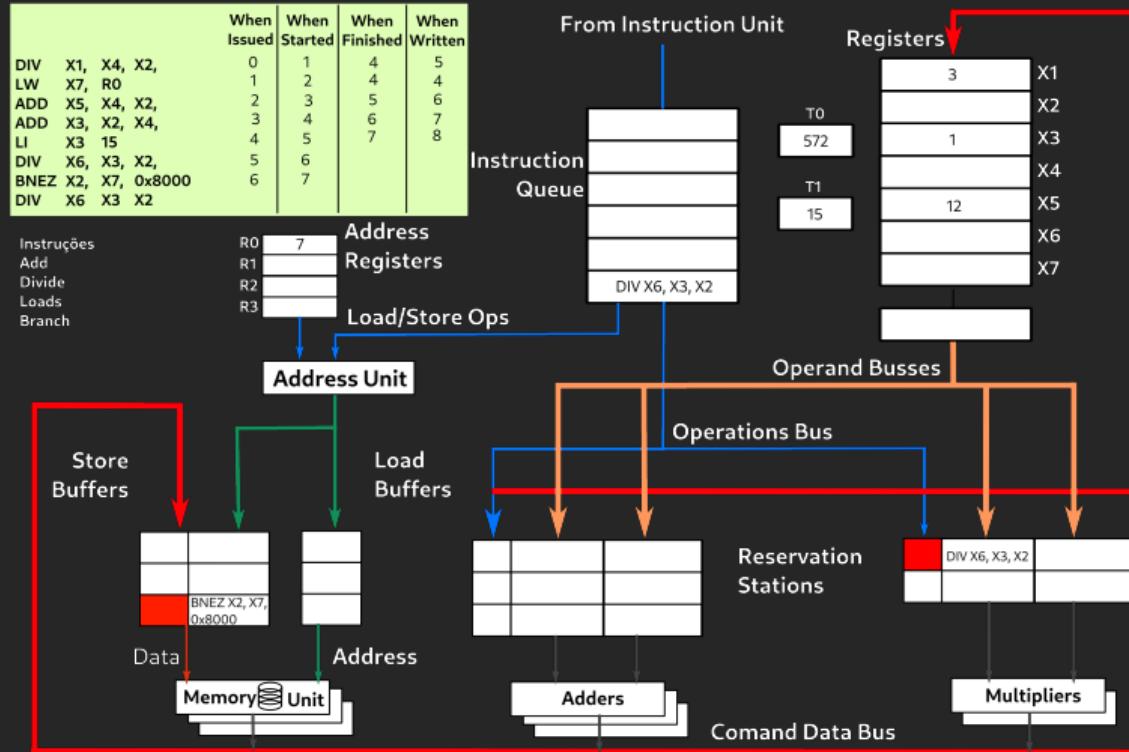
Simulação

Clock cycle: 7



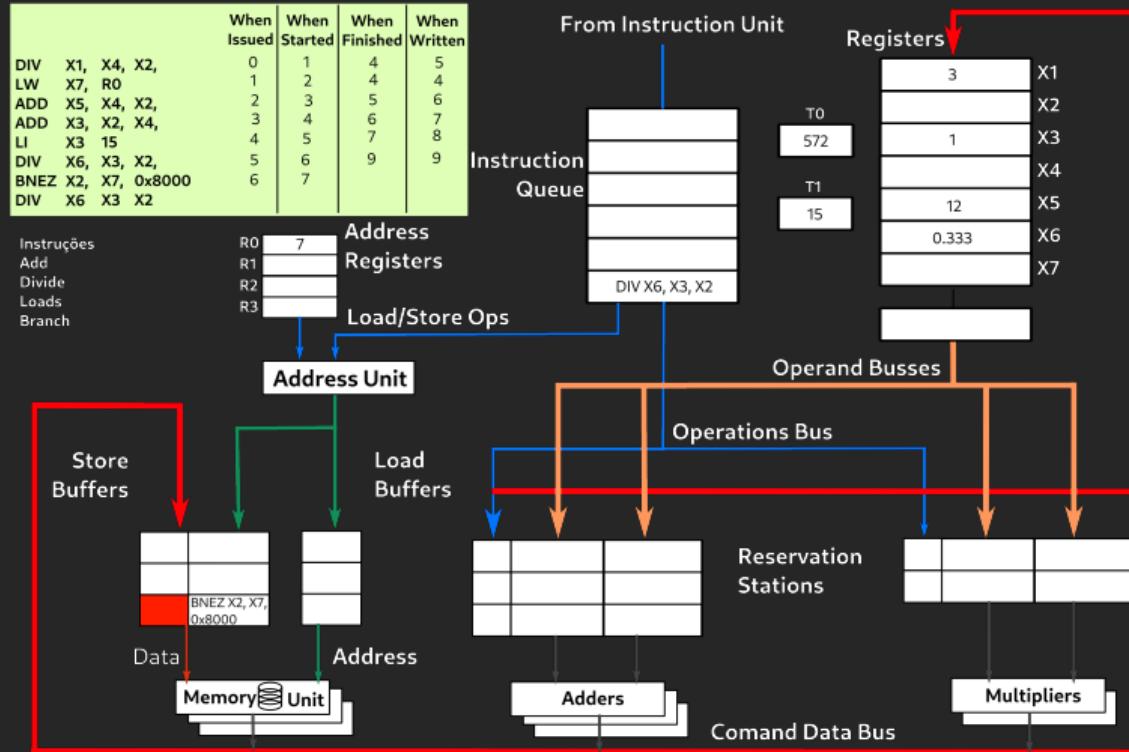
Simulação

Clock cycle: 8



Simulação

Clock cycle: 9



Simulação

Clock cycle: 10

