

Dept. of Computer Engineering 22541 Computer Architecture Spring 2022- Midterm Exam

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Name:	DOINTION	

Student ID: ....

Instructors: Dr. Awos Kanan

Duration: 60 minutes. Date: 8/5/2022

## Instructions:.

- Exam consists of six questions, with total of 30 points.

- Show your work, final answer by itself does not count.

- MIPS Instruction Set Sheet is provided in the last page

- Cell phones not allowed.



Q 1	/5	Q 4	/6
Q2	/6	Q 5	/5
Q3	/4	Q 6	/4

Total Grade:

/30

## **Question 1: Multiple Choice**

(5 points)

- 1. The word size of a 64-bit CPU is:
  - A. One byte.
  - B. Two bytes.
  - C. Four bytes.
- D. Eight bytes.
- 2. The clock rate of a processor that has clock cycle of 0.25ns is:
  - A. 2GHz
  - B. 3GHz
  - C. 4GHz
  - D. 8GHz
- 3. If computer A executes a program in 10 seconds and computer B runs the same program in 15 seconds, how much faster is computer A than computer B
  - A. 1.4 times
  - (B.) 1.5 times
    - C. 5 times
    - D. 0.67 times
- 4. A computer system has 456 instructions. What would be the minimum width of the Opcode field?
  - A. 8 bits
  - B. 10 bits
  - C. 11 bits
  - D.) 9 bits
- 5. In immediate addressing mode, the operand is placed in:
  - A. CPU register
  - B. Instruction
  - C. Memory
  - D. Stack

Question 2: Consider two processors  $P_1$  (Clock Rate = 3 GHz) and  $P_2$  (Clock Rate = 2.5 GHz) that implement the same instruction set with three classes of instructions A, B, and C. The average CPIs are given in the following table: (6 points)

Processor	CPI (Class A)	CPI (Class B)	CPI (Class C)
P1	3	4	2
P2	2	3	. 1

For a given program that has half of its instructions from Class A and the remaining half evenly divided between Class B and Class C:

a) What is the Global CPI for each processor?

(2 points)

$$CPI_{P_1} = 0.5 \times 3 + 0.75 \times 4 + 0.75 \times 2 = 3$$

$$CPI_{P_2} = 0.5 \times 2 + 0.75 \times 3 + 0.75 \times 1 = 2$$

b) Which processor is faster? By how much (factor)?

(2 points)

Which processor is faster? By how much (factor)?

$$CPU T_{ime} (PI) = \frac{IC * 3}{3 * 16 * 9} = IC * 10$$

$$CPU T_{ime} (P2) = \frac{IC * 2}{3 * 16 * 9} = 0.8 IC * 10$$

$$P_{2} is \left(\frac{IC * 10}{08 * * 10 * 10}\right) = \frac{I}{0.8} = 1.25$$
The slower processor so that it

c) By how much (percentage) do we need to increase the clock rate of the slower processor so that it has the same performance as the faster one?

$$0.8 \times 16^9 \text{ IC} = \frac{\text{IC} \times 3}{\text{clock rate new}} \rightarrow \frac{\text{clock rate raw}}{\text{clock rate new}} 3.75 \text{ GHz}$$

need to be increased by  $\left(\frac{3.75-3}{3}\right) = \frac{25\%}{3}$ 

Question 3: Floating-Point operations account for 30% of the execution time of a program on some computer. What is the overall speedup of executing the same program on an enhanced version of this computer that takes 60% less time to execute Floating-Point operations? (4 points)

Question 4: Translate the following C code to RISC-V assembly language. Assume that the variables a, b, and c are already stored in registers X3, X4, and X5 respectively, a and b are positive numbers, subtraction and multiplication instructions are not available.

(6 points)

Exit:

## Question 5: For the following piece of RISC-V assembly code:

(5 points)

Assume that the first instruction is at memory location 0xFFFF000C.

-At what memory address (Hex) is the label "Exit"?

- What is the value (**Decimal**) of the immediate field (Exit) in the **bne** instruction?

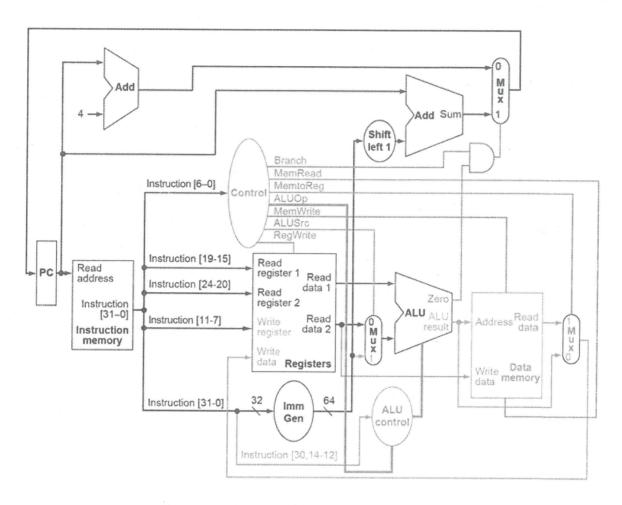
- What is the value (**Decimal**) of the immediate field (L) in the **jal** instruction?

$$-\left(6 \times 2\right) = -12$$

L: sll X2, X3, 2 add X2, X3, X6 ld X3, 0(X5) bne X3, X5, Exit addi X4, X3, 1 add X2, X4, X6 jal X0, L Exit: ...

Question 6: Refer to the RISC-V Datapath below to answer the following questions:

(4 points)



a) What is the main advantage of having a separate ALU Control Unit?

Modular design - can modify it independently of main control unit.

b) What are the two adders (on top of the figure) used for?

-Top Left Adder:

Increment PC to Letch next instruction

-Top Right Adder:

Calculate Branch Target Addrey

c) Complete the table below with the control signals values generated by the Control Unit for addi and sd instructions:

	ALUSrc	RegWrite
addi	. 1	1
sd	1	Ø