DE1-SoC board

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| **Node Name** | **Location** | **I/O Standard** | **Current Strength** | **Description** |
| CLK | PIN\_AF14 | 3.3-V LVTTL | 16mA (default) | 50 MHz clock |
| RST\_n | PIN\_AH17 | 3.3-V LVTTL | 16mA (default) | KYE[1] (low logic level) |
| I\_EN | PIN\_AA14 | 3.3-V LVTTL | 16mA (default) | Enable (KEY[0]) |
| I\_ECHO | PIN\_AJ21 | 3.3-V LVTTL | 16mA (default) | HC-SR04 (Echo) |
| O\_TRIG | PIN\_AG18 | 3.3-V LVTTL | 16mA (default) | HC-SR04 (Trig) |
| O\_HEX[0] | PIN\_AF19 | 3.3-V LVTTL | 16mA (default) | SegA (pin 11) желтый |
| O\_HEX[1] | PIN\_AE18 | 3.3-V LVTTL | 16mA (default) | SegB (pin 7) синий |
| O\_HEX[2] | PIN\_AG20 | 3.3-V LVTTL | 16mA (default) | SegC (pin 4) фиолетовый |
| O\_HEX[3] | PIN\_AF21 | 3.3-V LVTTL | 16mA (default) | SegD (pin 2) белый |
| O\_HEX[4] | PIN\_AG21 | 3.3-V LVTTL | 16mA (default) | SegE (pin 1) серый |
| O\_HEX[5] | PIN\_AF20 | 3.3-V LVTTL | 16mA (default) | SegF (pin 10) зеленый |
| O\_HEX[6] | PIN\_AE19 | 3.3-V LVTTL | 16mA (default) | SegG (pin 5) черный |
| O\_MUX\_HEX[0] | PIN\_AD19 | 3.3-V LVTTL | 16mA (default) | CC (pin 6) |
| O\_MUX\_HEX[1] | PIN\_AH20 | 3.3-V LVTTL | 16mA (default) | CC (pin 8) |
| O\_MUX\_HEX[2] | PIN\_AH19 | 3.3-V LVTTL | 16mA (default) | CC (pin 9) |
| O\_FL | PIN\_V16 | 3.3-V LVTTL | 16mA (default) | LEDR[0] |

Peripherals devises

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| **Connection 2841AD to FPGA**  **(led display common cathode)** | | **Connection HC-SR04 to FPGA** | |
| SegA (pin 11) | R = 150 to FPGA | VCC | DC-5V (from MB-102) |
| SegB (pin 7) | R = 150 to FPGA | Trig | Directly to FPGA |
| SegC (pin 4) | R = 150 to FPGA | Echo | Voltage divider (R1 = 330, R2 = 470) |
| SegD (pin 2) | R = 150 to FPGA | GND | GND (from MB-102) |
| SegE (pin 1) | R = 150 to FPGA |
| SegF (pin 10) | R = 150 to FPGA |
| SegG (pin 5) | R = 150 to FPGA |
| CC (pin 6) | Directly to FPGA |
| CC (pin 8) | Directly to FPGA |
| CC (pin 9) | Directly to FPGA |