

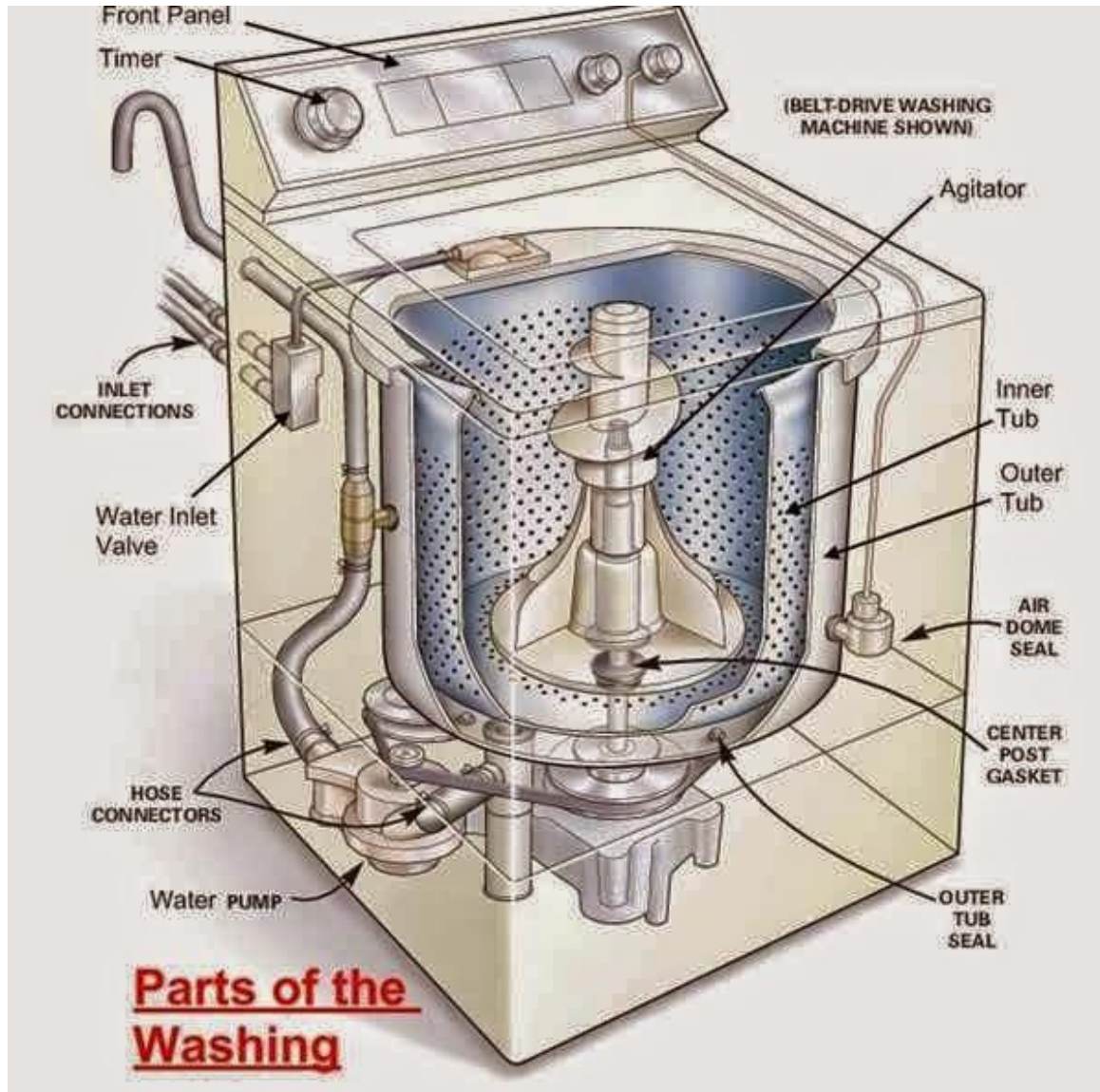
Introduction to Embedded Systems

An abstract digital graphic with a dark blue background. It features glowing blue and red lines that form concentric circles and arcs. In the center, there is a circular pattern with various symbols, including a gear-like shape and some text. A yellow line points from the top right towards the center.

Unit II

Mr. Umesh Koyande

Mr. Kiran Datar



Application-Specific
Embedded Systems

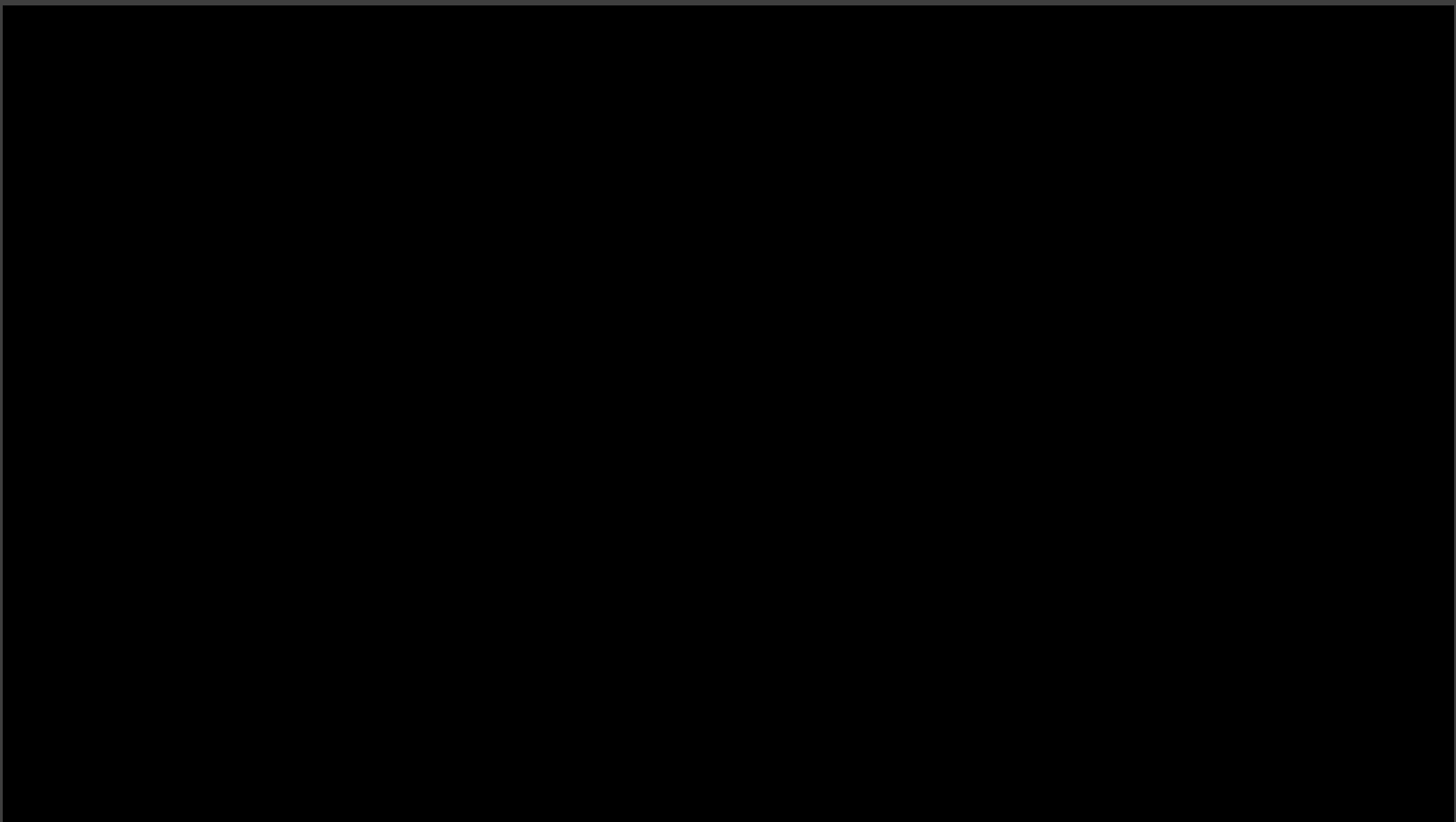




- https://www.youtube.com/watch?v=_EUxskkQjV8&ab_channel=eSpares

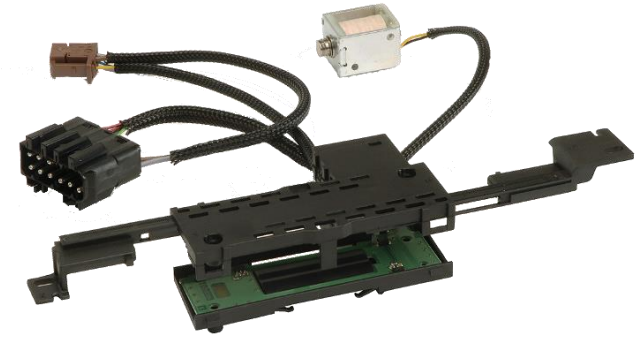


Domain Specific Embedded Systems



https://www.youtube.com/watch?v=oUf9_rS1fYg&ab_channel=tberth

Application And Domain Specific



Electronic Control Units

- High-speed Electronic Control Units (HECUs)
- Low-speed Electronic Control Units (LECUs)



Memory map

- All processors store their programs and data in memory.
- Some cases memory resides on the very same chip, but more often it is located in external memory chips.
- Processor communicates with memory with the address bus and the data bus.
- To read or write a particular location in memory, the processor first writes the desired address onto the address bus.
- Data is then transferred over the data bus.

EPROM (128K)	FFFFFh E0000h
Flash Memory (128K)	C0000h
Unused	72000h
Zilog SCC	70000h
Unused	20000h
SRAM (128K)	00000h

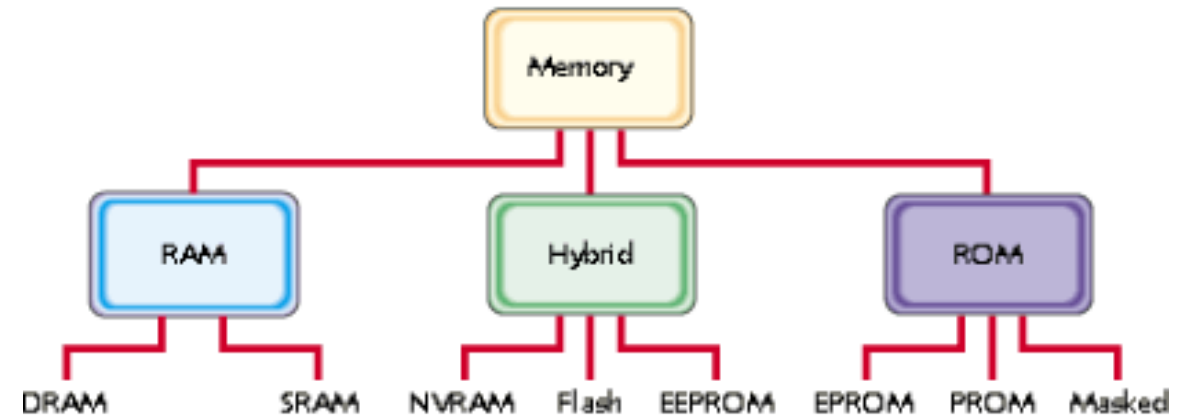
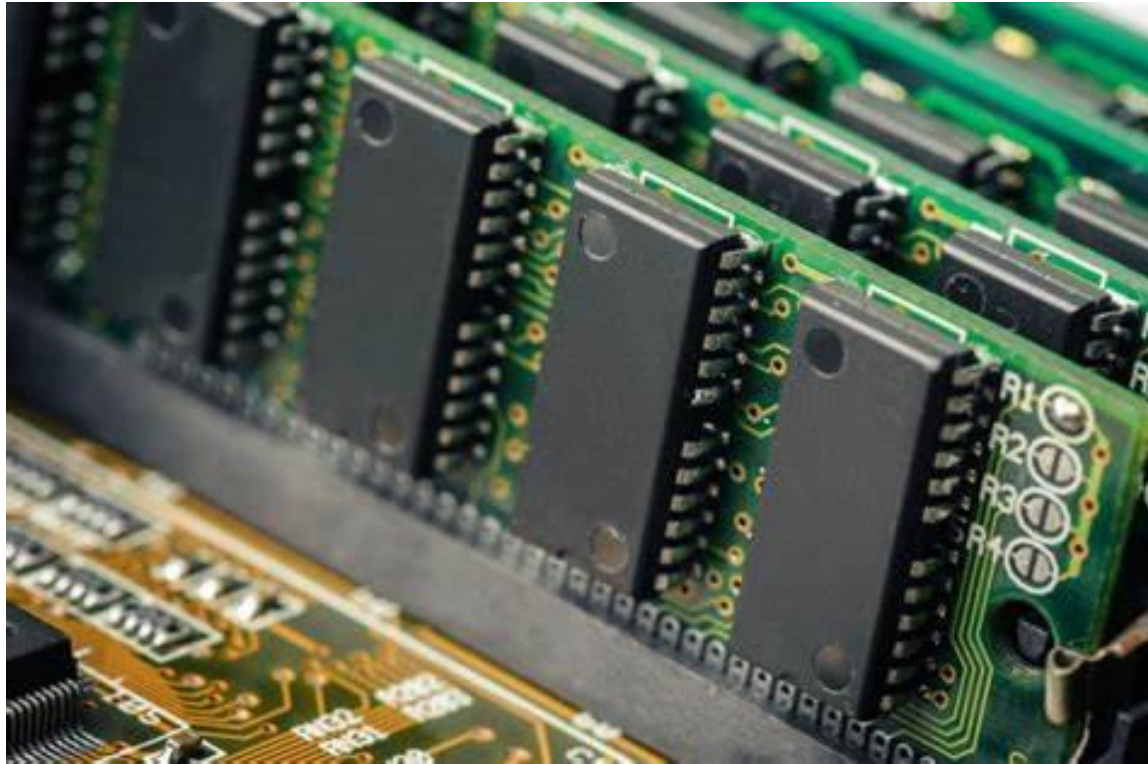
Interrupt map

- Interrupts and associated with each of these are an interrupt pin and an ISR.
- To execute the correct ISR, a mapping must exist between interrupt pins and ISRs.
- Interrupt vector table.
- An interrupt map is a table that contains a list of interrupt types and the devices to which they refer.

ARM Evaluator-7T interrupt vector addresses and their associated interrupt types

Address	Interrupt Type
0x20	reset
0x24	undefined instruction
0x28	SWI (software interrupt)
0x2C	prefetch abort
0x30	data abort
0x34	(reserved for future use)
0x38	IRQ
0x3C	FIQ

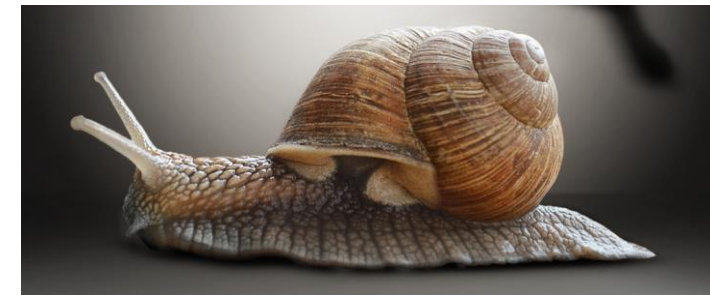
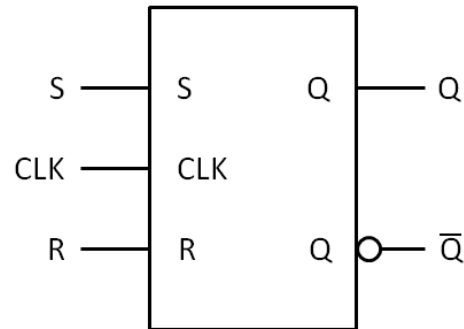
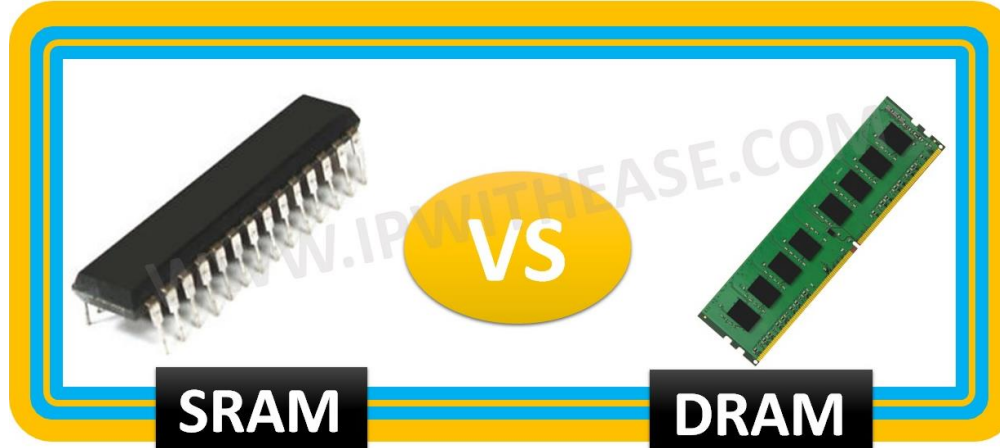
Types of Memory



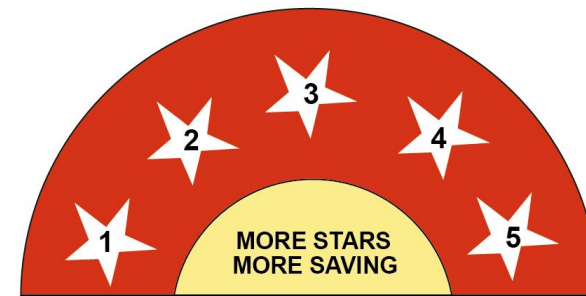


Expensive

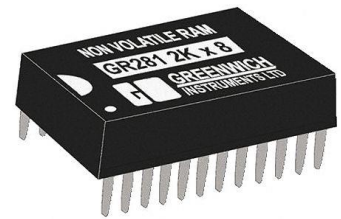
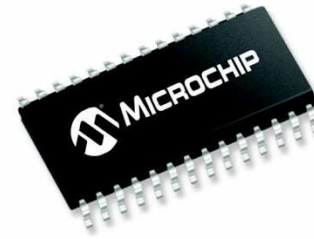
CACHE MEMORY

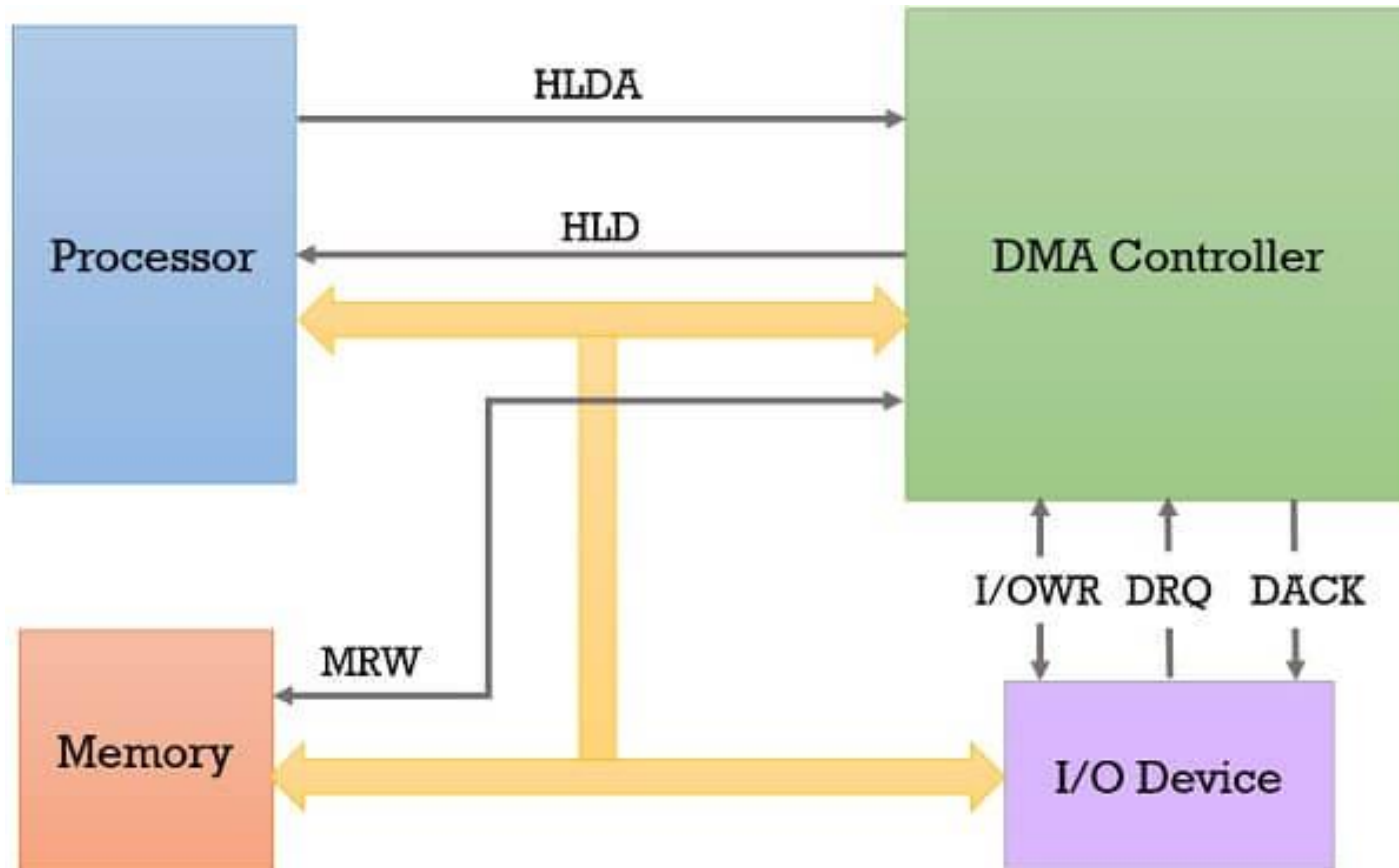


Cheap



Memory Type	Masked ROM	PROM	EPROM	EEPROM	Flash	NVRAM
Description	Preprogrammed	One Time Progamable	Erased using UV light	Electrically Reprogrammable	Electrically Reprogrammable	SRAM with a battery backup
Writeable	No	Once, with programmer	Yes, with programmer	Yes	Yes	Yes
Erase Size	n/a	n/a	Entire chip	Byte	Sector	Byte
Relative Cost	Inexpensive	Moderate	Moderate	Expensive	Moderate	Expensive
Relative Speed	Fast	Fast	Fast	Fast to read, slow to write	Fast to read, slow to write	fast





DMA Controller Data Transfer

Direct Memory Access

- Mode of data transfer between the memory and I/O devices, without the involvement of the processor
- The DMA controller transfers the data in three modes
 - Burst Mode
 - Cycle Stealing Mode
 - Transparent Mode

Direct Memory Access

