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|---|---|
| **Started on** | Friday, 13 May 2022, 10:02 AM |
| **State** | Finished |
| **Completed on** | Friday, 13 May 2022, 11:20 AM |
| **Time taken** | 1 hour 17 mins |
| **Marks** | 37.0/45.0 |
| **Grade** | **16.4** out of 20.0 (**82**%) |

Question **1**

Complete

Mark 1.0 out of 1.0

What is the CACHE address for direct mapped CACHE? the main memory location 31 and no. of CACHE locations are 8.

- a. 5
- b. 8
- c. 6
- d. 7

Question **2**

Complete

Mark 0.0 out of 1.0

To calculate the target address for the branch instruction. Select the correct option

- a. ALU perform the Addition operation and the content of register R1 should not be equal to R2
- b. ALU perform the subtraction operation and the content of register R1 should not be equal to R2
- c. ALU perform the Addition operation and the content of register R1 should be equal to R2
- d. ALU perform the subtraction operation and the content of register R1 should be equal to R2

Question **3**

Complete

Mark 1.0 out of 1.0

The drawback of loop unrolling technique?

- a. All of the mentioned
- b. Occupation of more code space
- c. Register shortfall may happned
- d. Number of instruction increases

Question **4**

Complete

Mark 1.0 out of 1.0

For Unconditional Jump, full 32 bit target address is computed by concatenating?

- a. Bits 00 in the lowest positions
- b. 26 bit immediate field
- c. All of the mentioned
- d. Upper 4 bits of PC

Question **5**

Complete

Mark 1.0 out of 1.0

When both integer are +ve i.e. (+ve) x (+ve) = (+ve) and Multiply 7 with 3 and register size is 4 bit. Choose the correct option?

- a. 3 Cycles are required to complete the multiplication
- b. 7 Cycles are required to complete the multiplication
- c. 5 Cycles are required to complete the multiplication
- d. 4 Cycles are required to complete the multiplication

Question **6**

Complete

Mark 1.0 out of 1.0

Name the type of hazard presented in the following two sequential instructions:

```
add t2, t1, t0
sub t4, t3, t2
```

- a. Read After Write (RAW)
- b. Read After Read (RAR)
- c. Write After Write (WAW)
- d. Write After Read (WAR)

Question **7**

Complete

Mark 1.0 out of 1.0

**The bit used to signify that the cache location is updated is _____**

- a. **Valid bit**
- b. **Dirty bit**
- c. **Reference bit**
- d. **Update bit**

Question **8**

Complete

Mark 1.0 out of 1.0

To Implements the following instructions, the instruction format is 6-bit opcode, 5-bit t1, 5-bit t2 and 16-bit for constant field value, to calculate the effective address at 3rd clock cycle of pipeline. select the right option.

lw $t1, offset_value($t2)

sw $t1, offset_value($t2)

- a. 16-bit constant field & must be sign extended to 32 bits
- b. 16-bit constant field & must be sign extended to 16 bits
- c. 16-bit constant field & must be sign extended to 28 bits
- d. 16-bit constant field & must be sign extended to 64 bits

Question **9**

Complete

Mark 1.0 out of 1.0

In pipeline instructions are executed in ?

- a. Parallel manner
- b. Bidirectional manner
- c. Serial manner
- d. Overlapping manner

Question **10**

Complete

Mark 1.0 out of 1.0

**The concept of Virtual memory used to _____**

a. **Allow the program to have more space than the main memory**

b. **All of the mentioned**

c. **Allow multiple programs**

d. **Provide protection**

Question **11**

Complete

Mark 1.0 out of 1.0

The instruction pipeline of a RISC processor has the following stages: Instruction Fetch (IF), Instruction Decode (ID),Operand Fetch (OF), Perform Operation(PO)and Writeback(WB).The IF,ID,OF and WB stages take 1 clock cycle each for every instruction. Consider a sequence of 100 instructions. In the PO stage, 40 instructions take 33 clock cycles each, 35 instructions take 22 clock cycles each, and the remaining 25 instructions take 11 clock cycles each. Assume that there are no data hazards and no control hazards.How many clock cycles are required for completion of execution of the sequence.

a. 221

b. 218

c. 219

d. 220

Question **12**

Complete

Mark 1.0 out of 1.0

**Consider the following code:**

**CODE:**

**Load R1,Loc1; Load R1 from memory location Loc1**

**Load R2,Loc2; Load R2 from memory location Loc2**

**Add R1,R2,R1; Add R1 and R2 and save result in R1**

**Dec R2; Decrement R2**

**Dec R1; Decrement R1**

**Mpy R1,R2,R3; Multiply R1 and R2 and store in R3**

**Store R3, Loc3; Store r3 in Memory Location Loc3**

**What is the number of cycles needed to execute the above code assuming each instruction takes one cycle to execute?**

- a. 10
- b. 8
- c. 9
- d. 11

Question **13**

Complete

Mark 0.0 out of 1.0

**Direct mapping is used for 32 Byte Main memory and 4 Byte Cache memory, How many bits are required for a TAG field?**

- a. 3
- b. 8
- c. 4
- d. 2

Question **14**

Complete

Mark 1.0 out of 1.0

The two numbers given below are multiplied using Booth's algorithm.

Multiplicand : 0101 1010 1110 1110

Multiplier: 0111 0111 1011 1101

How many additions/Subtractions are required for ?

a. **4 subtractions and 3 additions**

b. **4 subtractions and 4 additions**

c. **3 subtractions and 3 additions**

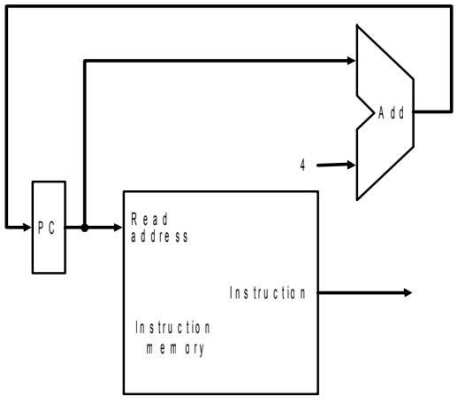
d. **3 subtractions and 4 additions**

Question **15**

Complete

Mark 1.0 out of 1.0

In the figure shown below, at the adder 4 can be replaced with ?




a. 3

b. 5

c. 2

d. 7

Question **16**

Complete

Mark 1.0 out of 1.0

**Code:**

**DIV.D F0,F2,F4**

**ADD.D F6,F0,F8**

**S.D F6,0(R1)**

**SUB.D F8,F10,F14**

**MUL.D F6,F10,F8**

**How many name-dependencies are available in the given code?**

a. 3

b. 4

c. 1

d. 4

Question **17**

Complete

Mark 1.0 out of 1.0

A four-stage pipeline has stage delays of 150, 120, 160, and 140 ns respectively. Registers are used between the stages and have a delay of 10 ns each. What is the cycle time?

a. 165 ns

b. 175 ns

c. 170 ns

d. 160ns

Question **18**

Complete

Mark 1.0 out of 1.0

In which architecture can the number of operands be three?

a. **accumulator**

b. **register-register**

c. **register-memory**

d. **stack**

Question **19**

Complete

Mark 1.0 out of 1.0

For the Software Pipelining, select the correct option.

a. Occupy no code space than loop unrolling

b. Occupy more code space than loop unrolling

c. Occupy less code space than loop unrolling

d. None of the mentioned

Question **20**

Complete

Mark 1.0 out of 1.0

For the CACHE miss. Choose the right option?

a. **All of the mentioned**

b. **The number of times CPU do not get data from CACHE**

c. **MISS penalty time is measured in terms of time taken to replace the new block in CACHE from main memory**

d. **CACHE MISS is also known as MISS penalty time**

Question **21**

Complete

Mark 1.0 out of 1.0

In pipeline processor, which hazard degrade the performance of the pipeline?

- a. WAR
- b. WAW
- c. RAR
- d. RAW

Question **22**

Complete

Mark 1.0 out of 1.0

A half adder is implemented with XOR and AND gates. A full adder is implemented with two half adders and one OR gate. The propagation delay of an XOR gate is twice that of an AND/OR gate. The propagation delay of an AND/OR gate is 1.2 microseconds. A 4-bit ripple-carry binary adder is implemented by using full adders. Find the total propagation time of this 4-bit binary adder in microseconds.

- a. 19.1 ms
- b. 19.4 ms
- c. 19.8 ms
- d. 19.2 ms

Question **23**

Complete

Mark 1.0 out of 1.0

For Translation Lookaside Buffer. Select the right option?

- a. It is a special address translation cache
- b. Used for to reduce the no. of memory read cycles
- c. Used for speedup the process
- d. All of the mentioned

Question **24**

Complete

Mark 1.0 out of 1.0

For the code given below choose the wrong answer.

MIPS Code:

1. ADD r1, r2, r3
2. SUB r4, r1, r5
3. AND r6, r1, r7
4. OR r8, r1, r9
5. XOR r10, r1, r11

- a. Direct data dependence is there
- b. Using split phase of the clock, data hazard can be eliminated from instruction no. fifth
- c. Using split phase of the clock, data hazard can be eliminated from instruction no. fourth
- d. Using split phase of the clock, data hazard can be eliminated from instruction no. second

Question **25**

Complete

Mark 1.0 out of 1.0

What is true for virtual memory?

- a. Processor sends virtual address for page table
- b. Processor sends physical address for page table
- c. Processor sends virtual address for main memory
- d. Processor sends physical address for main memory

Question **26**

Complete

Mark 0.0 out of 1.0

For the given code ( MIPS processor), the total number of stalls required ?

Original code:

```
L.D      F0, 0(R1)
ADD.D    F4,F0,F2
S.D      F4, 0(R1)
DADDUI R1,R1, #-8
BNE      R1,R2,Loop
```

- a. 3
- b. 2
- c. 4
- d. 5

Question **27**

Complete

Mark 1.0 out of 1.0

For 0 0 0 1 0 1 1 1 1 what is the arithmetic shift write operation?

- a. 0 1 1 0 1 1 1 1 1
- b. 0 1 1 0 1 1 1 1 0
- c. 0 1 1 0 1 1 1 0 1
- d. 0 1 1 0 1 1 0 1 1

Question **28**

Complete

Mark 1.0 out of 1.0

Computer architecture course is offered to study of ?

- a. Processor ISA
- b. Processor DPA
- c. All of the mentioned
- d. Processor hardware

Question **29**

Complete

Mark 1.0 out of 1.0

For A= 0 0 1 0 1 0 1 0 0 what will be arithmetic shift right ?

- a. A= 0 1 1 1 0 1 0 1 0
- b. A= 0 0 0 1 0 1 0 1 0
- c. A= 1 1 1 1 0 1 0 1 1
- d. A= 0 0 0 1 0 1 0 0 0

Question **30**

Complete

Mark 1.0 out of 1.0

Consider a pipeline having 4 phases with their execution delays in ns i.e. IF (60), ID(50), IE(80) and WB(75).The clock duration is calculated based on ?

- a. WB(75ns)
- b. IE(80ns)
- c. IF (60ns)
- d. ID(50ns)

Question **31**

Complete

Mark 0.0 out of 1.0

For the assembly code given below, the number of clock cycles required to execute by 5- stage pipeline are ?

Code:

```
LD  R1, 16(R5)
SW  R3, 0(R7)
```

- a. 4 and 5
- b. 5 and 5
- c. 4 and 4
- d. 5 and 4

Question **32**

Complete

Mark 1.0 out of 1.0

The number of register available in MIPS architecture are?

- a. 8
- b. 32
- c. 28
- d. 16

Question **33**

Complete

Mark 1.0 out of 1.0

What is the output of t5 after execution of the following MIPS assembly program by instruction-level parallelism? Consider the initial content of t0 = 1,t2 = 5 and t2 = 10.

or t0, t1, t2

xor t1, t2, t0

and t2, t1, t0

or t5, t2, t0

- a. 14
- b. 10
- c. 9
- d. 15

Question **34**

Complete

Mark 1.0 out of 1.0

For 0 1 0 1 1 1 1 0 1 what is shift right operation output?

- a. 0 0 1 0 1 1 0 0 0
- b. 0 0 1 0 1 1 1 0 0
- c. 0 0 1 0 1 1 1 1 1
- d. 0 0 1 0 1 1 1 1 0

Question **35**

Complete

Mark 0.0 out of 1.0

If page fault occur?

- a. It is handled by I/O
- b. It is handled by hardware (Processor)
- c. None of the mentioned
- d. It is handled by software (OS)

Question **36**

Complete

Mark 0.0 out of 1.0

if we run the following program on the pipeline to execute it. Select the correct option.

Program:

```
start: ADD R2, R0, R1
       stall
       ADD R4, R2, R3
       stall
       stall
.end start
```

- a. Three stalls are required between first ADD instruction and second ADD instruction
- b. Two stalls are required between first ADD instruction and second ADD instruction
- c. one stalls is required between first ADD instruction and second ADD instruction
- d. Noe of the mentioned.

Question **37**

Complete

Mark 1.0 out of 1.0

For the given code ( MIPS processor), the total number of stalls required with loop unrolling 5 copies along with scheduling implementation?

Original code:

```
L.D      F0, 0(R1)
ADD.D    F4,F0,F2
S.D      F4, 0(R1)
DADDUI R1,R1, #-8
BNE      R1,R2,Loop
```

- a. 1
- b. 2
- c. 3
- d. 0

Question **38**

Complete

Mark 0.0 out of 1.0

How many nop (no operation) instruction need to be inserted between the two instructions given below in order to avoid data hazard:

```
lw t1, 4(t0)
add t2, t1, t0
```

- a. 2
- b. 3
- c. 1
- d. 4

Question **39**

Complete

Mark 1.0 out of 1.0

In pipeline, spilt phase concept is used for a clock cycle?

- a. Forward only
- b. None of the mentioned
- c. In first half of clock write back and second half forwarding
- d. Write back only

Question **40**

Complete

Mark 1.0 out of 1.0

For single instruction execution?

- a. Non-pipeline processor is  good
- b. Both pipeline and non-pipeline are good
- c. Pipeline processor is good
- d. None of the mentioned

Question **41**

Complete

Mark 1.0 out of 1.0

Consider the unpipelined machine with 10ns clock cycles. It uses four cycles for ALU operations and branches where as five cycles for memory operations. Assume that the relative frequencies of these operations are 40%,20% and 40% respectively. Let due to clock skew and set up pipelining, the machine adds 1 ns of overhead to the clock. How much speed in instruction execution rate will we gain from pipeline ?

- a. 2X
- b. 3X
- c. 5X
- d. 4X

Question **42**

Complete

Mark 1.0 out of 1.0

Which one of the following characteristics is associated with shared memory multiprocessors?

- a. Tightly coupled and coarse grained parallelism
- b. Tightly coupled and fine grained parallelism
- c. Loosely coupled and fine grained parallelism
- d. Loosely coupled and coarse grained parallelism

Question **43**

Complete

Mark 1.0 out of 1.0

For the instruction given below, select the correct option.

I ADD R1, R2, R3

II SUB R1, R2, R3

III LW R1, 0(R7)

IV SW R1, 0(R7)

V BNE R1, R2, Loop

- a. I & II i-Type, III & IV R-Type and V J-Type Instructions
- b. I & II R-Type, III & IV J-Type and V i-Type Instructions
- c. I & II R-Type, III & IV i-Type and V J-Type Instructions
- d. None of the mentioned

Question **44**

Complete

Mark 1.0 out of 1.0

Forwarding can be implemented in 5-stage and 6-stage MIPS pipeline ?

- a. Using one multiplexer
- b. Using two multiplexers with extra latch
- c. Using three multiplexers
- d. Using two multiplexers

Question **45**

Complete

Mark 0.0 out of 1.0

In a 4-bit carry look ahead adder, the propagation delay of EX−OR gate is 20ns, AND and OR gates is 10ns. The sum and carry output of full adder takes 20 ns and 10 ns respectively. Find out the total propagation delay of the above adder in ns .

- a. 64 ns
- b. 58 ns
- c. 60 ns
- d. 62 ns

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