Started on	Wednesday, 23 February 2022, 12:10 PM
State	Finished
Completed on	Wednesday, 23 February 2022, 12:15 PM
Time taken	4 mins 59 secs
Grade	**1.0** out of 5.0 (**20**%)

Question **1**

Incorrect

Mark 0.0 out of 1.0

for Pseudo-direct Addressing. Select the correct option.

- a. Address is 26 bits of constant within instruction concatenated with lower 6 bits of PC ✖
- b. Address is 26 bits of constant within instruction concatenated with upper 6 bits of PC
- c. Address is 26 bits of constant within instruction concatenated with lower 6 bits of Instruction register
- d. Address is 26 bits of constant within instruction concatenated with upper 6 bits of Instruction register

Your answer is incorrect.

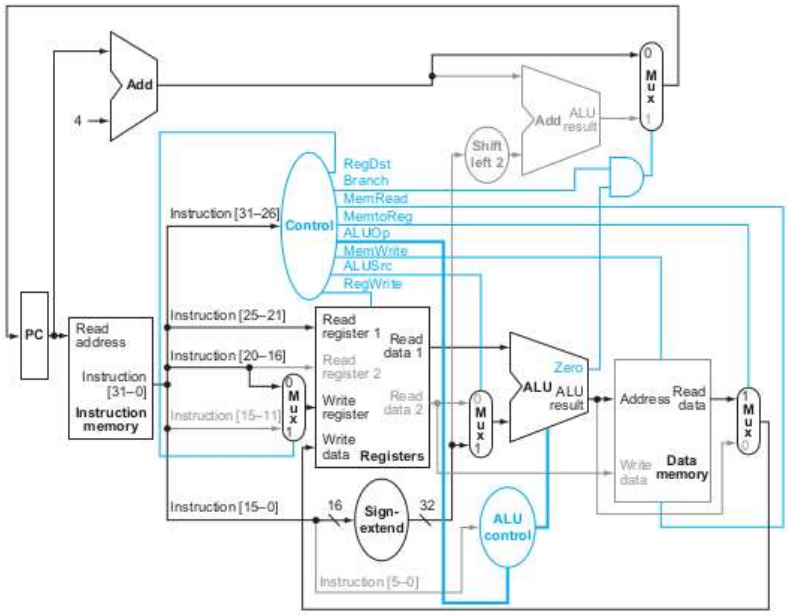
The correct answer is:
Address is 26 bits of constant within instruction concatenated with upper 6 bits of PC

Question **2**

Incorrect

Mark 0.0 out of 1.0

Which type of datapath architecture is given in the following ?



- a. **R-type of instruction** ✖
- b. **Branch on equal instruction**
- c. **With Load instruction**
- d. J-type instruction

Your answer is incorrect.

The correct answer is:
With Load instruction

Question **3**

Correct

Mark 1.0 out of 1.0

For the instructions Load R1, 0(R2). Choose the correct option.

- a. Effective address is calculated by the ALU
- b. Effective address will be the addition of 0 and content of R2
- c. All of the mentioned ✔
- d. From the memory 0+R2's location content will loaded into the destination register

Your answer is correct.

The correct answer is:
All of the mentioned

Question **4**

Incorrect

Mark 0.0 out of 1.0

ALU to support the MIPS instruction should have ?

- a. Multiplexor to select the output we want
- b. All of the mentioned
- c. Subtraction using two's complement
- d. Replica of 1-bit ALU to produce a 32-bit ALU ✖

Your answer is incorrect.

The correct answer is:
All of the mentioned

Question **5**

Incorrect

Mark 0.0 out of 1.0

For the given code select the correct option.

Code:

Load R1, A

Load R2, B

Add R3, R1, R2

Store C, R3

- a. Register to Memory based MIPS processor
- b. Accumulator based MIPS Processor
- c. Memory to register based MIPS processor ✖
- d. Register to register based MIPS processor

Your answer is incorrect.

The correct answer is:
Register to register based MIPS processor

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