Started on	Wednesday, 20 April 2022, 12:10 PM
State	Finished
Completed on	Wednesday, 20 April 2022, 12:15 PM
Time taken	4 mins 54 secs
Marks	4.00/5.00
Grade	**8.00** out of 10.00 (**80**%)

Question **1**

Complete

Mark 1.00 out of 1.00

For virtual memory address translation, select the correct option.

- a. Hardware converts virtual addresses to virtual addresses and OS-managed lookup table
- b. Hardware converts virtual addresses to physical addresses and OS-managed lookup table
- c. Hardware converts physical addresses to virtual addresses and OS-managed lookup table
- d. None of the mentioned

Question **2**

Complete

Mark 1.00 out of 1.00

For the Virtual Memory Design Issues, select the right option.

- a. All of the mentioned
- b. Page faults need not be handled by hardware
- c. Write through approach cannot be used
- d. Page size should be large enough to try to amortize the high access time

Question **3**

Complete

Mark 1.00 out of 1.00

Making Address Translation Faster, Choose the correct option.

- a. Each memory access requires two memory reads
- b. All of the mentioned
- c. A special address translation cache called Translation Lookaside is required
- d. The page tables are stored in the main memory

Question **4**

Complete

Mark 1.00 out of 1.00

For 32 bit data/4 blocks, 32 bit address is given for the CACHE of 32 KB(data part only). Calculate the size of the CACHE?

- a. None of the mentioned
- b. 314 KB
- c. 316 KB
- d. 314 B

Question **5**

Complete

Mark 0.00 out of 1.00

What is miss penalty for the parameters given below.

1. One clock to send the address.

2.10 clocks for each DRAM access.

3.1 clock for send the memory word to CACHE from DRAM.

4. CACHE width is 4W and DRAM width is 1W

- a. 46 Clock Cycles
- b. 45 Clock Cycles
- c. None of the mentioned
- d. 44 Clock Cycles

◄ CS-208-Assignment-4_13-04-2022

Jump to...