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Complete

Mark 0.00 out of 1.00

For the given code (MIPS processor), the total number of stalls required with scheduling?

Original code:

L.D F0, 0(R1)

ADD.D F4,F0,F2

S.D F4, 0(R1)

DADDUI R1,R1, #-8

BNE R1,R2,Loop

☒ a. 4

☐ b. 5

☐ c. 2

☐ d. 3

Question **2**

Complete

Mark 1.00 out of 1.00

Consider the unpipelined machine with 10ns clock cycles. It uses four cycles for ALU operations and branches where as five cycles for memory operations. Assume that the relative frequencies of these operations are 40%,20% and 40% respectively. Let due to clock skew and set up pipelining, the machine adds 1 ns of overhead to the clock. How much speed in instruction execution rate will we gain from pipeline ?

- ☐ a. 5 times
- ☐ b. 6 times
- ☐ c. None of the mentioned
- ☒ d. 4 times

Question **3**

Complete

Mark 1.00 out of 1.00

Consider a pipeline having 4 phases with their execution delays in ns i.e. IF (60), ID(50), IE(90) and WB(80).

The clock duration is calculated based on ?

- ☒ a. IE(90ns)
- ☐ b. IF (60ns)
- ☐ c. WB(80ns)
- ☐ d. ID(50ns)

Question 4

Complete

Mark 1.00 out of 1.00

For the given code (MIPS processor), the total number of stalls required ?

Original code:

L.D F0, 0(R1)

ADD.D F4,F0,F2

S.D F4, 0(R1)

DADDUI R1,R1, #-8

BNE R1,R2,Loop

- ☐ a. 5
- ☐ b. 3
- ☒ c. 4
- ☐ d. 2

Question 5

Complete

Mark 0.00 out of 1.00

For the given code (MIPS processor), the total number of stalls required with loop unrolling 4 copies along with scheduling implementation?

Original code:

L.D F0, 0(R1)

ADD.D F4,F0,F2

S.D F4, 0(R1)

DADDUI R1,R1, #-8

BNE R1,R2,Loop

- ☒ a. 4
- ☐ b. 0
- ☐ c. 2
- ☐ d. 1

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