Started on	Friday, 4 March 2022, 1:50 PM
State	Finished
Completed on	Friday, 4 March 2022, 1:55 PM
Time taken	5 mins 41 secs
Marks	3.00/5.00
Grade	**6.00** out of 10.00 (**60**%)

Question **1**

Complete

Mark 1.00 out of 1.00

For the of RISC pipeline. Choose the correct option.

○ a. All operands are in registers

◉ b. All of the mentioned

○ c. all instructions are the same size

○ d. The only operations that affect memory are loads and stores

Question **2**

Complete

Mark 1.00 out of 1.00

For Implementing Instruction Pipeline ?

◉ a. Cycle time is determined by the longest stage

○ b. None of the mentioned

○ c. Cycle time does not dependent on stages of the pipeline

○ d. Cycle time is determined by the smallest stage

Question **3**

Complete

Mark 0.00 out of 1.00

For the single instruction pipeline (code given below). The two stalls are provided as a part of the program. Choose the correct option?

Begin: add t0, t1, t2

nop

nop

.end Begin

○ a. For the given program two more stalls are required

○ b. For the given program one more stall is required

○ c. For the given program three more stalls are required

◉ d. For the given program no stalls are required

Question **4**

Complete

Mark 1.00 out of 1.00

The Ideal RISC pipeline may have?

○ a. Successive instructions are independent of one another

◉ b. All of the mentioned

○ c. Instructions can be divided into independent parts, each taking nearly equal time

○ d. Instructions are executed in sequence one after the other in the order in which they are written

Question **5**

Complete

Mark 0.00 out of 1.00

A four stage pipeline has the stage delays as 150, 120, 170 and 140 ns respectively. Registers are used between the stages and have a delay of 5 ns each. Assuming constant clocking rate. The total time taken to process 1000 data items on the pipeline?

○ a. 170.5 us

○ b. 165.3 us

◉ c. 165.5 us

○ d. 180.3 us

◄ Assignment 3-25-02-2022

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