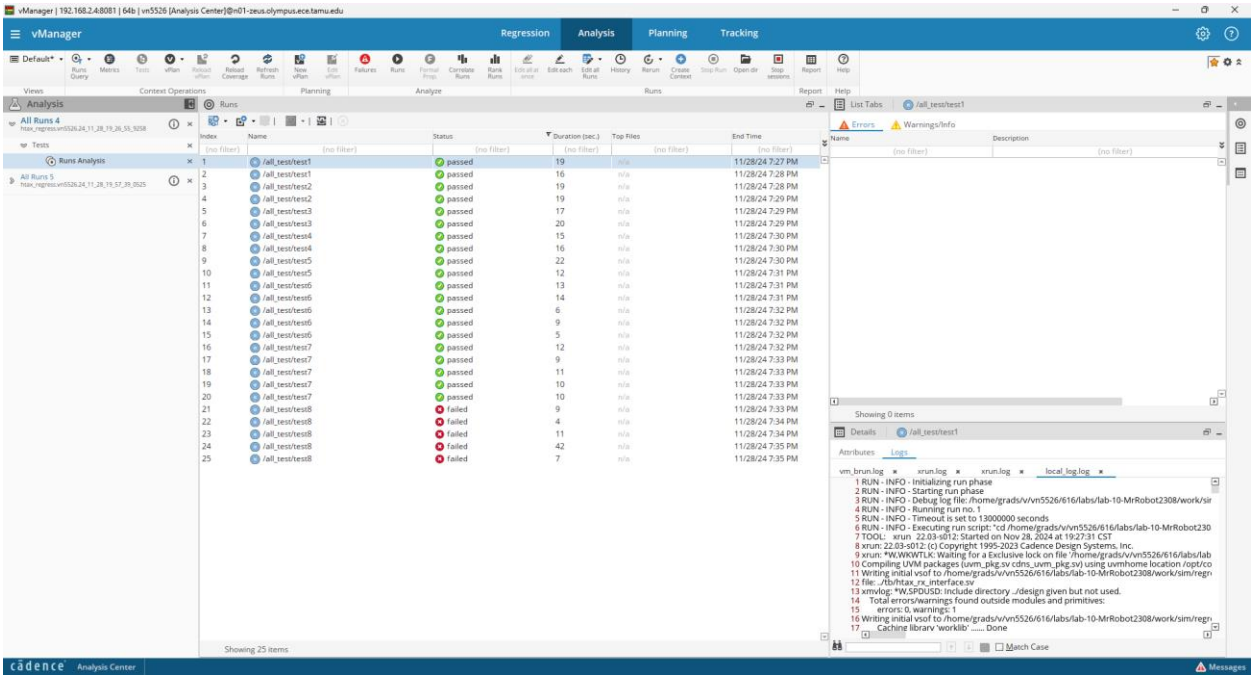
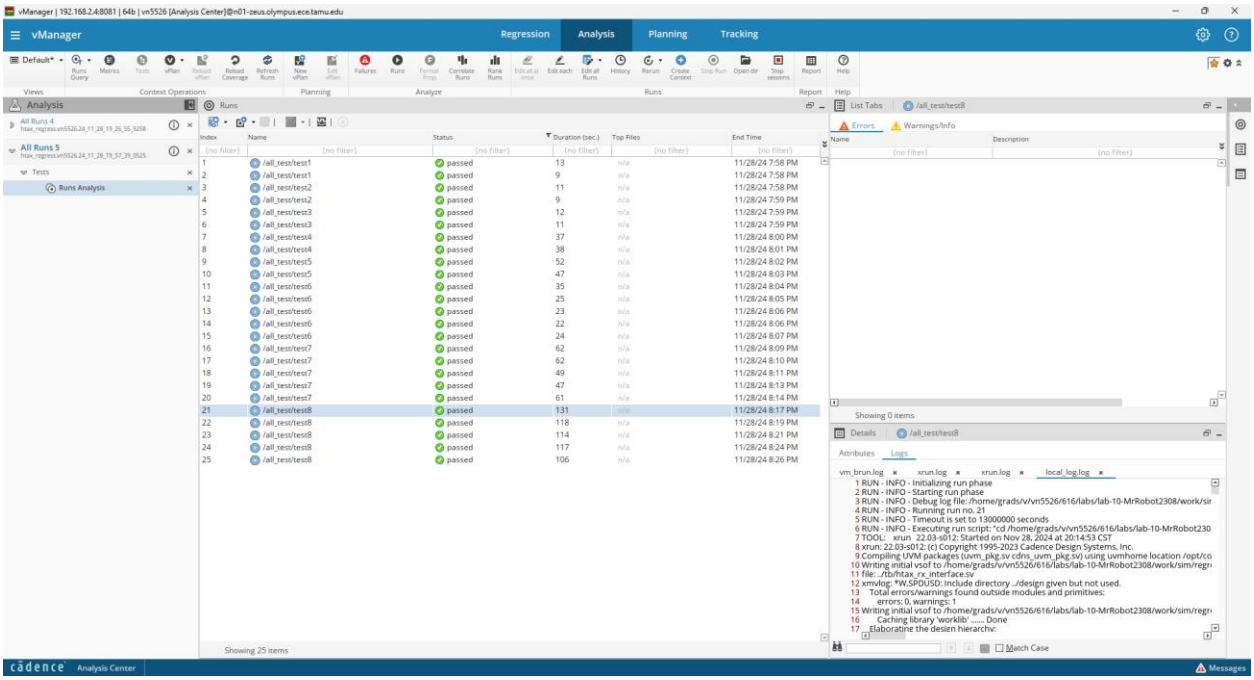
Coverage report

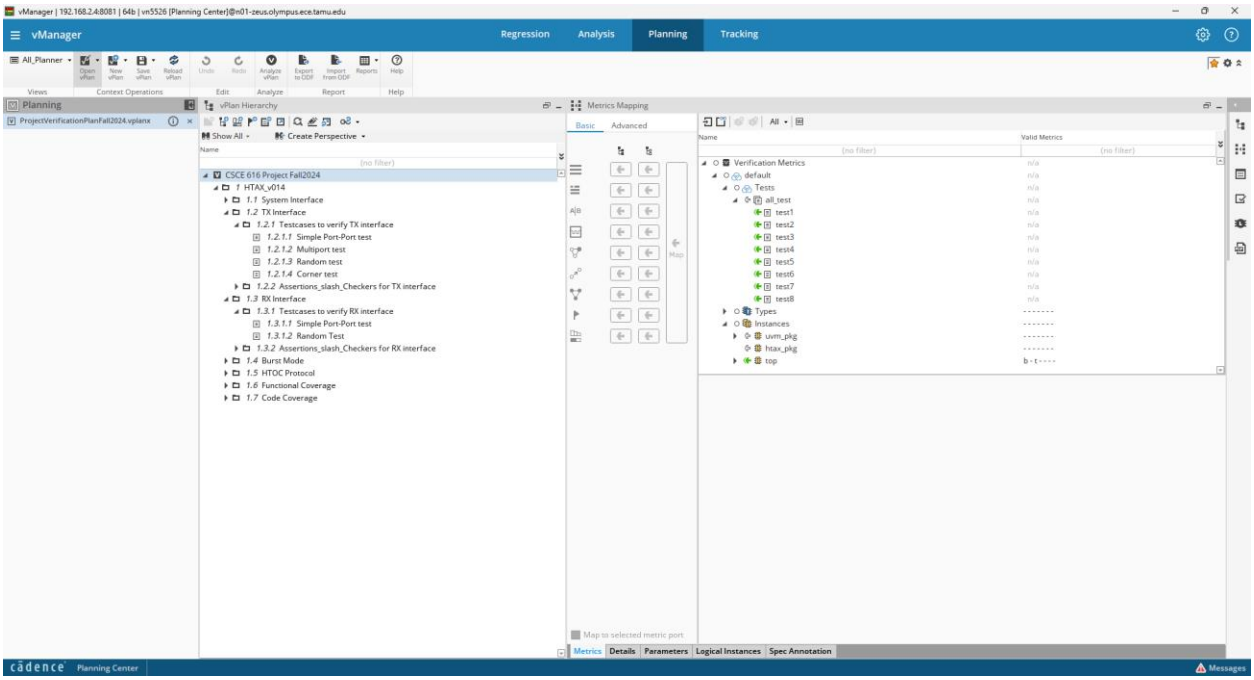
Failing Regression:



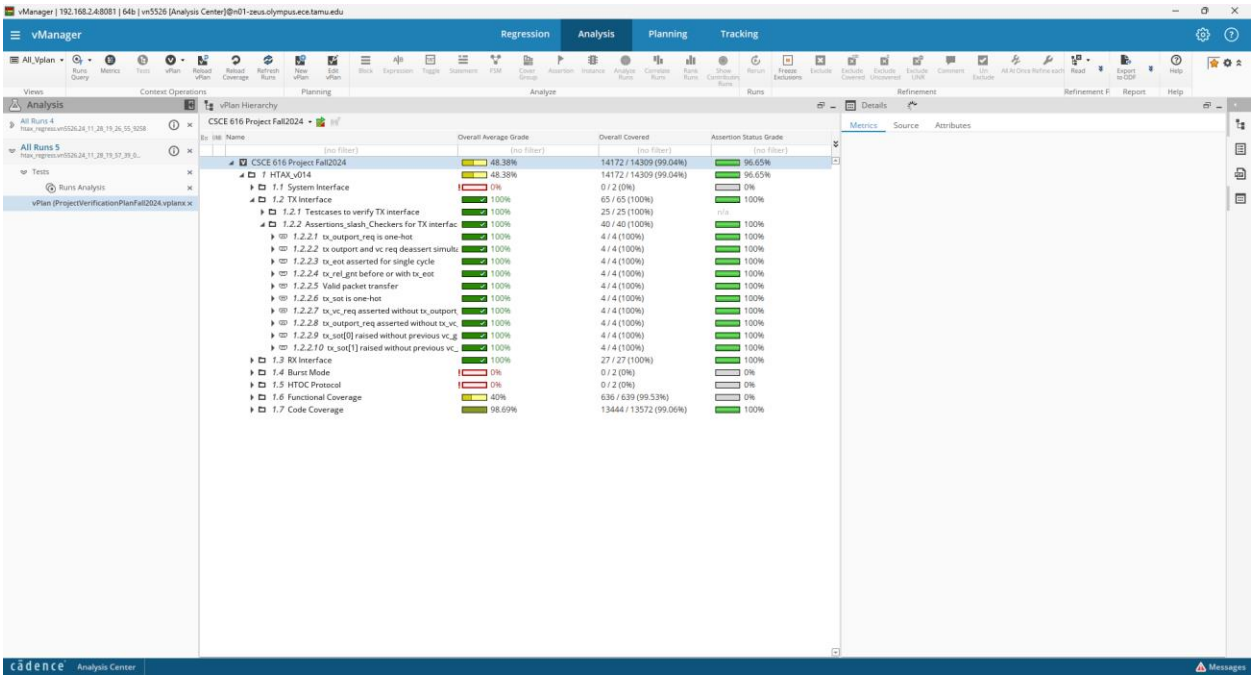
Passing Regression after the failing regression:



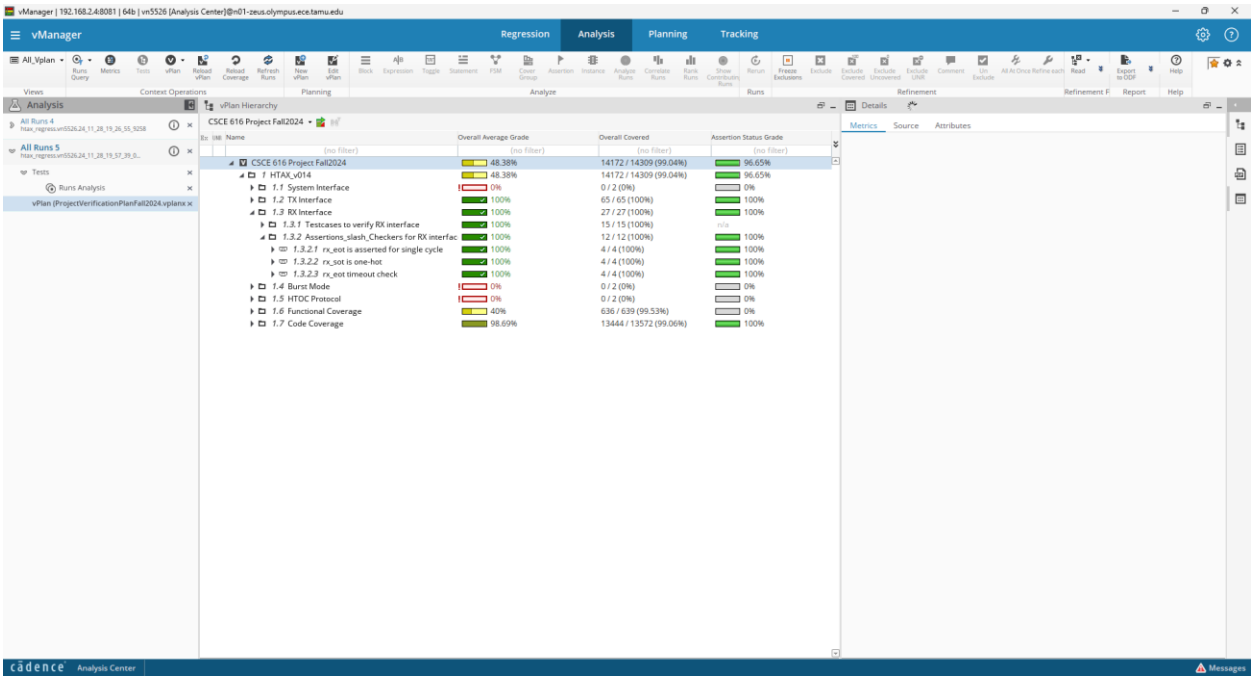
TestCases Mapped:



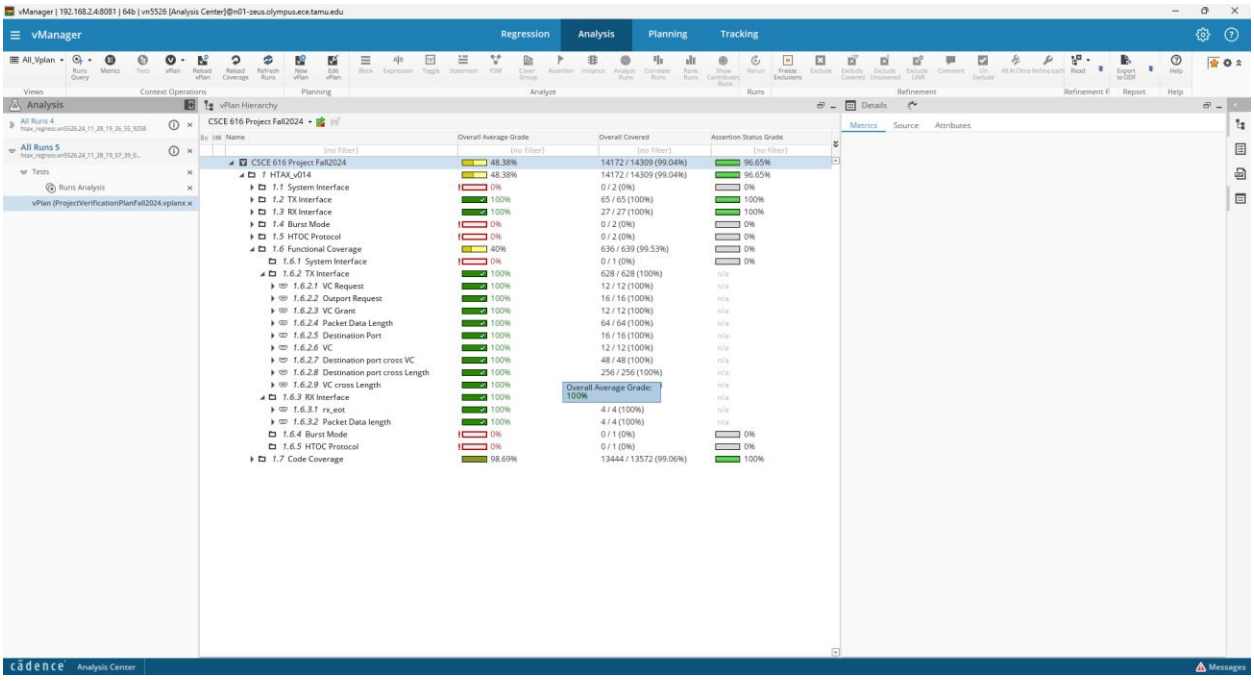
Assertions/Checkers for Tx interface:



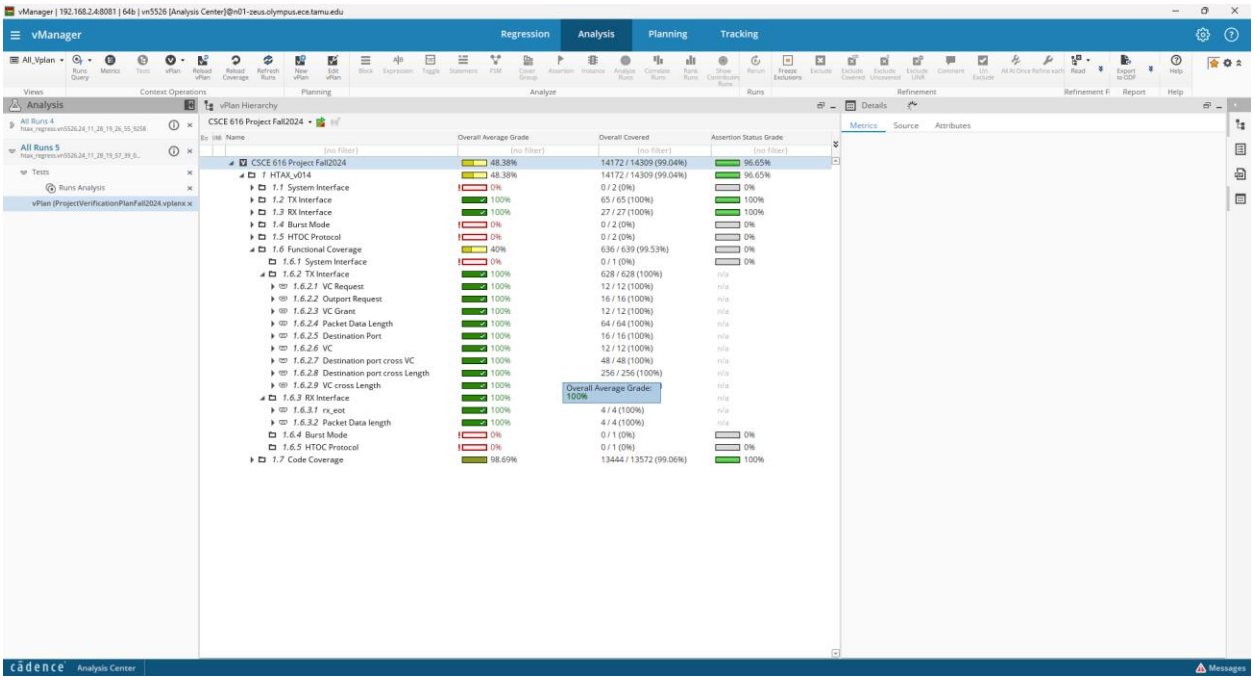
Assertions/Checkers for Rx interface:



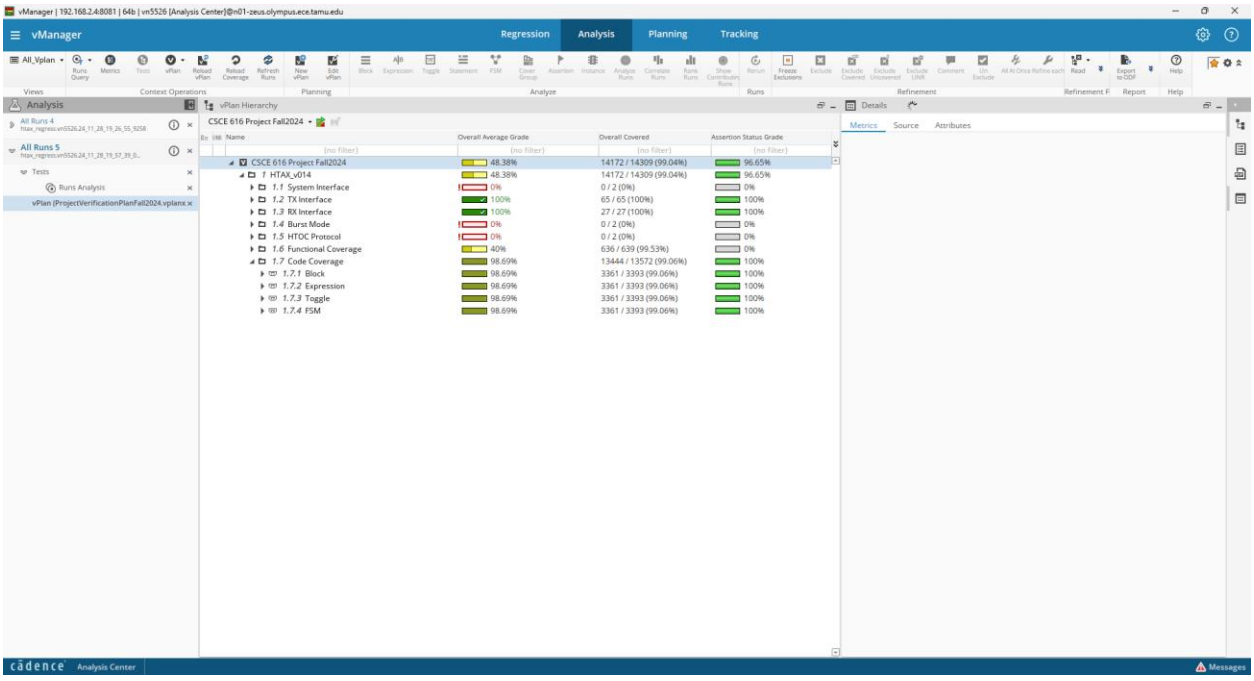
Functional Coverage for Tx interface:



Functional Coverage for Rx interface:



Code Coverage:



Code Coverage Holes:

[Explain any code coverage holes (if any)]

Bugs report

Bug 1

What is the bug?

When multiple short packet sequences are received parallelly on different ports, the rx_eot_timeout_check assertion fails. This means that End of Transmission signal is creating an issue in some part of the design files.

Where is it?

Module: module htax_outport_data_mux

File: module htax_outport_data_mux.v

Line number(s): L43

How to reproduce:

```
task body();
repeat(500) begin
    for (int j = 0; j < 4; j++) begin
    // Shuffle ports before assigning them
    foreach (port[i]) begin
        int rand_idx = $urandom_range(3, i); // Random index between i and 3
        int temp = port[i];
        port[i] = port[rand_idx];
        port[rand_idx] = temp;
    end

    // Fork and send packets with randomized ports
    fork
        `uvm_do_on_with(pkt0, p_sequencer.htax_seqr[port[0]], {pkt0.dest_port == port[0]; pkt0.length inside
        {[3:10]}; pkt0.delay < 5;})
        `uvm_do_on_with(pkt1, p_sequencer.htax_seqr[port[1]], {pkt1.dest_port == port[1]; pkt1.length inside
        {[3:10]}; pkt1.delay < 5;})
        `uvm_do_on_with(pkt2, p_sequencer.htax_seqr[port[2]], {pkt2.dest_port == port[2]; pkt2.length inside
        {[3:10]}; pkt2.delay < 5;})
        `uvm_do_on_with(pkt3, p_sequencer.htax_seqr[port[3]], {pkt3.dest_port == port[3]; pkt3.length inside
        {[3:10]}; pkt3.delay < 5;})
    join
    end
end
```

By running this parallelized short-packet test, the assertion bug can be triggered.

Expected behavior:

The selected_eot signal in the DUT should correctly indicate the End of Transmission. This should work even if EOT occurs on one or more than one input port. This in turn drives the eot timeout assertion which has a tran_cycles_left counter which should decrement when tran_on is active.

Actual behavior:

```
assign selected_eot = |(eot_in & inport_sel_reg) & ~(&(eot_in));
```

The selected_eot signal does not assert when all eot_in bits are set. As a result, the tran_cycles_left counter does not decrement and leads to the eot_timeout assertion fails.

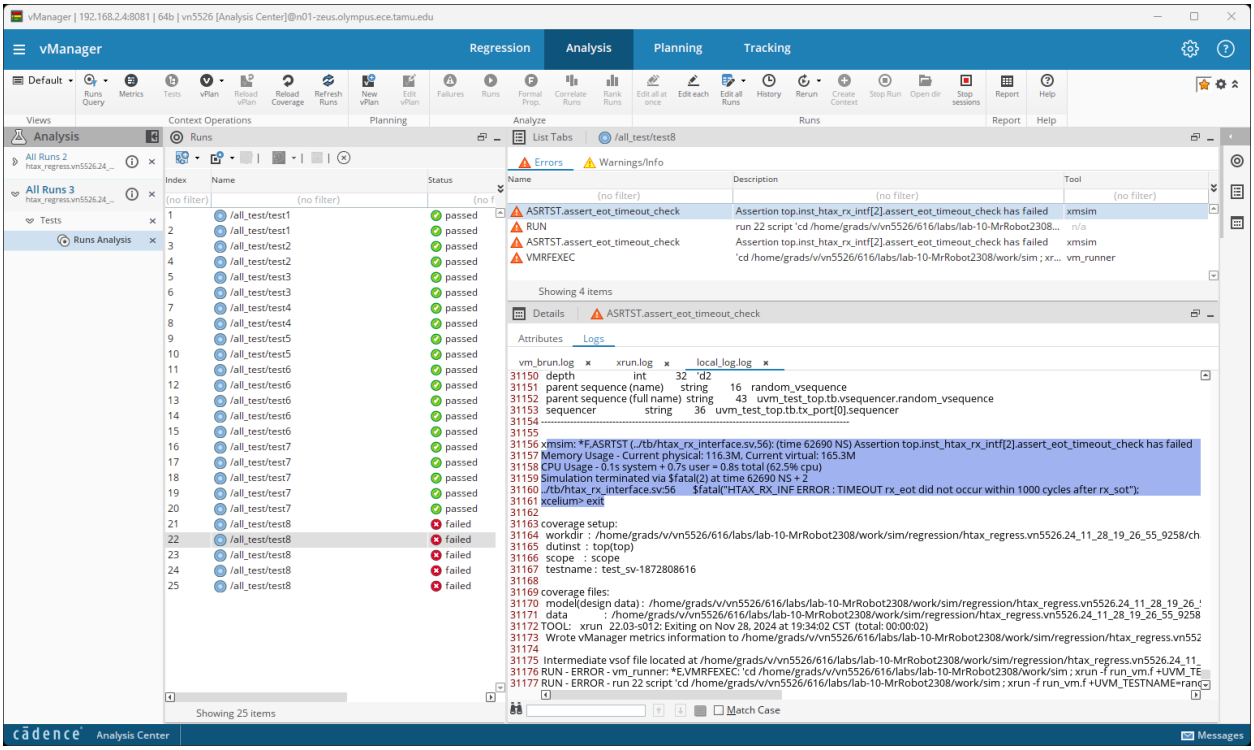
Bug fix:

Removing the `& ~(&(eot_in))` from the design file, should fix the code.

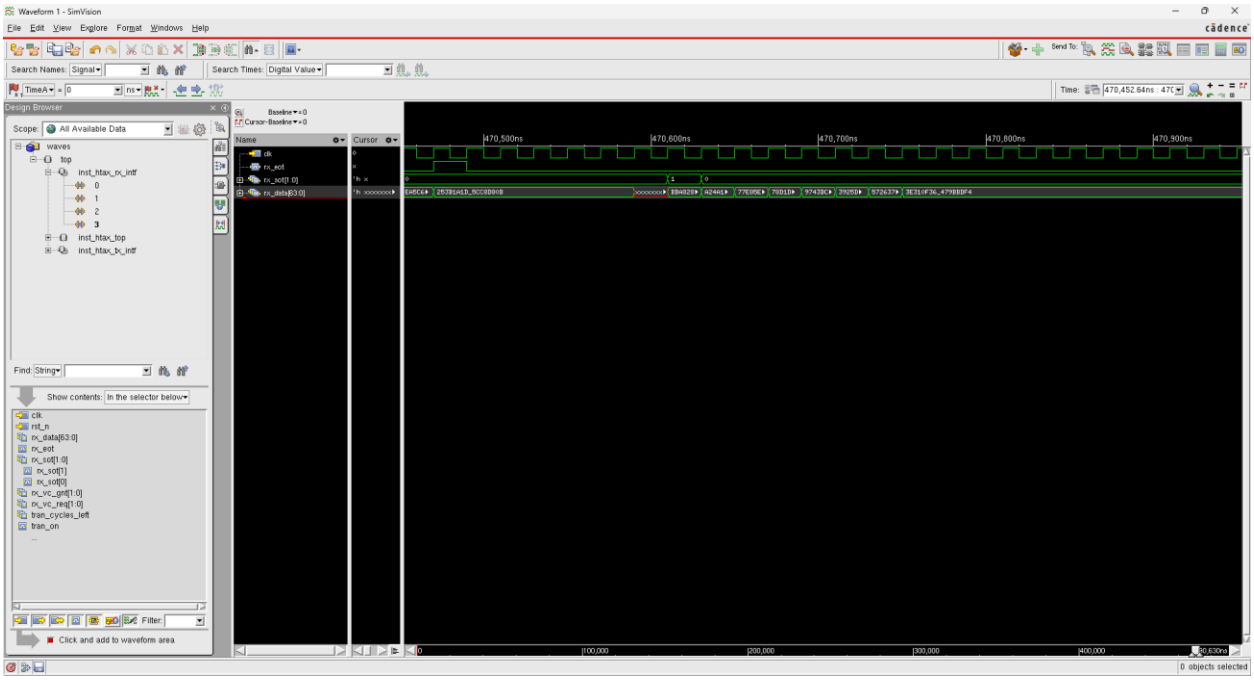
```
assign selected_eot = |(eot_in & inport_sel_reg);
```

This way, the selected_eot signal asserts if any valid EOT signal exists. This removes the erroneous dependency on `~(&(eot_in))`, which incorrectly deasserted selected_eot when all eot_in bits were set.

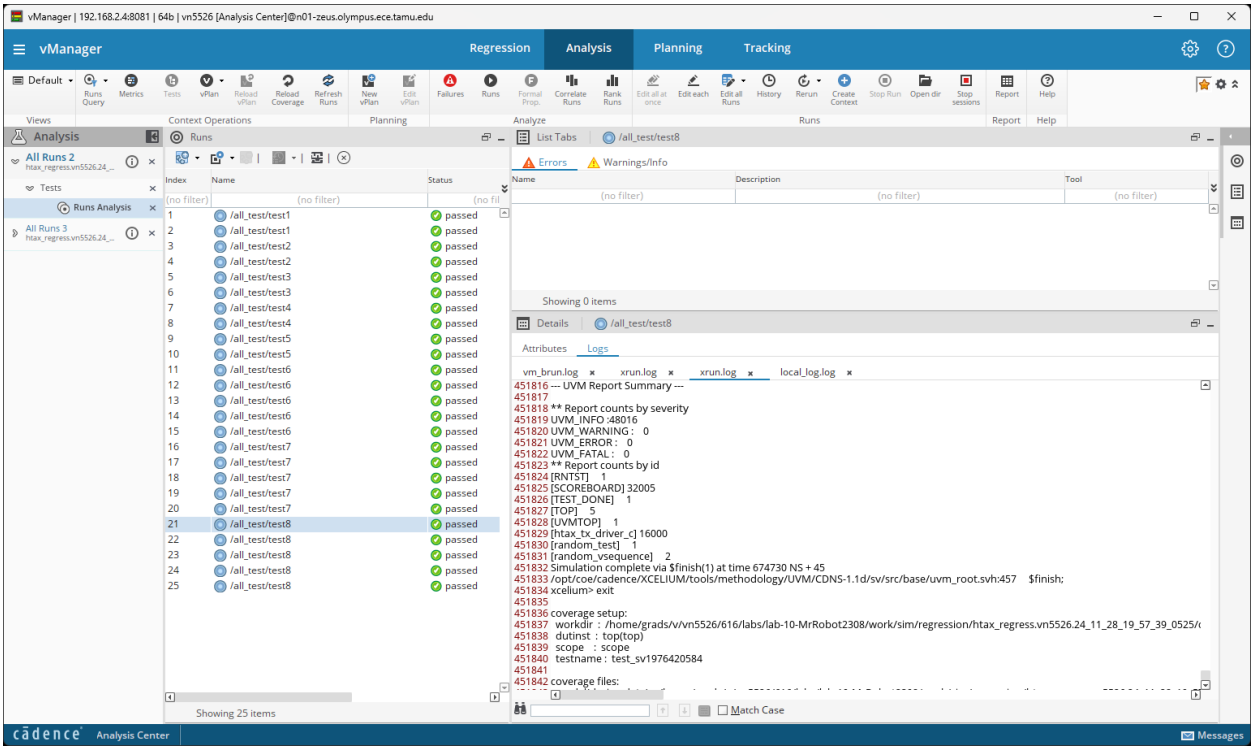
Failing Assertion:



Failing Scenario Waveform:



Failing Assertion Passing after the fix:


vManager | 192.168.2.4:8081 | 64b | vn5526 [Analysis Center]@n01-zeus.olympus.ece.tamu.edu
vManager
Regression
Analysis
Planning
Tracking
Default
Runs Query
Metrics
Tests
vPlan
Reload vPlan
Reload Coverage
Refresh Runs
New vPlan
Edit vPlan
Failures
Runs
Formal Prop.
Correlate Runs
Rank Runs
Edit all at once
Edit each
Edit all Runs
History
Rerun
Create Context
Stop Run
Open dir
Stop sessions
Report
Help
Views
Context Operations
Planning
Analyze
Runs
Report
Help
Analysis
All Runs 2
htax_regress.vn5526.24_...
Tests
Runs Analysis
All Runs 3
htax_regress.vn5526.24_...
Runs
Index
Name
Status
(no filter)
1 /all_test/test1 passed
2 /all_test/test1 passed
3 /all_test/test2 passed
4 /all_test/test2 passed
5 /all_test/test3 passed
6 /all_test/test3 passed
7 /all_test/test4 passed
8 /all_test/test4 passed
9 /all_test/test5 passed
10 /all_test/test5 passed
11 /all_test/test6 passed
12 /all_test/test6 passed
13 /all_test/test6 passed
14 /all_test/test6 passed
15 /all_test/test6 passed
16 /all_test/test7 passed
17 /all_test/test7 passed
18 /all_test/test7 passed
19 /all_test/test7 passed
20 /all_test/test7 passed
21 /all_test/test8 passed
22 /all_test/test8 passed
23 /all_test/test8 passed
24 /all_test/test8 passed
25 /all_test/test8 passed
Showing 25 items
List Tabs
/all_test/test8
Errors
Warnings/Info
Name
Description
Tool
(no filter)
Showing 0 items
Details
/all_test/test8
Attributes
Logs
vm_brun.log
xrun.log
xrun.log
local_log.log
451816 --- UVM Report Summary ---
451817
451818 ** Report counts by severity
451819 UVM_INFO :48016
451820 UVM_WARNING : 0
451821 UVM_ERROR : 0
451822 UVM_FATAL : 0
451823 ** Report counts by id
451824 [RNTST] 1
451825 [SCOREBOARD] 32005
451826 [TEST_DONE] 1
451827 [TOP] 5
451828 [UVMTOP] 1
451829 [htax_tx_driver_c] 16000
451830 [random_test] 1
451831 [random_vsequence] 2
451832 Simulation complete via $finish(1) at time 674730 NS + 45
451833 /opt/coe/cadence/XCELIUM/tools/methodology/UVM/CDNS-1.1d/sv/src/base/uvm_root.svh:457 $finish;
451834 xcelium> exit
451835
451836 coverage setup:
451837 workdir : /home/grads/v/vn5526/616/labs/lab-10-MrRobot2308/work/sim/regression/htax_regress.vn5526.24_11_28_19_57_39_0525/
451838 dutinst : top(top)
451839 scope : scope
451840 testname : test_sv1976420584
451841
451842 coverage files:
Match Case
cadence
Analysis Center
Messages