DIGITAL INTELLECTUAL PROPERTY CORES (IP) DESIGN

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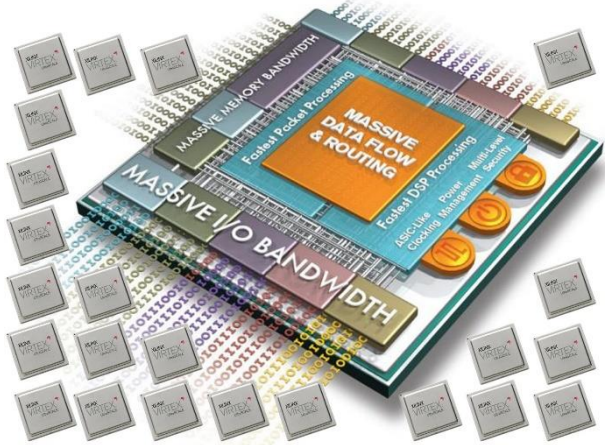
Course URL: https://sites.google.com/view/trinhquangkien/Courses/

LECTURE 1.3 OUTLINE

- Introduction of FPGA
  - What is an FPGA?
  - FPGA architecture
  - FPGA configurability
  - FPGA resources

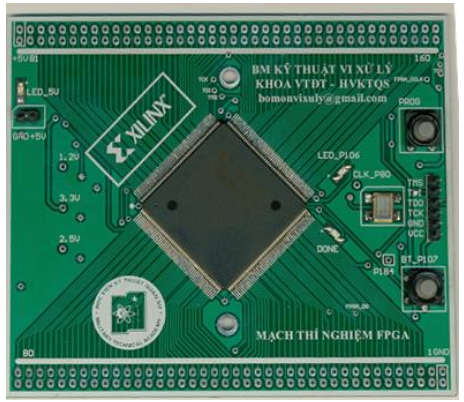


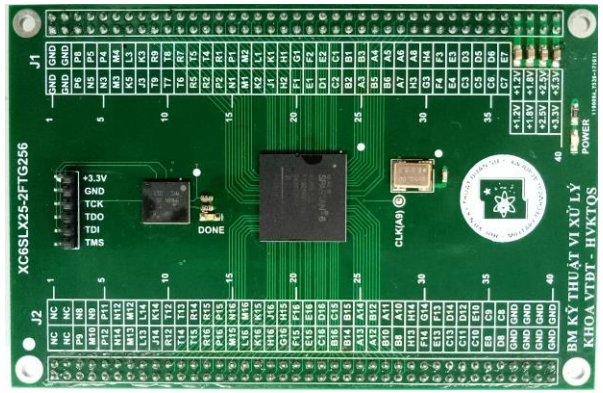
intel FPGA

XILINX
ALL PROGRAMMABLE™

WHAT IS THE FPGA?

- *FPGA* (Xilinx.com):*
  - *Field-programmable Gate Arrays are semiconductor devices that are based around a matrix of configurable logic blocks (CLBs) connected via programmable interconnects. FPGAs can be reprogrammed to desired application or functionality requirements after manufacturing.*
- *Other means to build a digital system:*
  - *ASICs Application-Specific Integrated Circuits*
  - *ASSPs Application-Specific Standard Products*





** Modern FPGA is an integrated IC based on CMOS technology*

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FPGA APPLICATIONS

Implementation of random logic

- easier changes at system-level (one device is modified)
- can eliminate need for full-custom chips

Prototyping

- ensemble of gate arrays used to emulate a circuit to be manufactured
- get more/better/faster debugging done than possible with simulation

Reconfigurable hardware

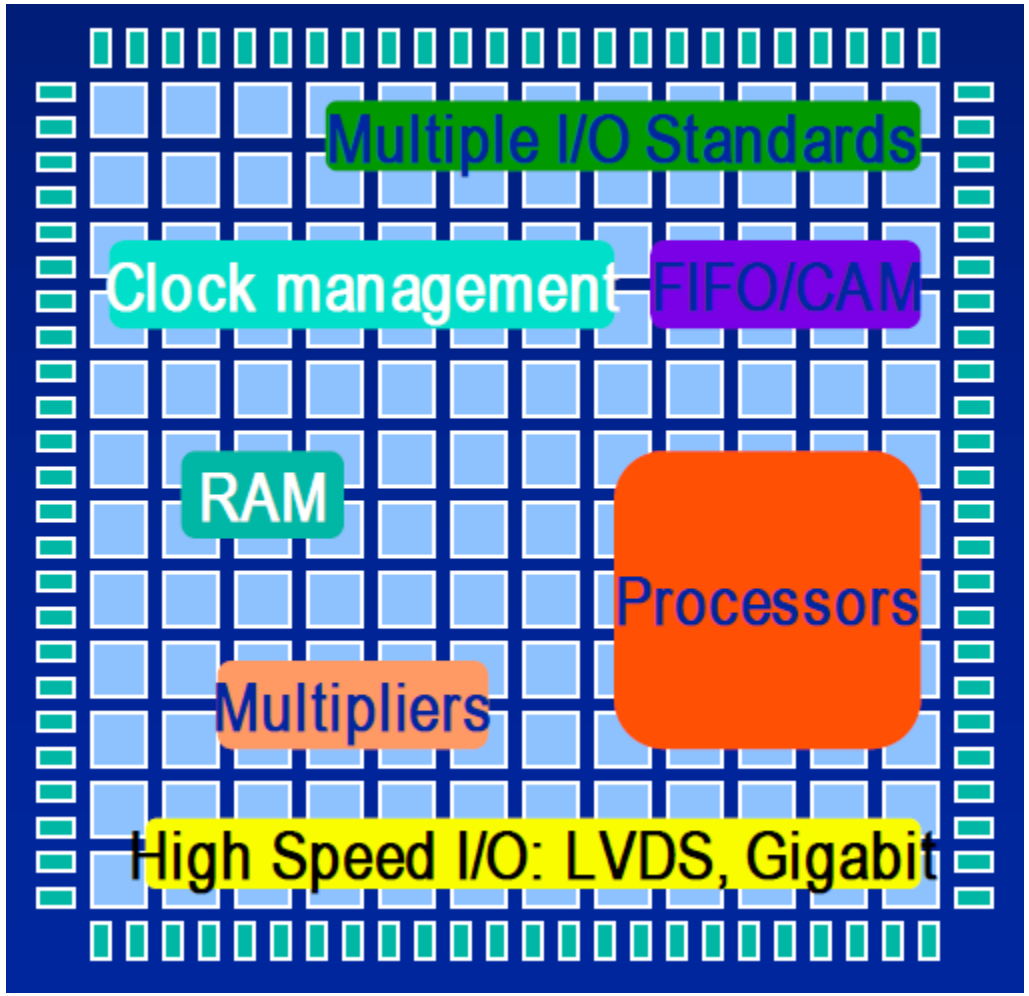
- one hardware block used to implement more than one function
- functions must be mutually-exclusive in time
- can greatly reduce cost while enhancing flexibility
- RAM-based only option

Special-purpose computation engines

- hardware dedicated to solving one problem (or class of problems)
- accelerators attached to general-purpose computers

FPGA ARCHITECTURE

- **configurable logic blocks** (up to 10 millions gates)
- **configurable interconnects**
- **configurable IO pads** (large number 100-1000 pins)
- Two-dimensional array (matrix) architecture: scalable
- state-of-the-art CMOS process (most advanced 7nm),
  - High speed (up to 500 Mhz logic core)
  - High density (tens of billion transistor count)
- Integrated dedicated IPs
  - DSP
  - Block RAM (SRAM-based)
  - Embedded CPU
  - High-speed IO (GTP (6.5Gbps), GTX (12Gbps), GTZ (32Gbps), 100Gbps Ethernet, 150Gbps Interlake
  - AI engines (Versal FPGA)
- Low-cost reconfigurability by the end user



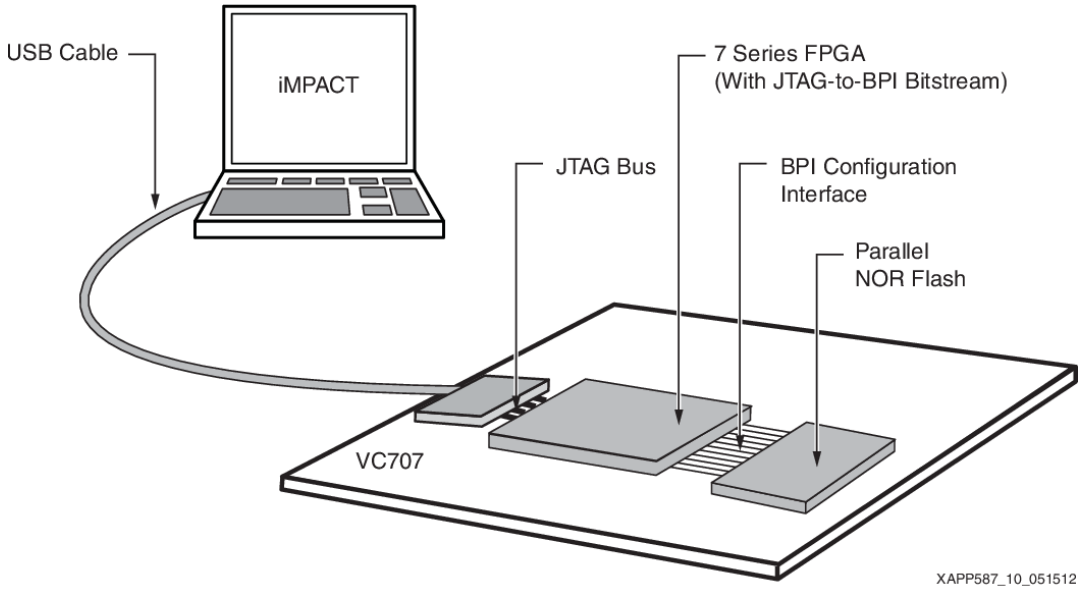
IC INTEGRATION

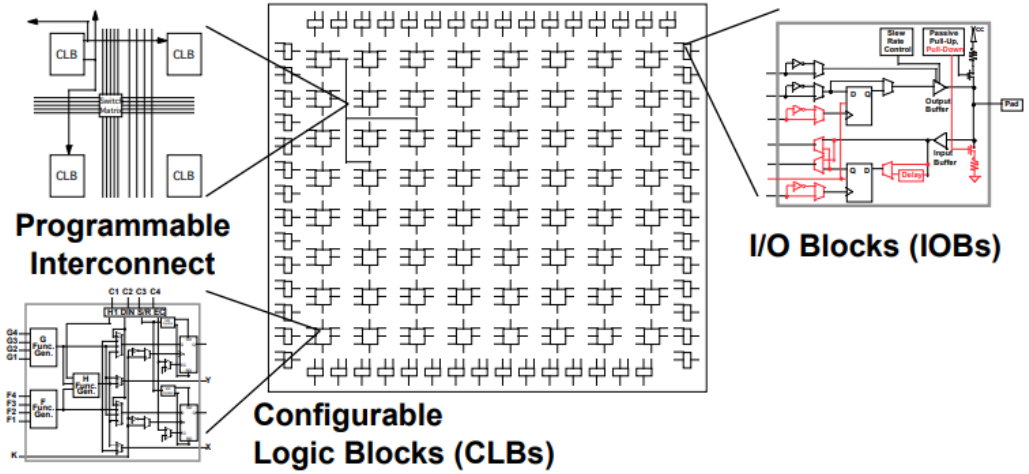
IC	Transitor count	Process	Manufacture	Year
Intel 4004	2 300	10 um	Intel	1971
Zilog Z80	8 500	4 um	Zilog	1976
Intel 80286	164 000	1.5 um	Intel	1982
Pentium 2	7 500 000	0.35um	Intel	1997
Pentium 4	42 000 000	180 nm	Intel	2000
Core 2 Duo	291 000 000	65 nm	Intel	2006
Six core Xenon 7400	1 900 000 000	45 nm	Intel	2008
10-Core Xeon	2 600 000 000	32 nm	Intel	2010
GK110 Kepler	7,080,000,000	28nm	NVIDIA	2012
AMD K8	106 000 000	130 nm	AMD	2003
Spartan 3E	~40 000 000	90 nm	Xilinx	1998
Virtex 5	1 100 000 000	65 nm	Xilinx	2006
Starix IV	2 500 000 000	40 nm	Altera	2008
Starix V	3 800 000 000	28 nm	Altera	2011
Virtex 7	~6 800 000 000	28nm	Xilinx	2011
Versal VC1902	37,000,000,000	7nm	Xilinx	2H 2019

https://en.wikipedia.org/wiki/Transistor_count

FPGA PROGRAMMABILITY

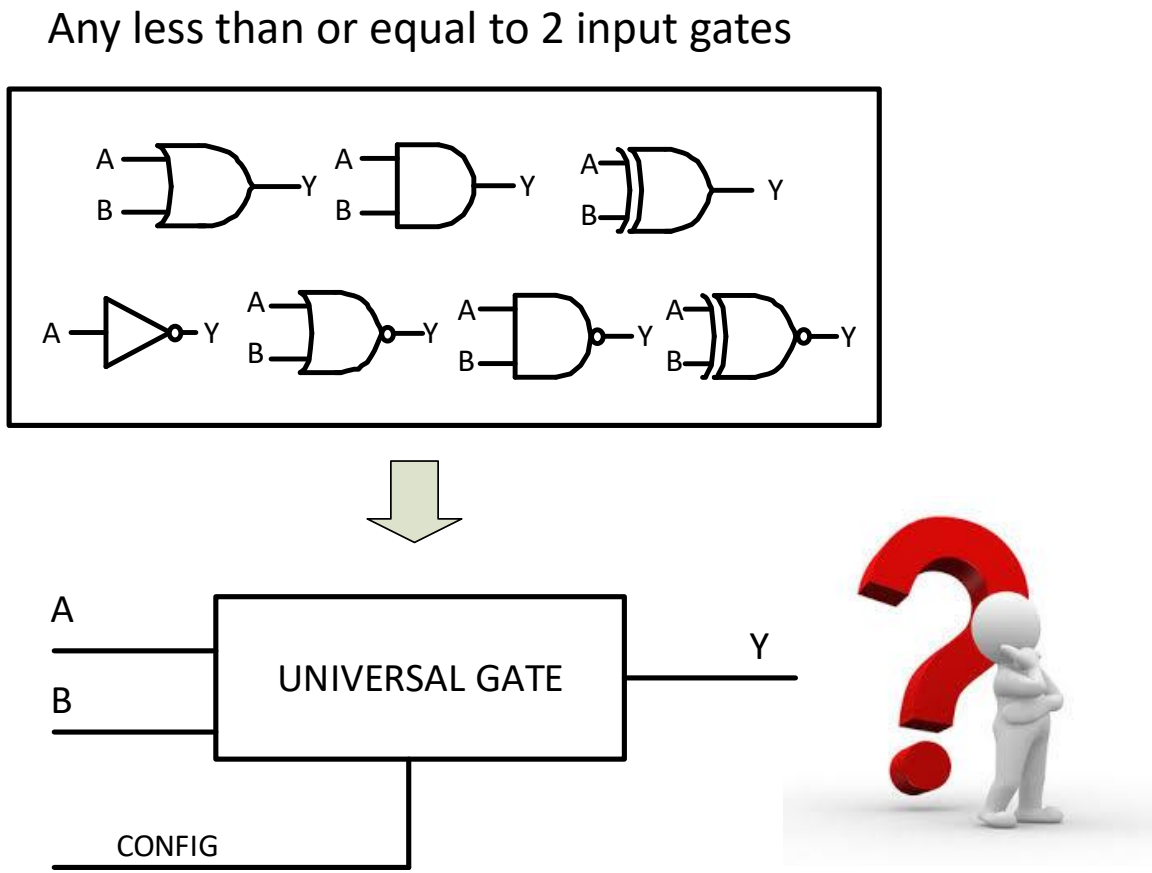
- SRAM-based (volatile memory) configuration file (bitstream)
- Permanent configuration
  - Serial Peripheral interface (SPI) Flash
  - Byte-peripheral interface BPI Flash
- Others options (outdated FPGA)
  - Fused and anti-fused (one time)
  - EPROM and EEPROM (high power consumption, difficult for integration)





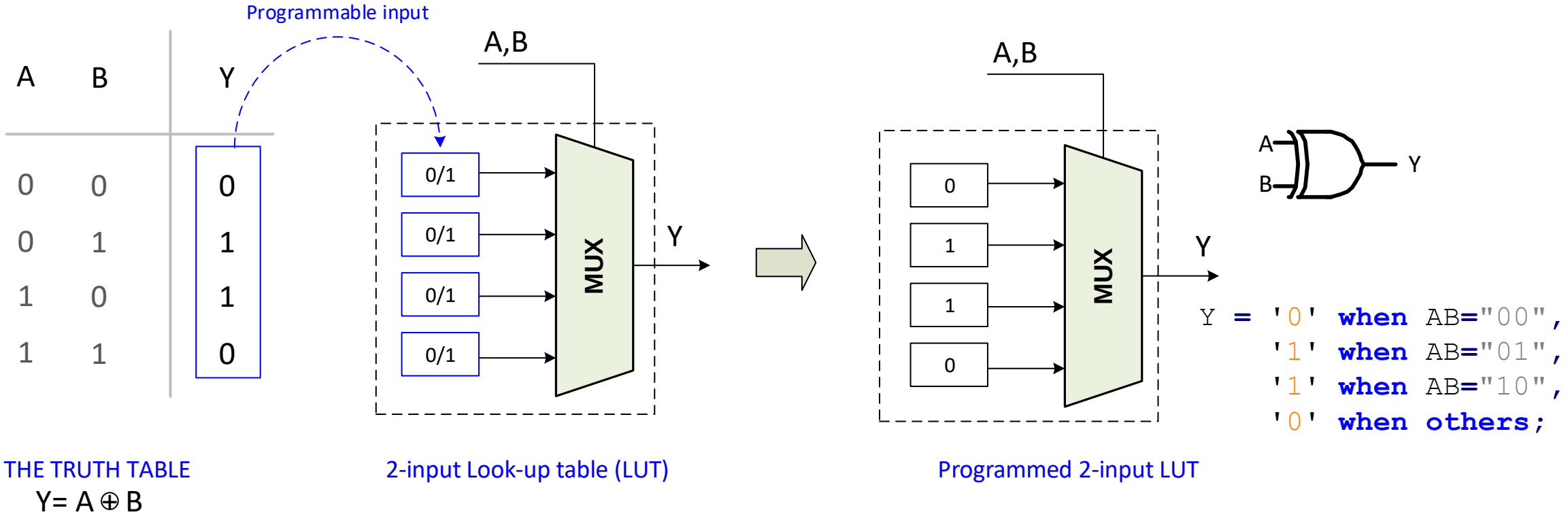
FPGA PROGRAMABLE LOGIC

- Which universal circuit can do all logic functions?
- Logic function representation ?
  - Boolean function
  - Schematics
  - Truth table
- Two equivalent circuit?
  - *Which-ever input results in the same output*
- Classic theorem:
  - All logic functions can be implemented via basic gates



FPGA PROGRAMABLE LOGIC: EXAMPLE #1

- XOR gate equivalent 2-inputLUT



THE TRUTH TABLE

$Y = A \oplus B$

2-input Look-up table (LUT)

Programmed 2-input LUT

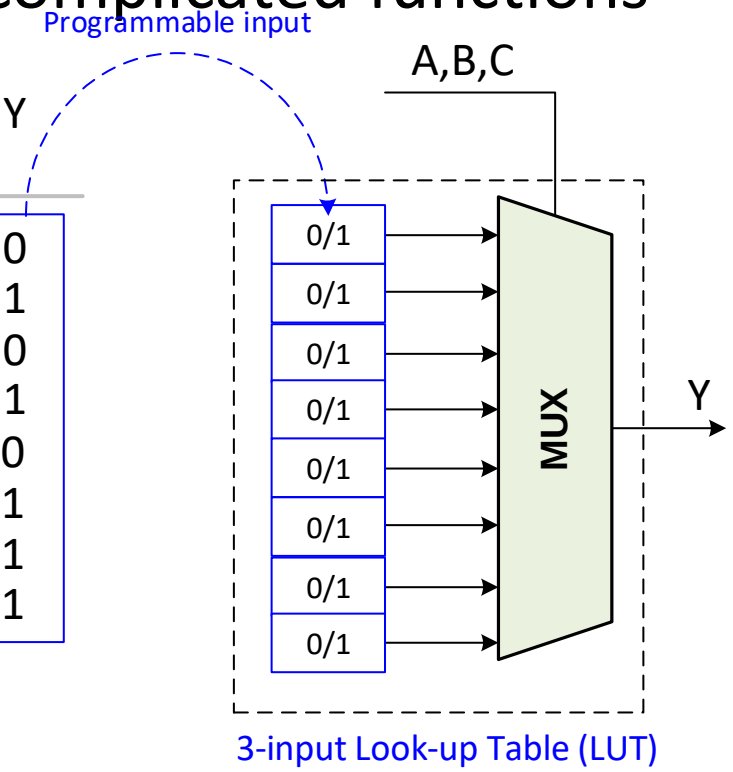
FPGA PROGRAMABLE LOGIC: EXAMPLE #2

- More complicated functions

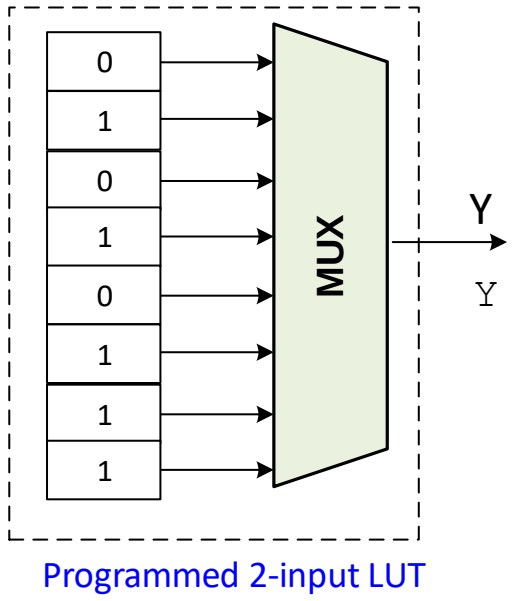
A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

THE TRUTH TABLE

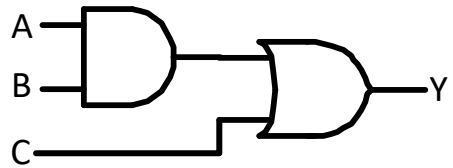
Y= A B + C



3-input Look-up Table (LUT)



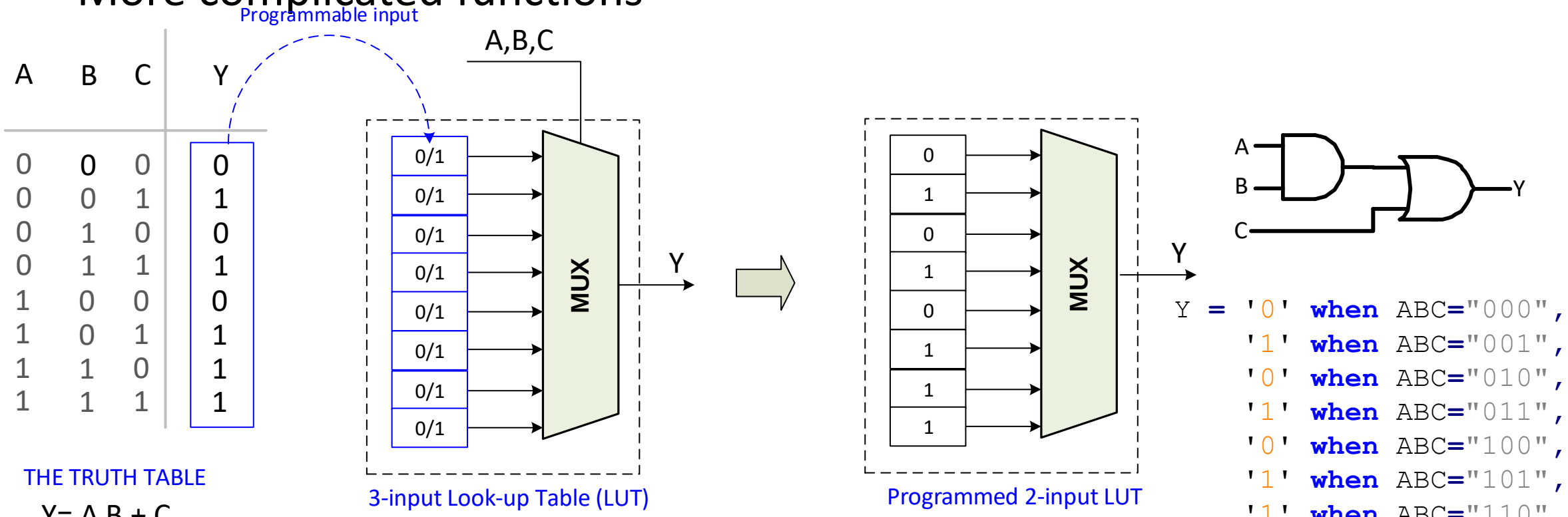
Programmed 2-input LUT




```
Y = '0' when ABC="000",
    '1' when ABC="001",
    '0' when ABC="010",
    '1' when ABC="011",
    '0' when ABC="100",
    '1' when ABC="101",
    '1' when ABC="110",
    '1' when others;
```

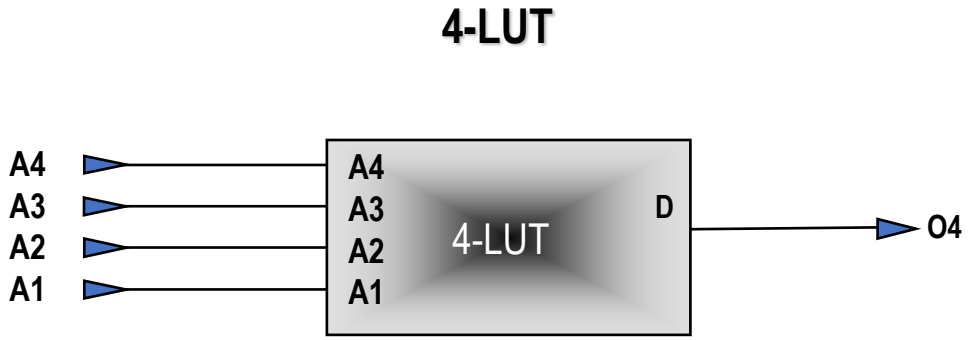
FPGA PROGRAMABLE LOGIC: EXAMPLE #2

- More complicated functions

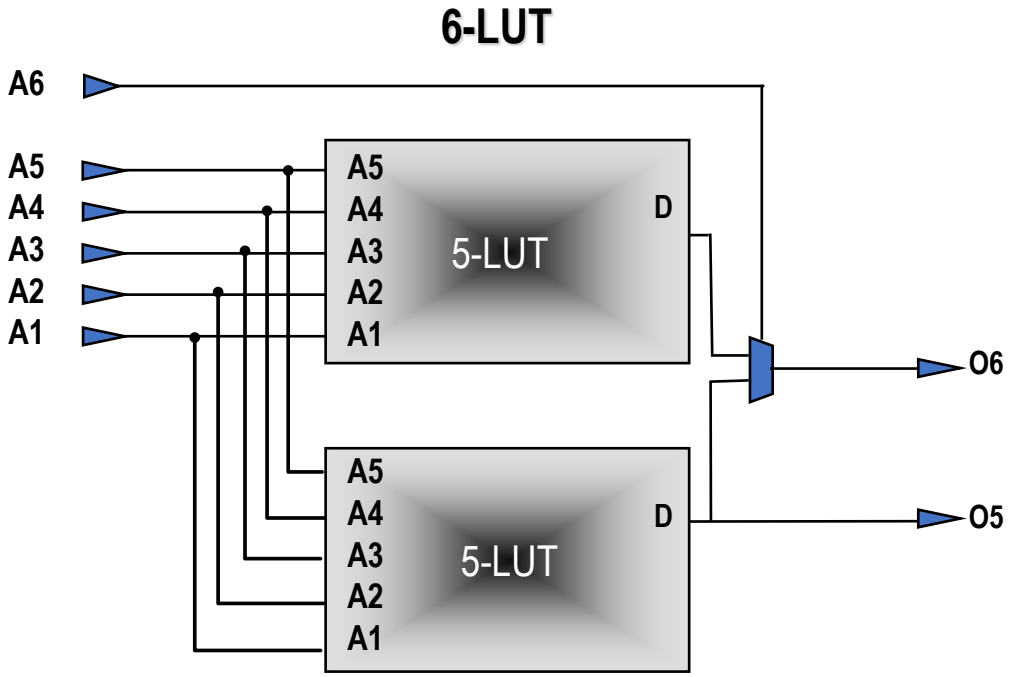


FPGA PROGRAMABLE LOGIC: LUT

- 4-LUT vs 6 LUT in FPGA



Spartan 3/3E 4 input LUT



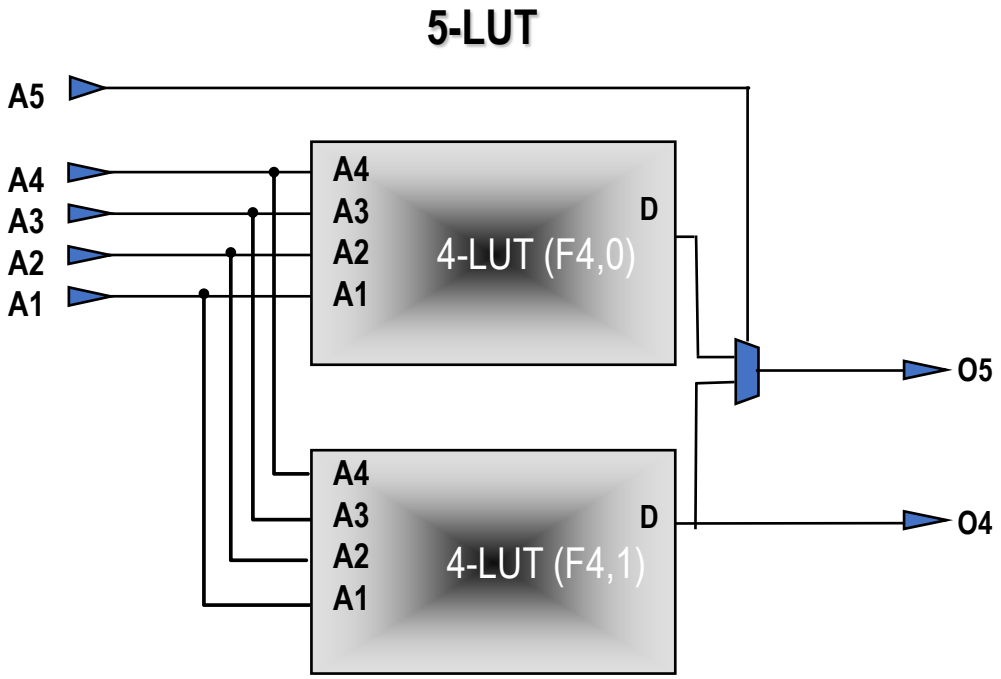
Series 7 6-input LUTs

FPGA WIDE MULTIPLEXER

- How to implement larger number of input functions?

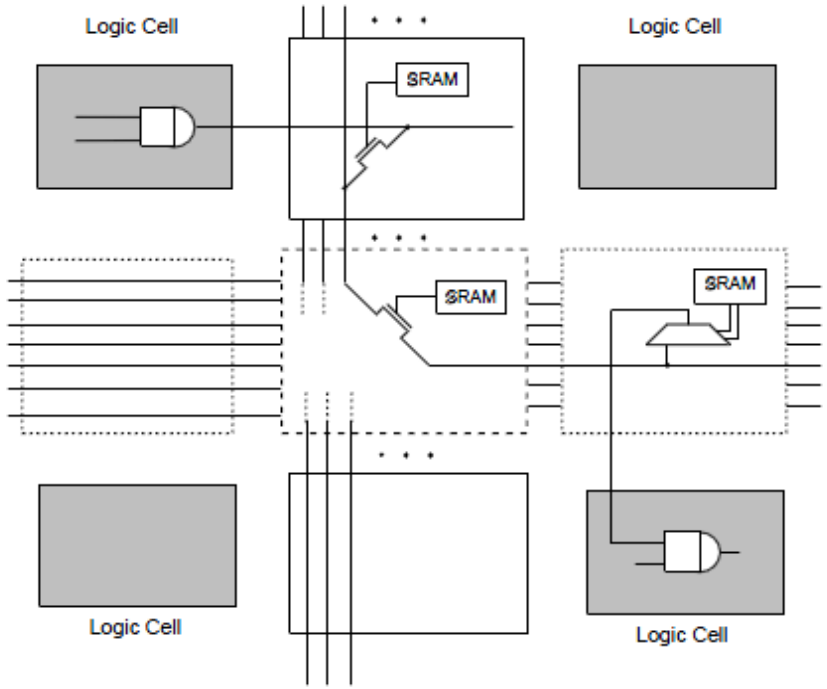
$$O_5 = F_{5(A_5,A_4,A_3,A_2,A_1)} = \begin{cases} F_5(0, A_4, A_3, A_2, A_1) \text{ when } A_5{=}0 \\ F_5(1, A_4, A_3, A_2, A_1) \text{ when } A_5{=}1 \end{cases}$$

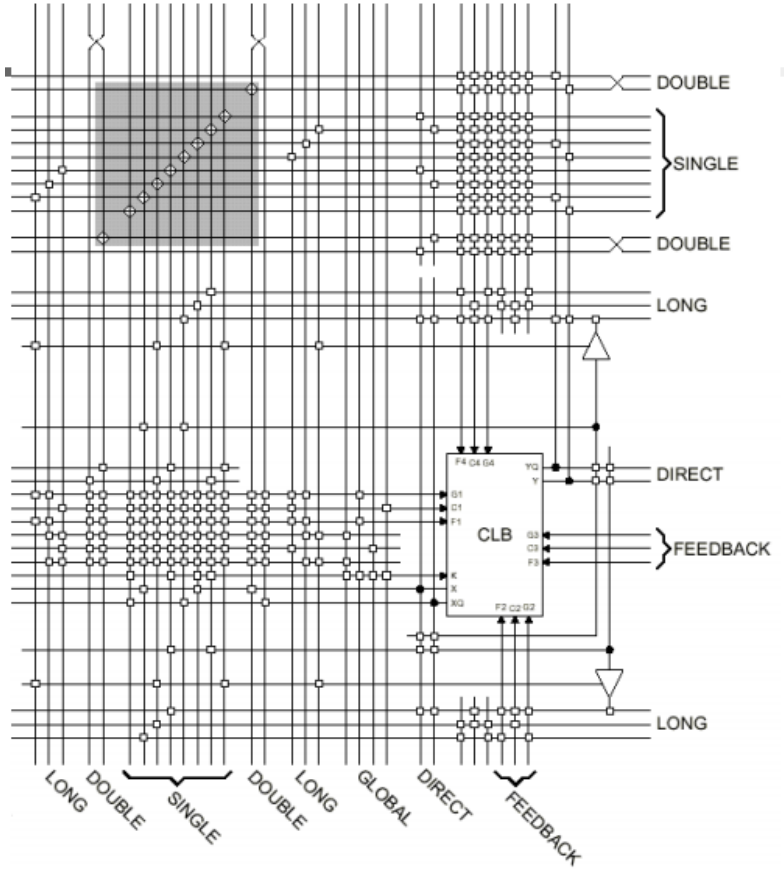
$$= \begin{cases} F_{4,0}(A_4, A_3, A_2, A_1) \text{ when } A_5{=}0 \\ F_{4,1}(A_4, A_3, A_2, A_1) \text{ when } A_5{=}1 \end{cases}$$



FPGA PROGRAMABLE INTERCONECT

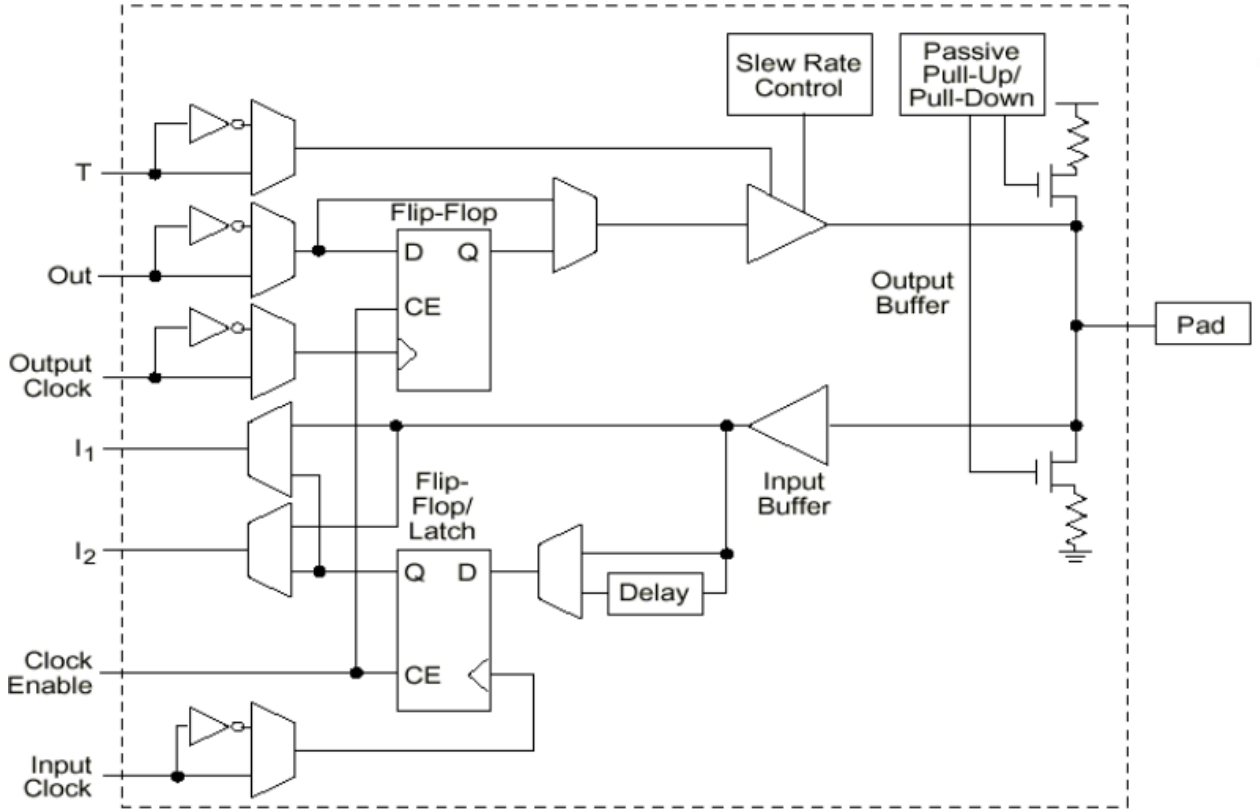
- Routing is done by a pass transistor (switch)
  - 1: connected
  - 0: isolated
- Routing lines
  - Direct
  - Double/single
  - Long line
  - Global





FPGA PROGRAMABLE IO

- Majority IO are inout Pin
- Signal can be delayed by a programmable value
- Support double data rate (DDR)
- Programmable voltage
- GTP, GTX, GTX for Gigabit serial transmission (all are LVDS)



FPGA FURTHER READING TOPIC

- Examples of FPGA Architectures
  - Spartan 3 Architectures
  - Spartan-6 FPGA Configurable Logic Block
  - 7 Series FPGAs Configurable Logic Block
- FPGA for dummies ☺