Reducing Complexity of CD-NOMA Decoding Algorithm Using Hardware Optimization

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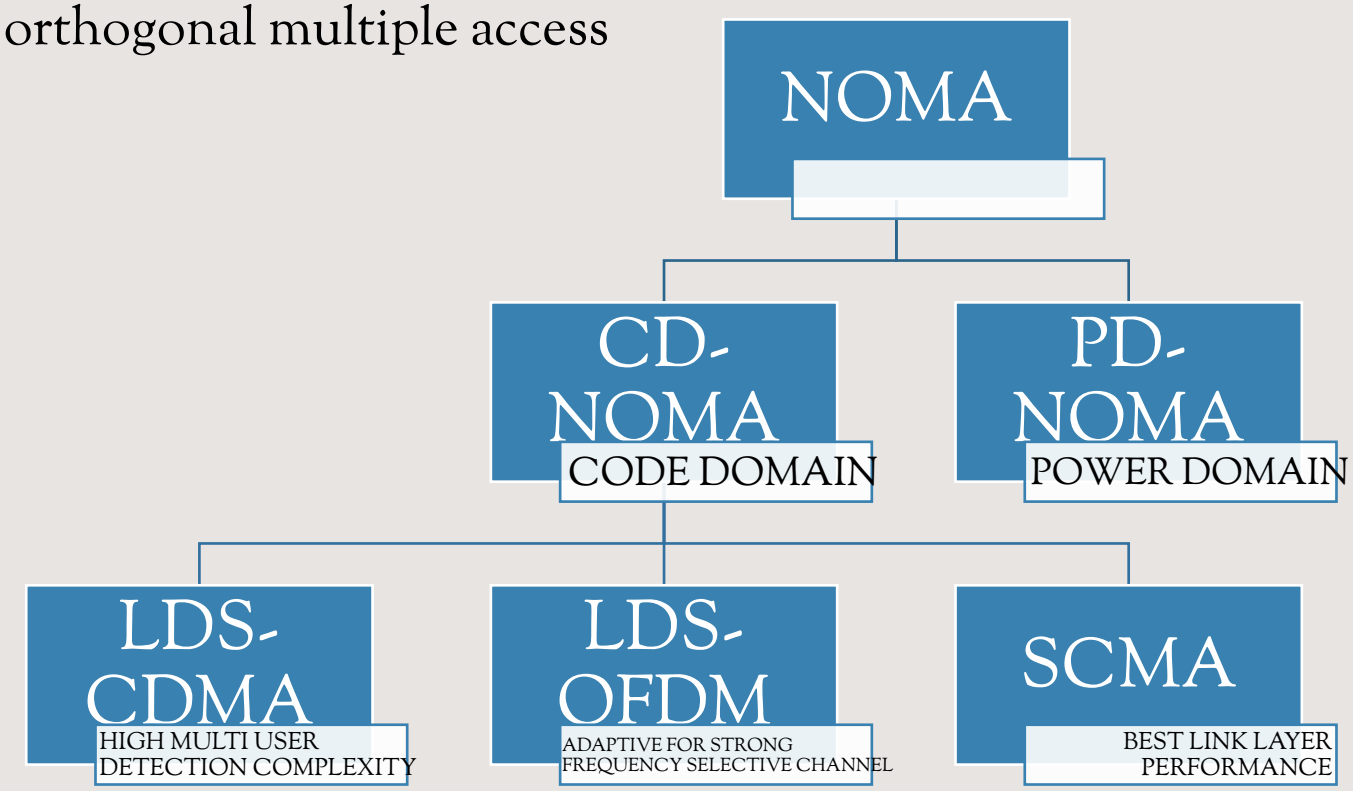
5g challenges

- Increasing no. of connected users and devices
- Target connection density: 1 million devices per km^2 [1]
- Difficulty in satisfying this with flexible - orthogonal multiple access techniques

CD-NOMA

- Code-Domain Non-Orthogonal Multiple Access (NOMA) evolved from CDMA
- Provides access to finite system resources
  - Simultaneously
  - Efficiently



CD-NOMA

- Allows multiple users to share same REs (Resource Element
- Each user adapts unique user specific spreading sequences which presents the signature

Challenges in CD-NOMA

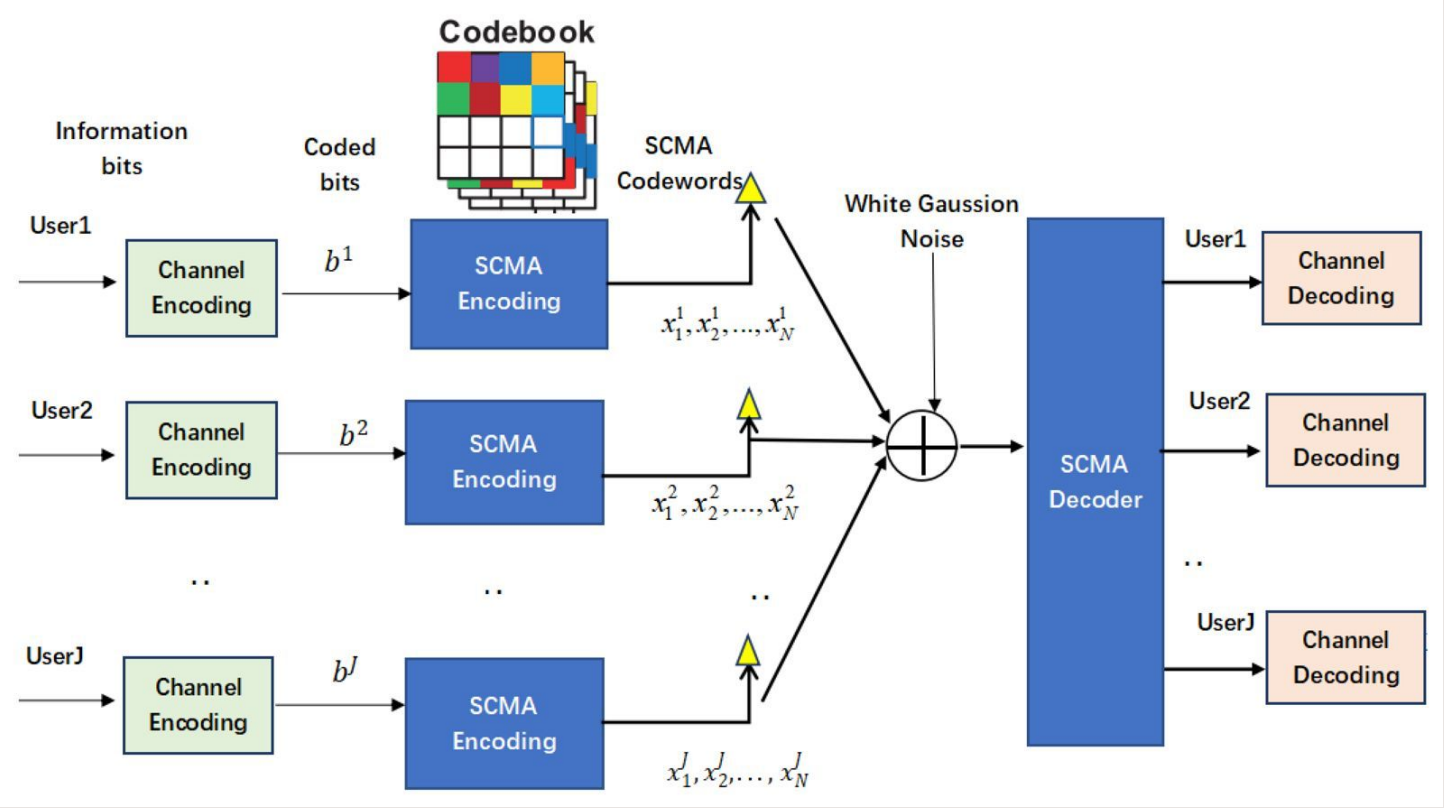
HIGH TIME COMPLEXITY

SIGNIFICANT ENERGY REQUIREMENTS FOR DECODING ALGORITHMS

SCMA

Sparse Code Multiple Access

- A CD-NOMA technique.
- Bit <---> Constellation Mapping + Low Density Spreading = Bit <---------> Different Sparse Codewords
- Outperforms PD-NOMA



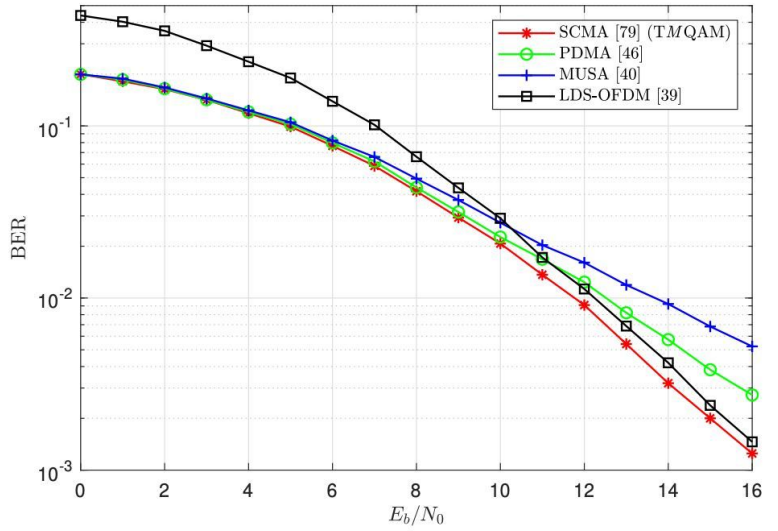


Figure 5. Performance comparison of LDS-CDMA, MUSA, PDMA and SCMA, in terms of BER, through Rayleigh fading channel : the number of orthogonal REs is 4 and the number of users is 6.

Existing Literature

Sparse Code Multiple Access

- Hardware Design and Implementation of Sparse Code Multiple Access : Applies a fast convergence message passing algorithm and proposes a unified quantization scheme based on density evolution optimization. Performs both encoding and decoding.
- Efficient Sparse Code Multiple Access Decoder Based on Deterministic Message Passing Algorithm : Implements deterministic message passing algorithm. Implements decoding using various techniques on the FPGA and show BER vs SNR ratio and resource optimizations
- Grant-Free Sparse Code Multiple Access for Uplink Massive Machine-Type Communications and Its Real-Time Receiver Design
- Performance Characterization of an SCMA Decoder
- Toward High-Performance Implementation of 5G SCMA Algorithms

Proposed Project

- Provide a hardware implementation of SCMA decoder.
- Offload bottleneck tasks to FPGA (Field-Programmable Gate Array)
- Reduce time complexity and resource utilization with hardware optimizations on the FPGA.

Expected outcome

- FPGA implementation of SCMA
- Enhanced overall performance of CD-NOMA decoding for 6G

Timeline

10th September, 2024

Understanding SCMA Algorithm.

Midsem (3-11 Oct) Evaluation

First draft of algorithm ready to run on processor.

Optimize the code.

Report bottlenecks in code.

Find which part of algorithm to be offloaded on FPGA

20th October, 2024

First draft of hardware code (HLS).

Running it on FPGA to get the readings.

Comparing results of FPGA & Processor

Endsem (4-12 Dec) Evaluation

Running final optimized code on FPGA & comparing the results with the literature

Reporting the final readings:-

$T_{execution}$,

Resource Utilization,

$P_{consumption}$