LAB ASSESSMENT -1

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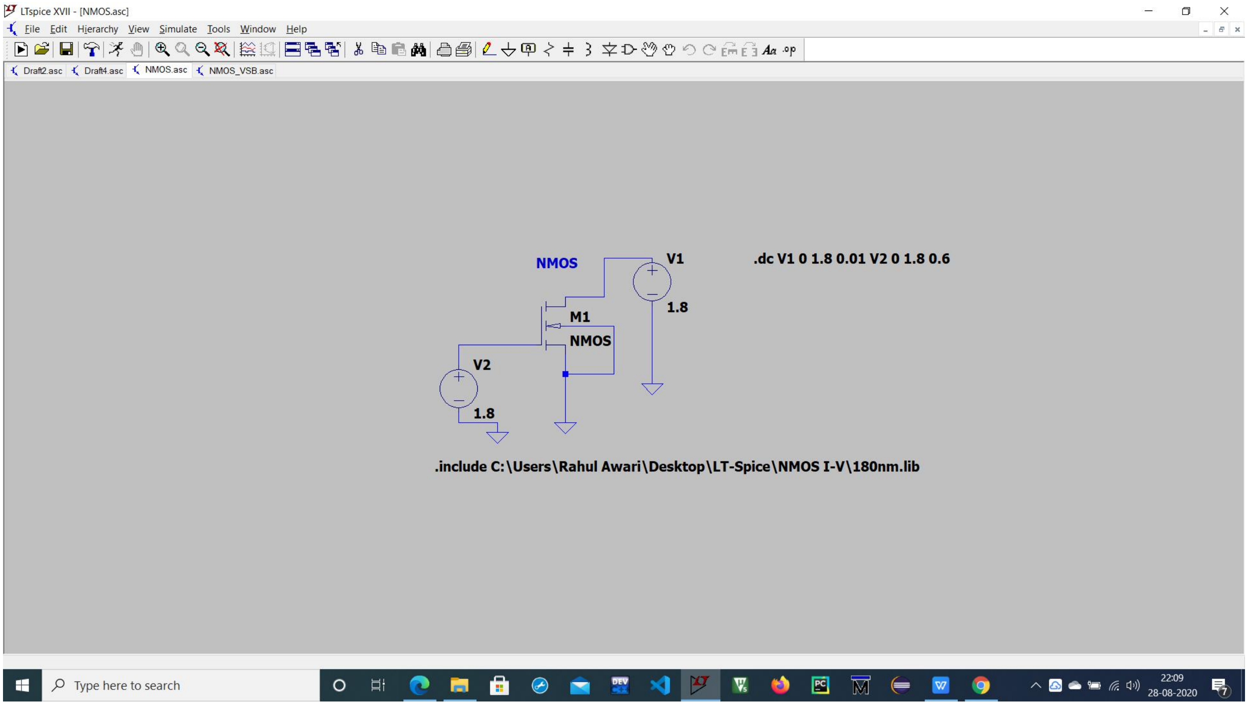
SUBJECT : VLSI SYSTEM DESIGN (ECE3002-ELA)
SLOT : L43 + L44
FACULTY : PROF. JAGANNADHA NAIDU K

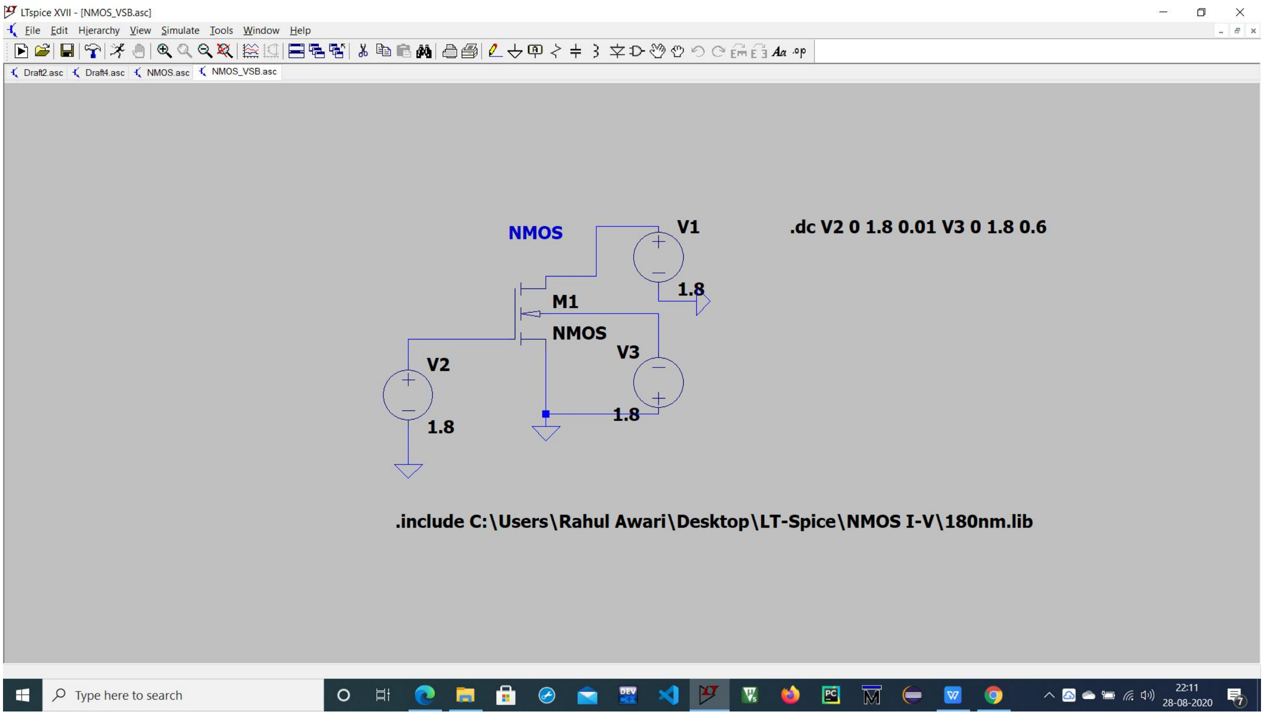
NMOS

AIM:- To calculate and plot following for NMOS and PMOS.

1) **Plot Ids vs Vds with variable Vgs**
2) **Calculate Channel length modulation.**
3) **For Plot of Ids vs Vgs calculate I(reference) ,reference current**
4) **Plot Ids vs Vgs for variable Vsb**

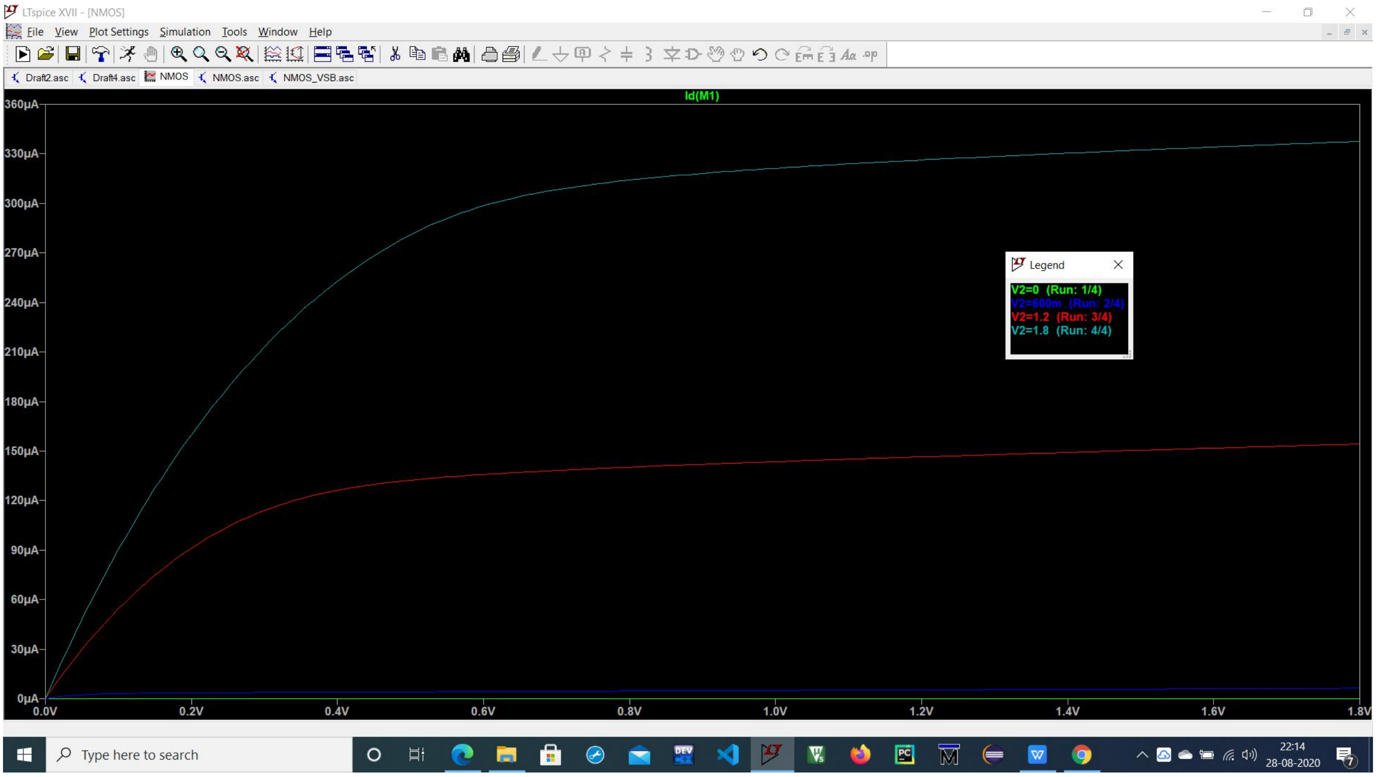
Schematic:-



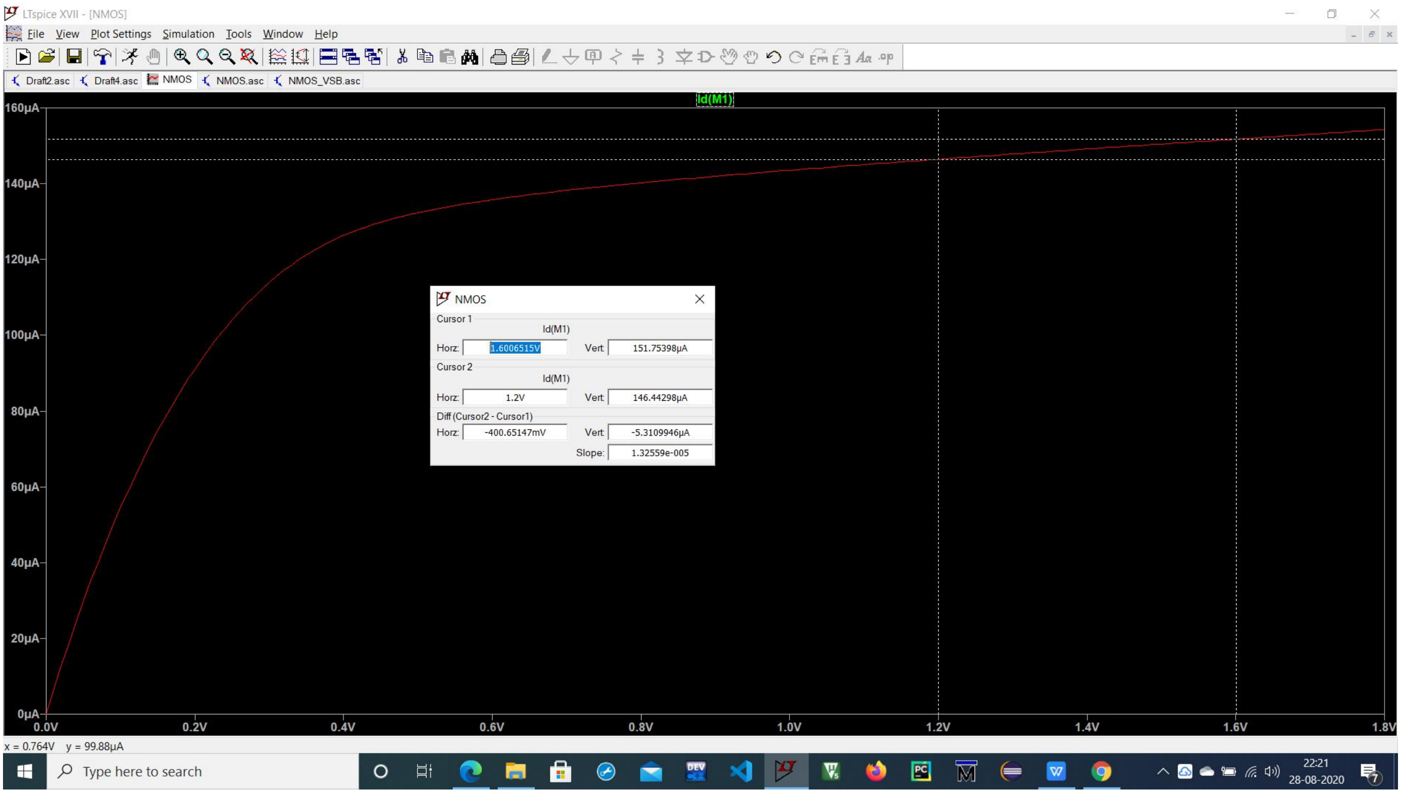


GRAPHS:-

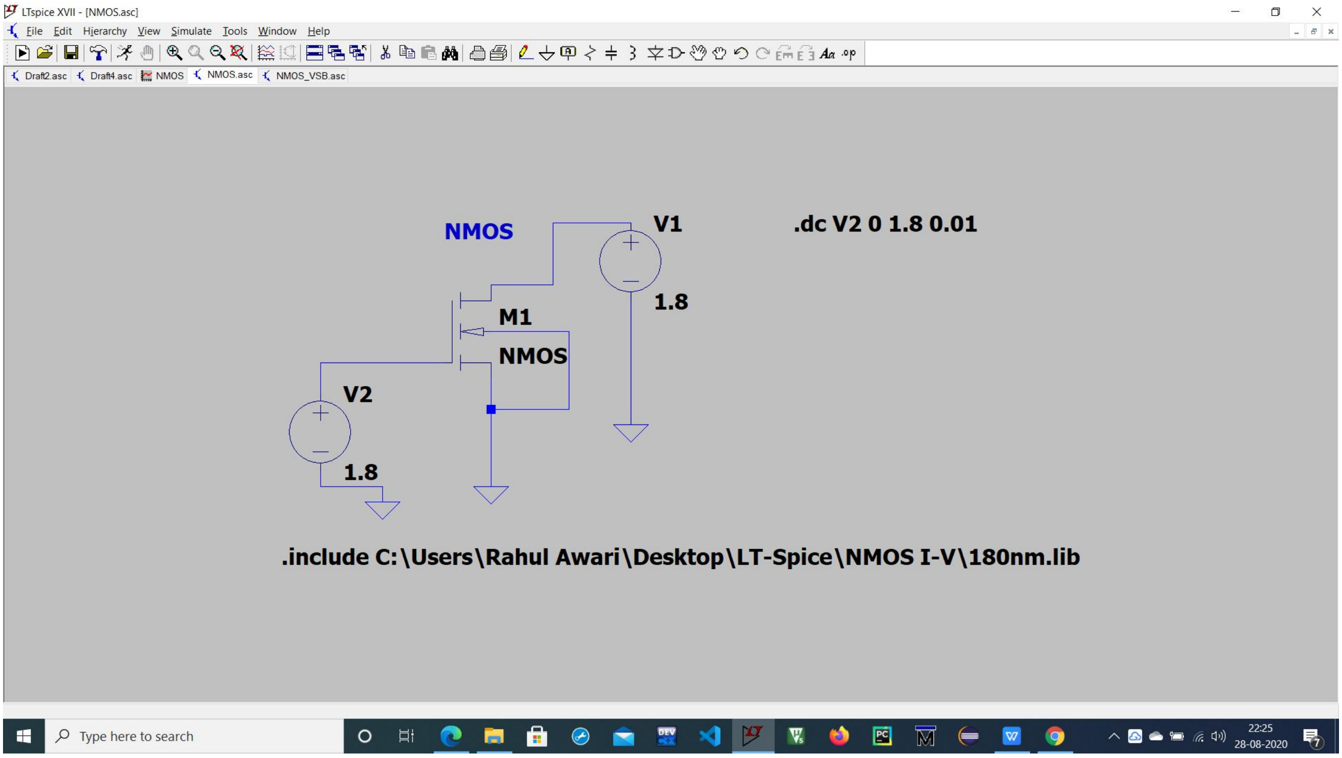
1) Plot Id vs Vds (with Vgs (0→1.8V) with interval of 0.6V)

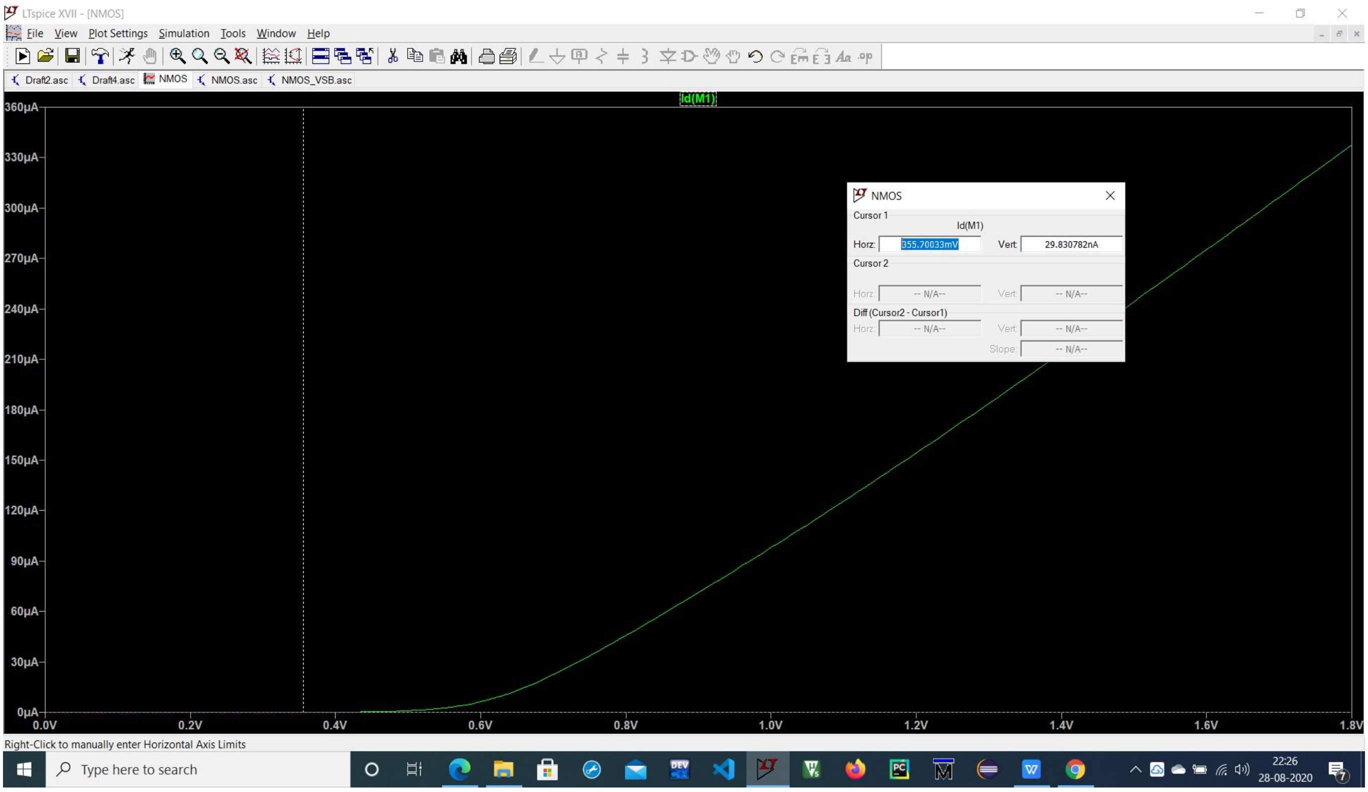


2) To Plot and find Ids1 and Ids2 at Vds1=1.6V and Vds2=1.2V for Vgs=1.2V



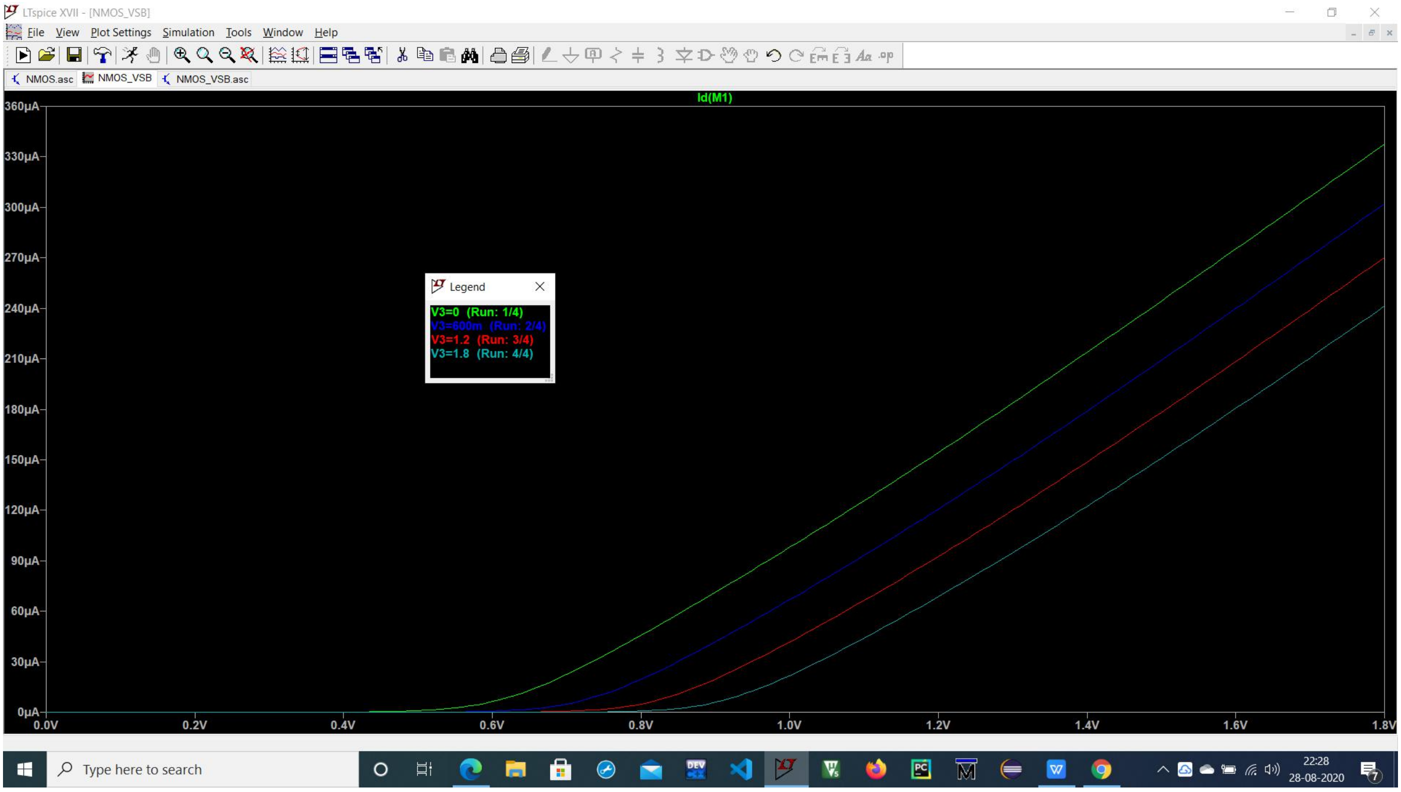
3) For calculating I reference(reference current) for Vth0 at 355mV





4) Plot for Ids vs Vgs for Vsb(0→1.8V) at interval of 0.6V

Graph:-



CALCULATIONS FOR NMOS:-

Vth0=355mV

Vdsat=Vgs-Vth0

Table for Vgs and Vdsat:-

Vgs	Vdsat
0.6V	0.245V
1.2V	0.845V
1.8V	1.445V

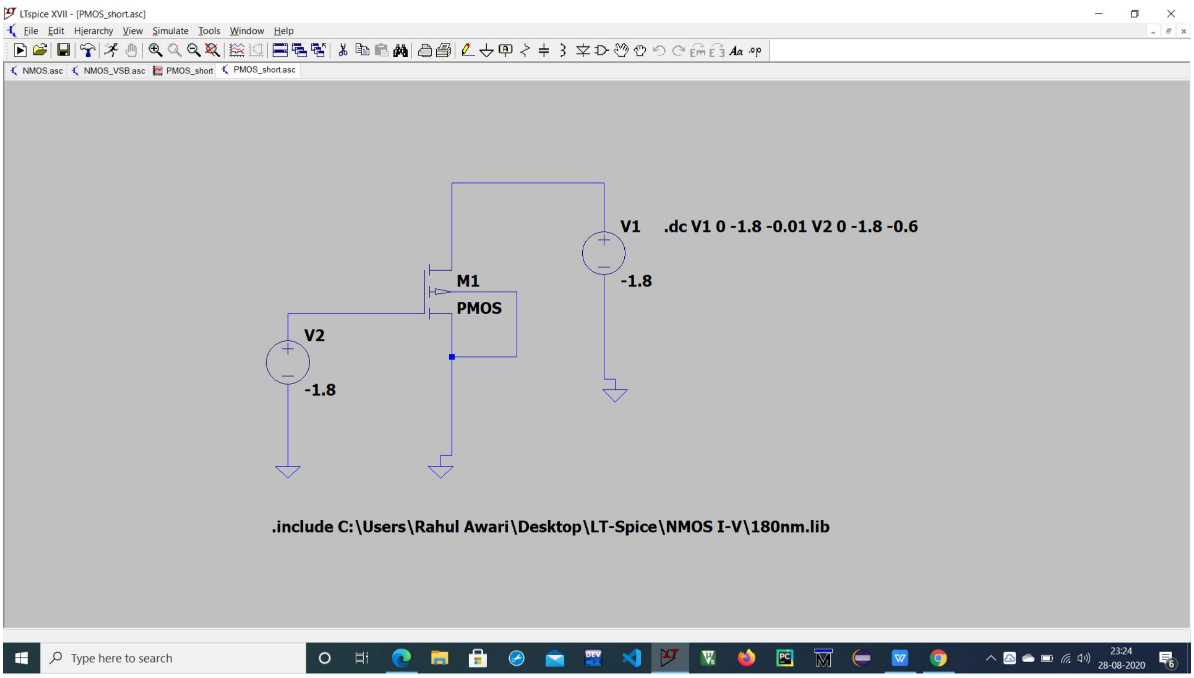
For Channel length modulation Calculation:-
Vds1=1.2V
Vds2=1.6V
Ids2=151.753uA
Ids1=146.442uA
λ = 0.1017
I reference = 29.830nA

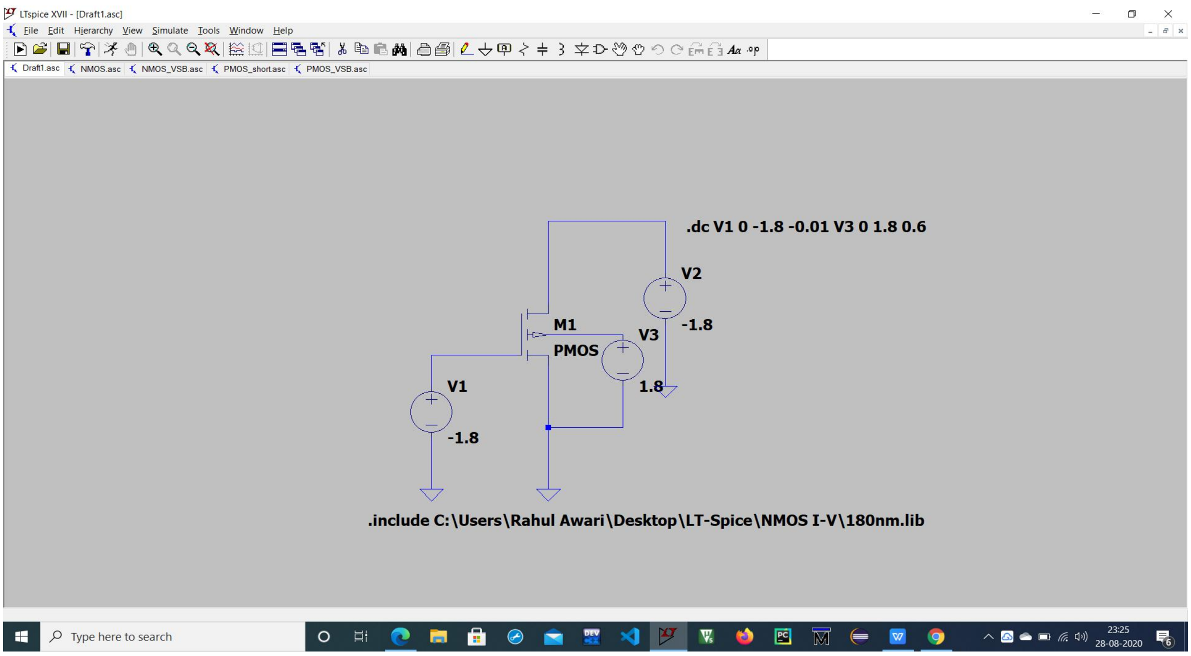
Table:-Vt for Vsb>0 by using Iref

Vsb	Vth
0V	355.700mV
0.6V	484.690mV
1.2V	591.205mV
1.8V	684.039mV

PMOS

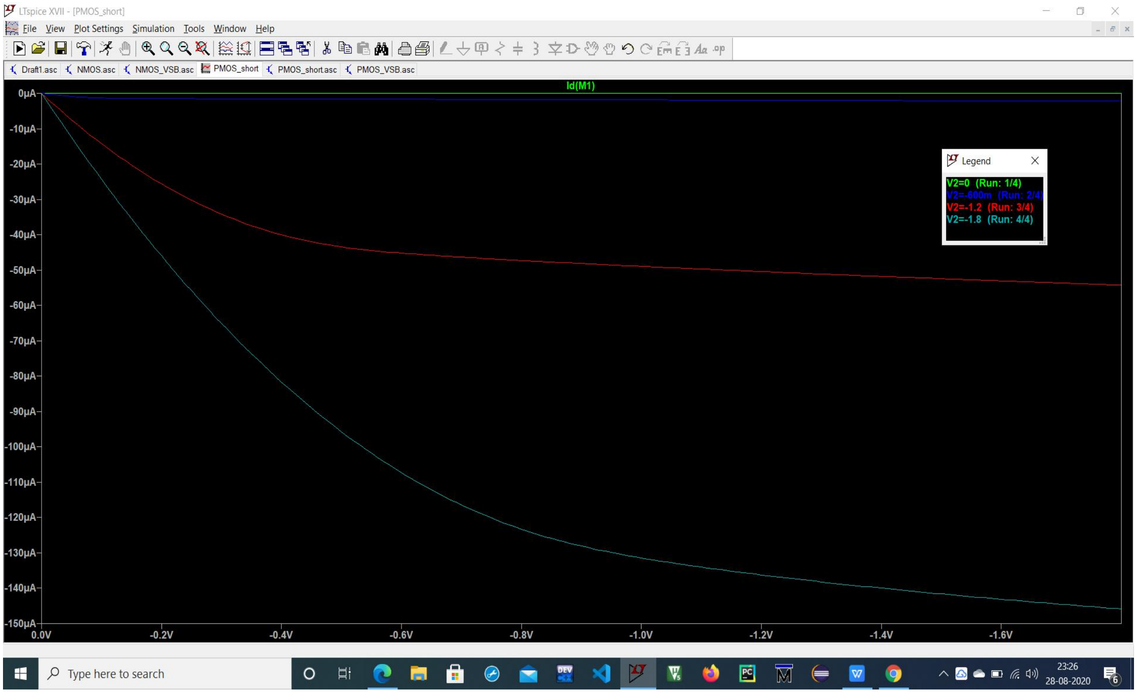
SCHEMATIC:-



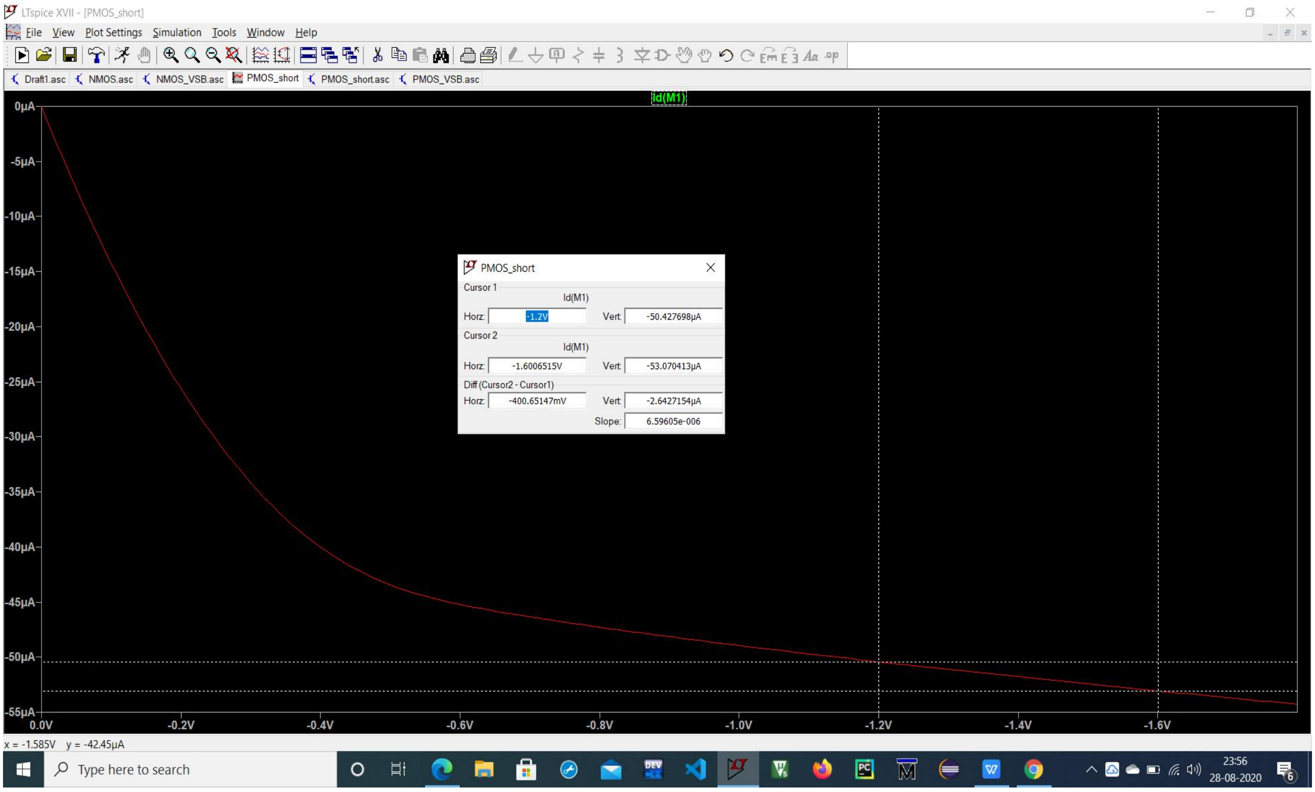


GRAPHS:-

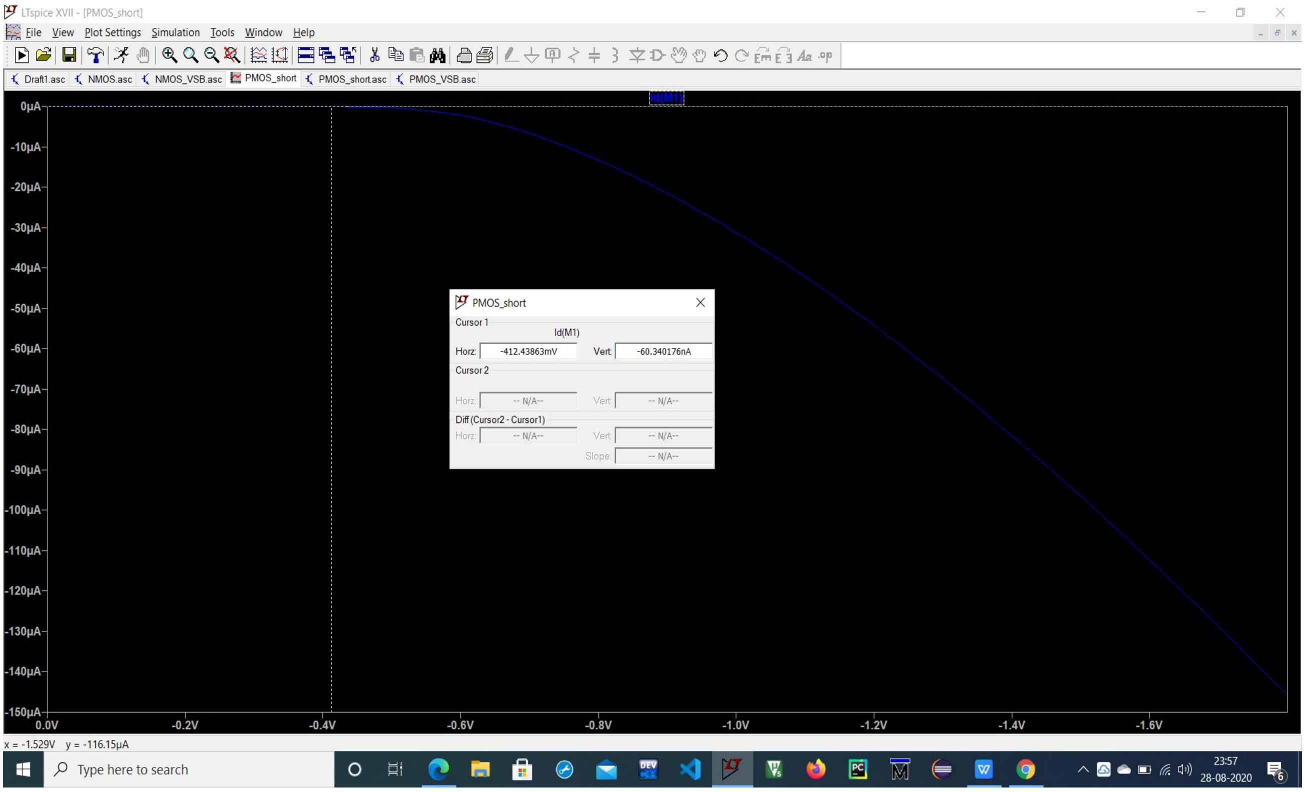
Screen Shot:-

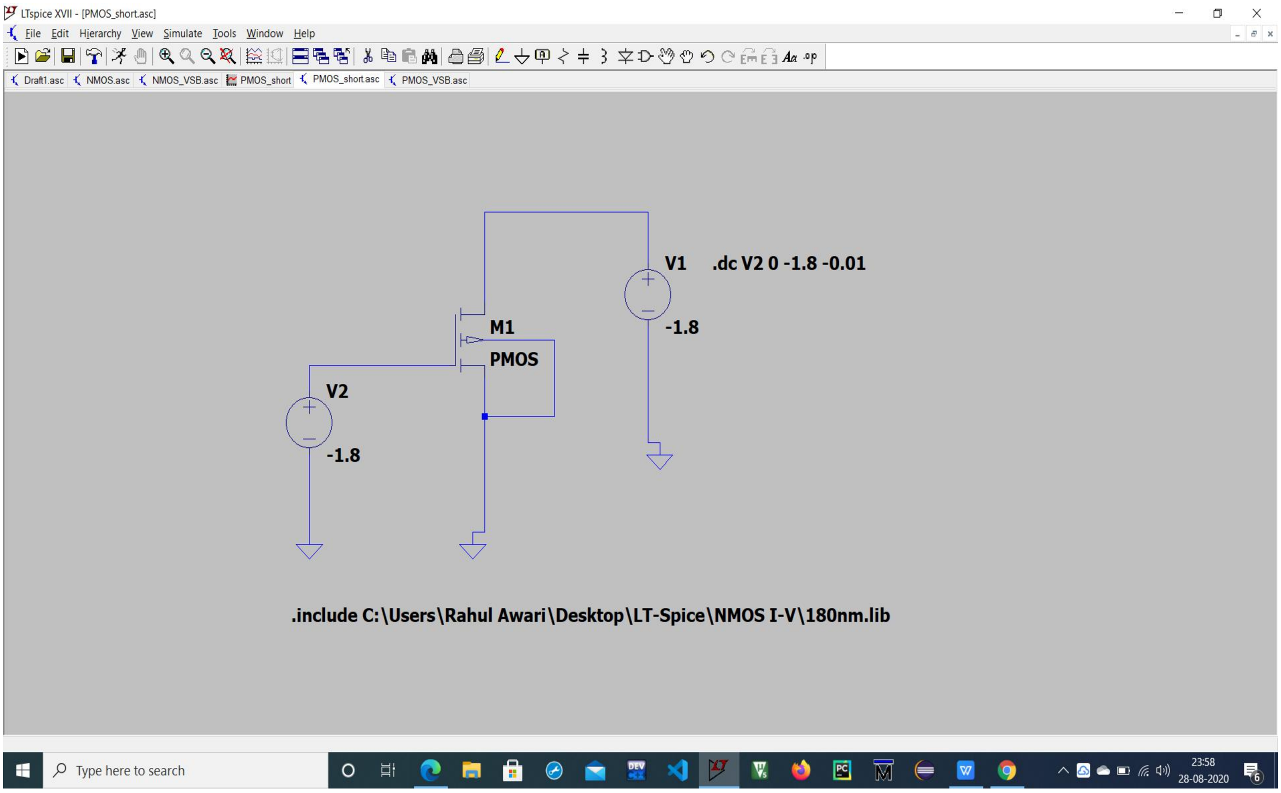


2) To Calculate channel Length modulation Vds1 =-1.2V and Vds2=-1.6V for Vgs=1.2V

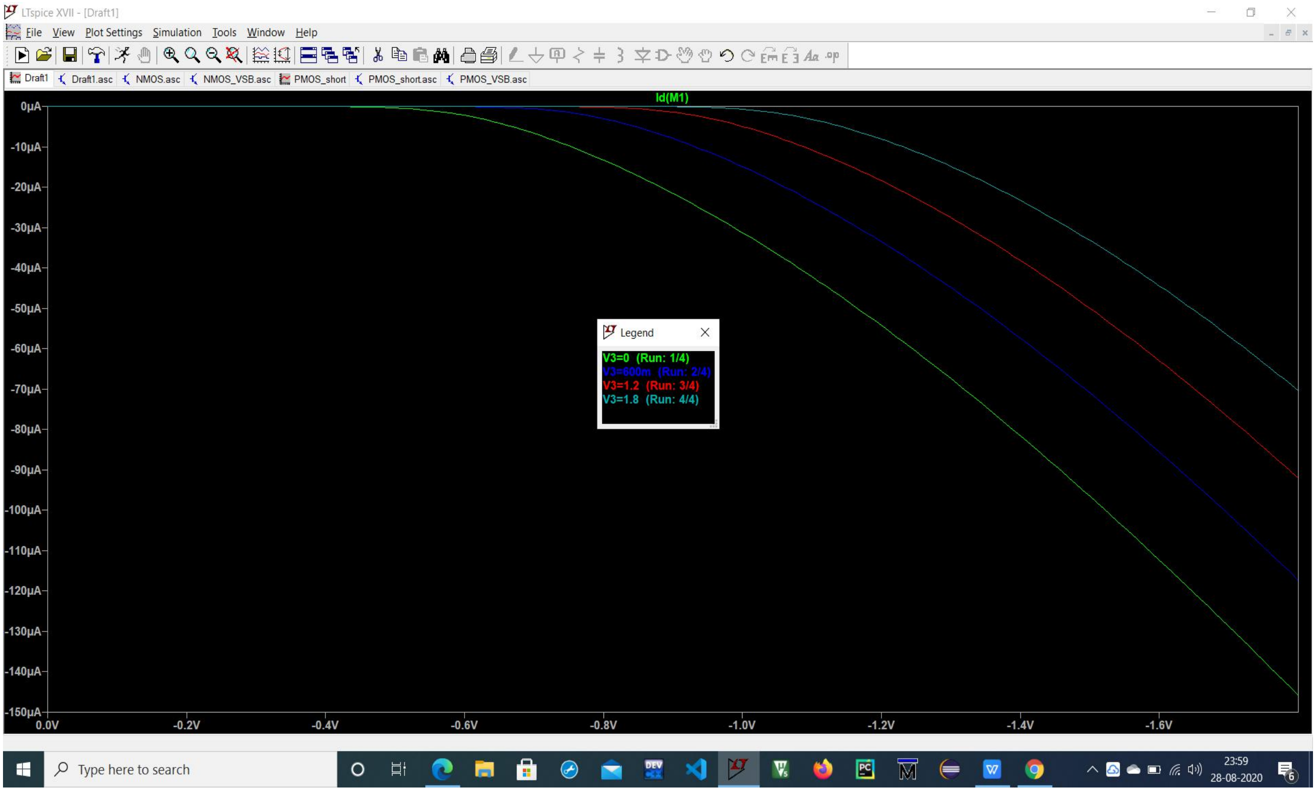


3) To plot Iref(reference current) with vtp=-412.43mV





4) To Plot Ids Vs Vgs for Vsb(0→-1.8V) at interval of -0.6V



Calculations for PMOS:-

Vtp=-0.412V

Table for Vgs and Vdsat:-

Vgs	Vdsat
-0.6V	-0.188V
-1.2V	-0.788V
-1.8V	-1.388V

For Calculation of Channel length modulation:-
Vds1=-1.2V
Vds2=-1.6V
Ids1=-50.427uA
Ids2=--53.070uA
λ=0.1562
I reference=-60.34nA

Table of Vt for different Vsb:-

Vsb	Vt
0V	-412.43mV
-0.6V	-594.10mV
-1.2V	-750.48mV
-1.8V	-891.20mV

Inference for Both PMOS and NMOS:-

1) Length:-180n and Width=500n is for both NMOS and PMOS.

2) Vthn and Vthp is observed for both NMOS and PMOS which is required for ploting and calculation of I reference.

3) Vdsat = Vgs-Vthn is calculated for observing cutoff, saturation and linear region in Id Vs Vds graph.For NMOS with Vgs=1.2V,Vds-1.2V,1.6V were taken for calculation and similarily for PMOS.

4) Vdsat is observed for PMOS and NMOS and for calculation of channel length modulation Vds1 and Vds2 is taken from both saturation region of graph of Id vs Vds.

5) Vds1,Vds2,Id1,Id2 are used to calculate channel length modulation.

6) The I reference obtained at Vthn and Vthp, is used to obtain Vt for different Voltage and curve of Vsb where initially source to body voltage is observed to be 0V.

7) The body effect of NMOS i.e. plot of Ids vs Vgs as over different value of Vsb is plotted and the value of threshold voltage for different Vsb values are tabulated. The voltage difference between the source and the bulk, Vsb changes the width of the depletion layer and therefore also the voltage across the oxide due to the change of the charge in the depletion region

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8) The transfer characteristic is the drain current (Ids) response to the input gate-source voltage (Vgs). Since the gate terminal is electrically isolated from the remaining terminals the gate current is zero, so that gate current is not part of device characteristics.