LAB ASSESSMENT -2

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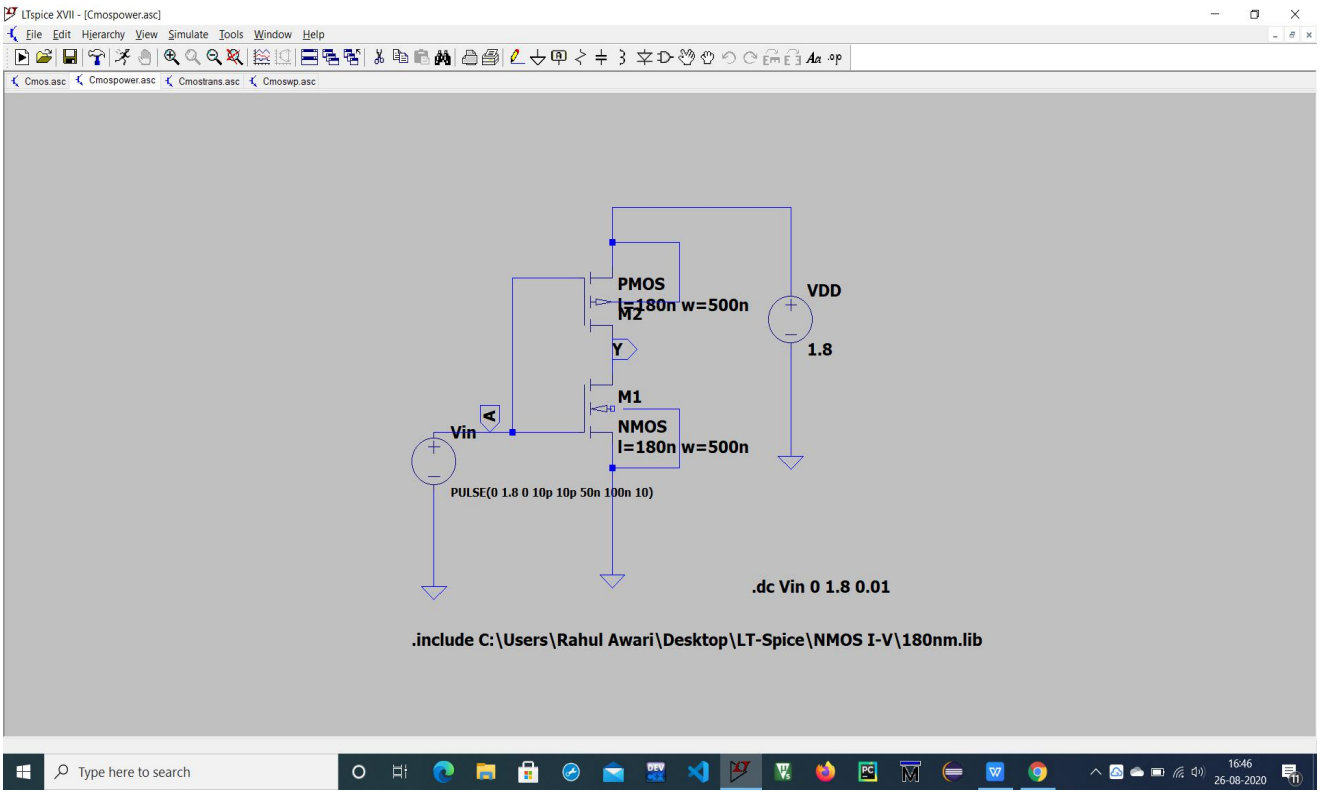
REGISTER NUMBER: 18BEC2014
SUBJECT : VLSI SYSTEM DESIGN (ECE3002-ELA)
SLOT : L43 + L44
FACULTY : PROF. JAGANNADHA NAIDU K

CMOS INVERTER

AIM:

1) To Plot DC Analysis of CMOS Inverter.
2) To Plot DC Analysis with variable width of PMOS.
3) To plot the Transient analysis and to calculate the propagation delay.
4) To plot and Calculate Average Power.

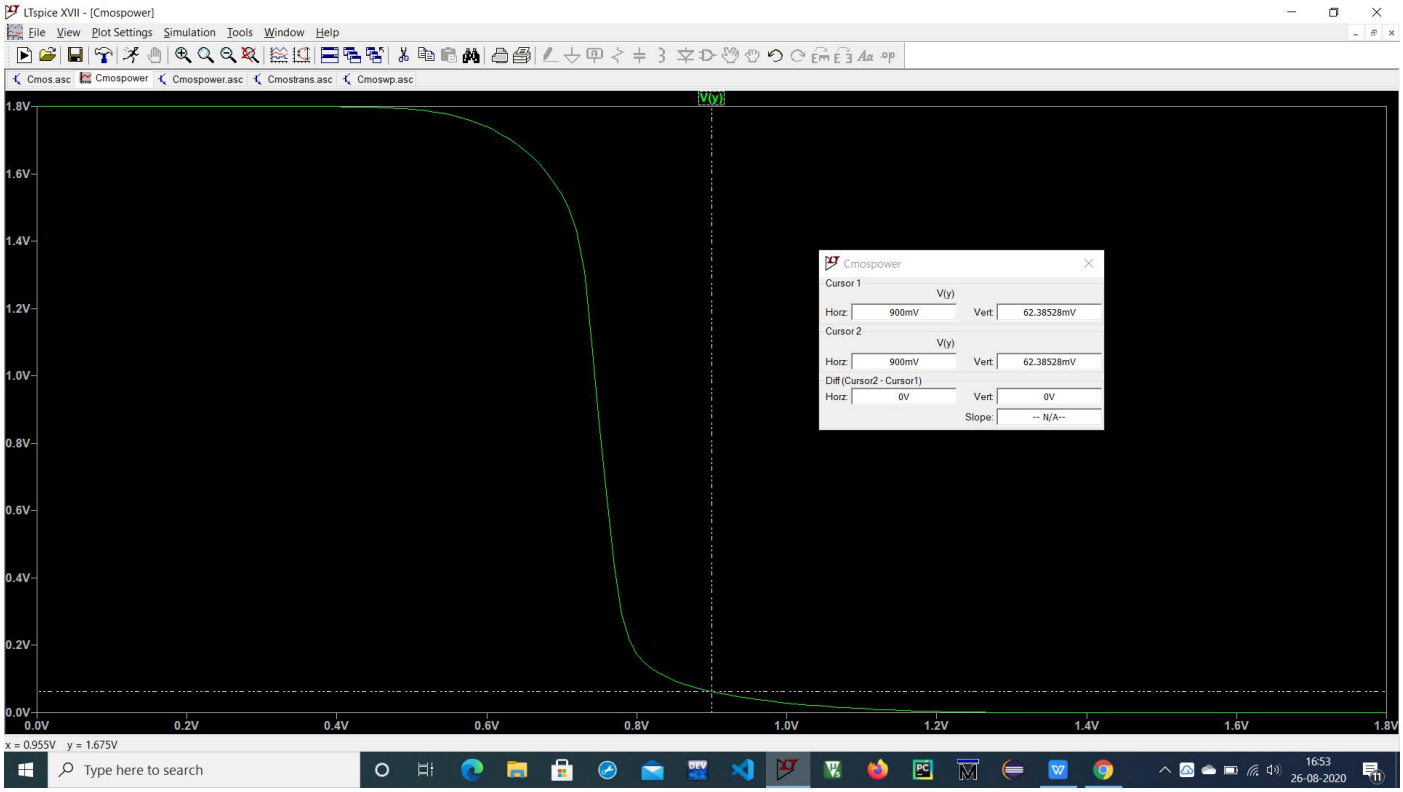
SCHEMATIC:



GRAPHS:-

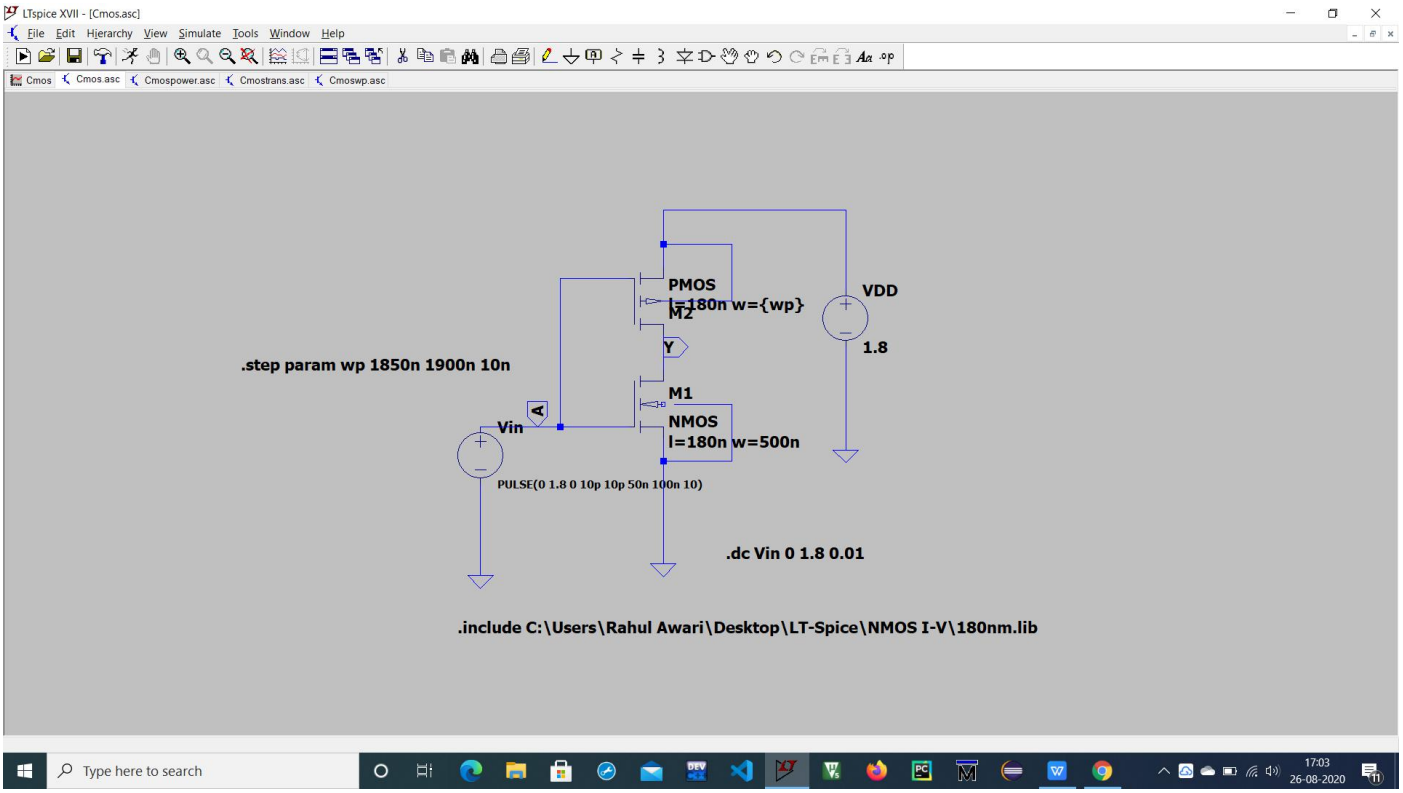
1) To plot Transfer characteristics of CMOS Inverter.
   a) PMOS :- length=180n,Width=500n
   b) NMOS:- length=180n,Width=500n
   c) Vin - pulse
   d) Vdd- 1.8V

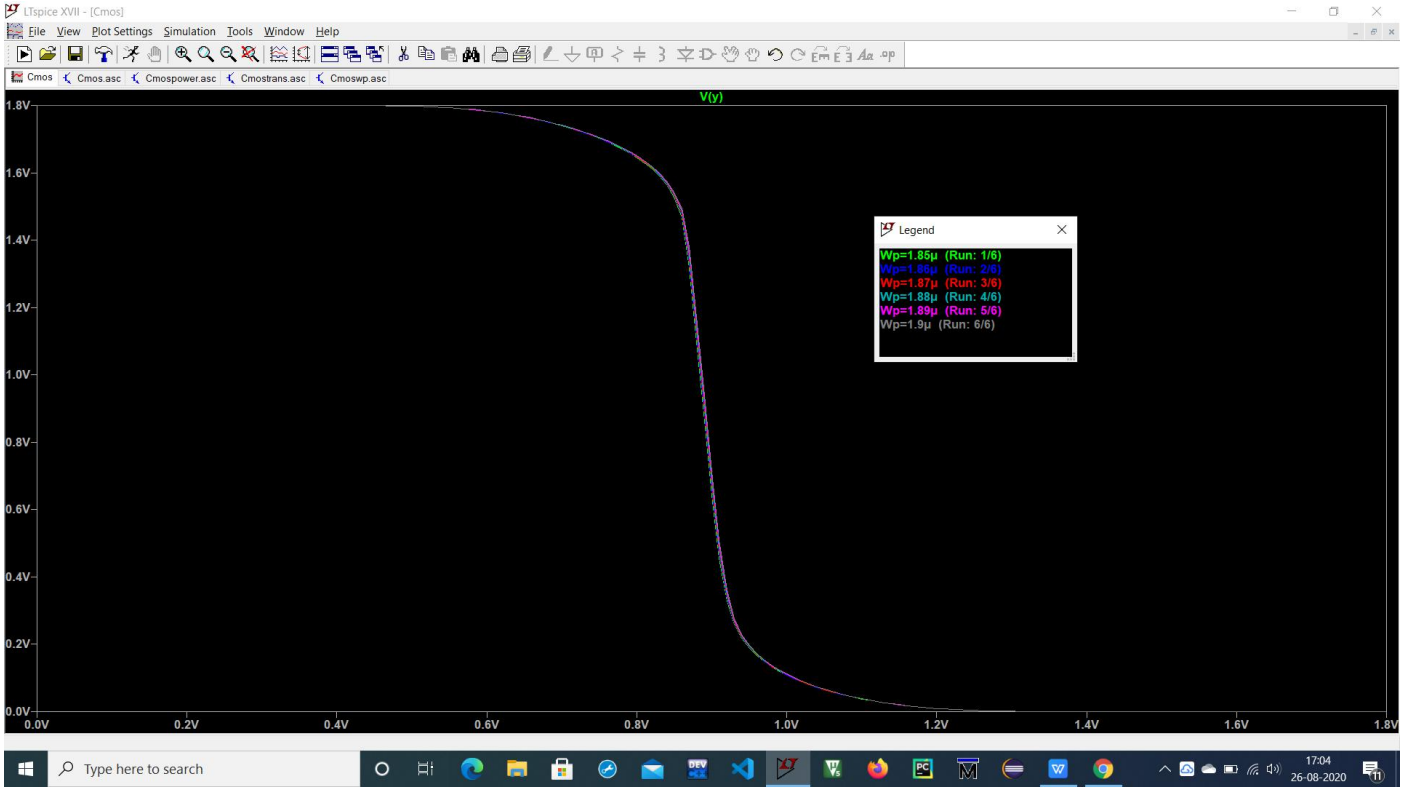
   Screen Shot:-

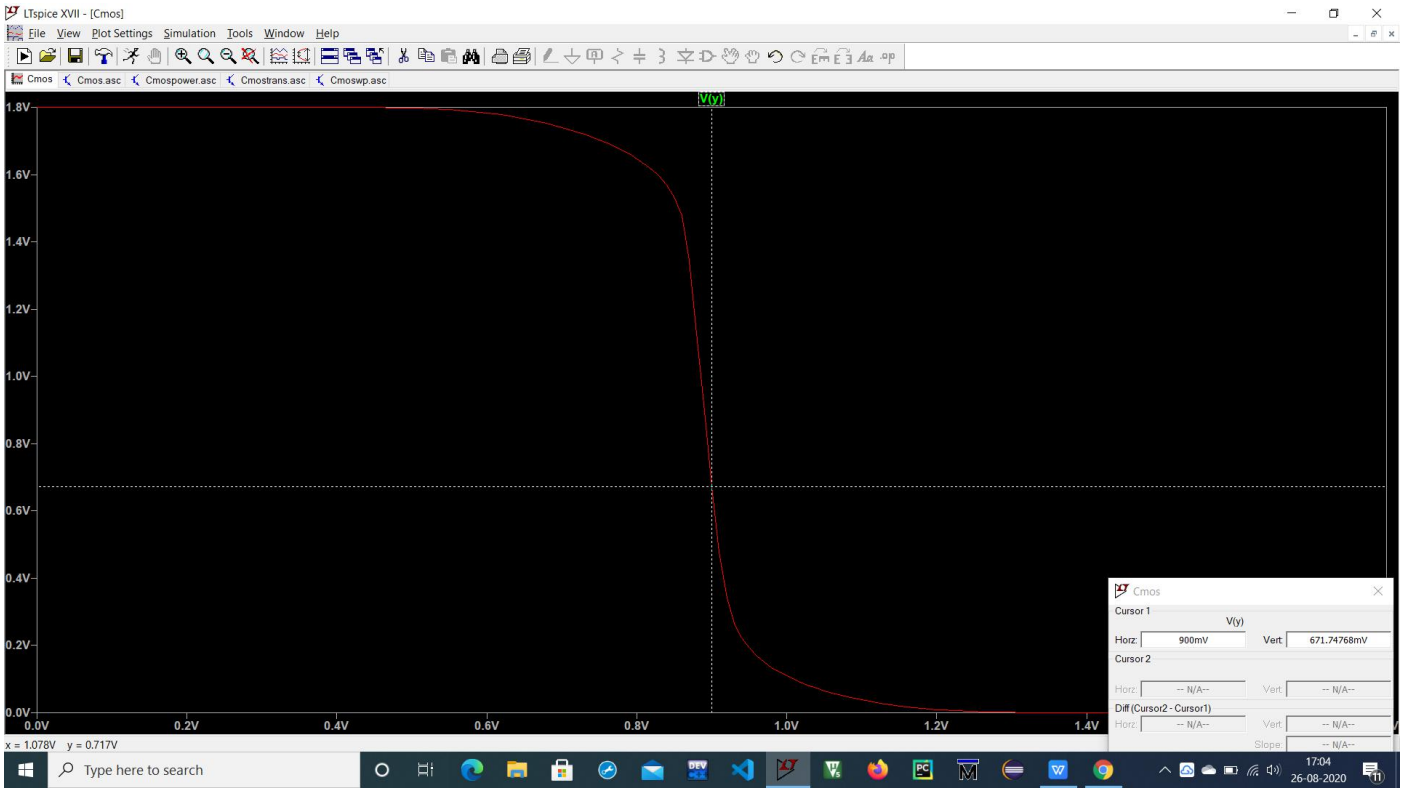


2) To Plot DC Analysis with variable width of PMOS.
   a)PMOS :- length=180n,Width={wp}(1850n,1900n,10n)
   b)NMOS:- length=180n,Width=500n
   c)Vin-pulse
   d)Vdd-1.8v

Screen Shot:-


LTspice XVII - [Cmos.asc]
File Edit Hierarchy View Simulate Tools Window Help
Cmos Cmos.asc Cmospower.asc Cmostrans.asc Cmoswp.asc
PMOS
l=180n w={wp}
M2
VDD
1.8
Y
.step param wp 1850n 1900n 10n
M1
NMOS
l=180n w=500n
Vin
PULSE(0 1.8 0 10p 10p 50n 100n 10)
.dc Vin 0 1.8 0.01
.include C:\Users\Rahul Awari\Desktop\LT-Spice\NMOS I-V\180nm.lib
Type here to search
17:03
26-08-2020


LTspice XVII - [Cmos]
File View Plot Settings Simulation Tools Window Help
Cmos Cmos.asc Cmospower.asc Cmostrans.asc Cmoswp.asc
V(y)
1.8V
1.6V
1.4V
1.2V
1.0V
0.8V
0.6V
0.4V
0.2V
0.0V
0.0V 0.2V 0.4V 0.6V 0.8V 1.0V 1.2V 1.4V 1.6V 1.8V
Legend
Wp=1.85µ (Run: 1/6)
Wp=1.86µ (Run: 2/6)
Wp=1.87µ (Run: 3/6)
Wp=1.88µ (Run: 4/6)
Wp=1.89µ (Run: 5/6)
Wp=1.9µ (Run: 6/6)
Type here to search
17:04
26-08-2020



3) To plot the Transient analysis and to calculate the propagation delay.

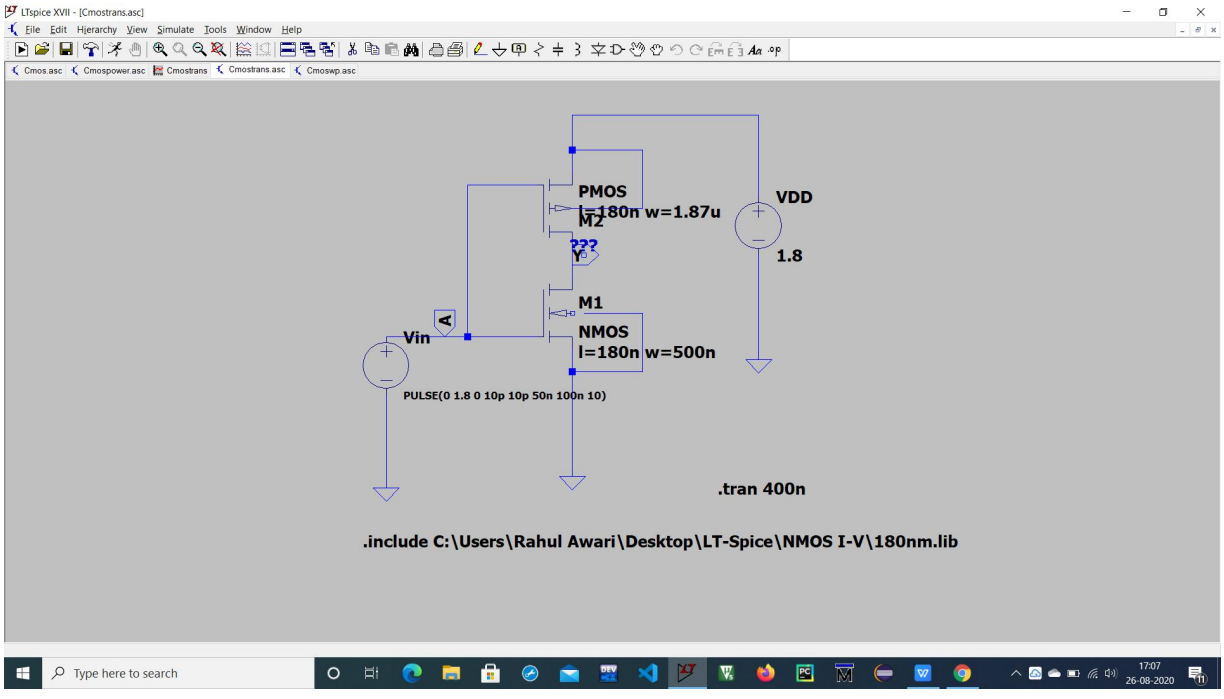
a)PMOS :- length=180n,Width=1.87u

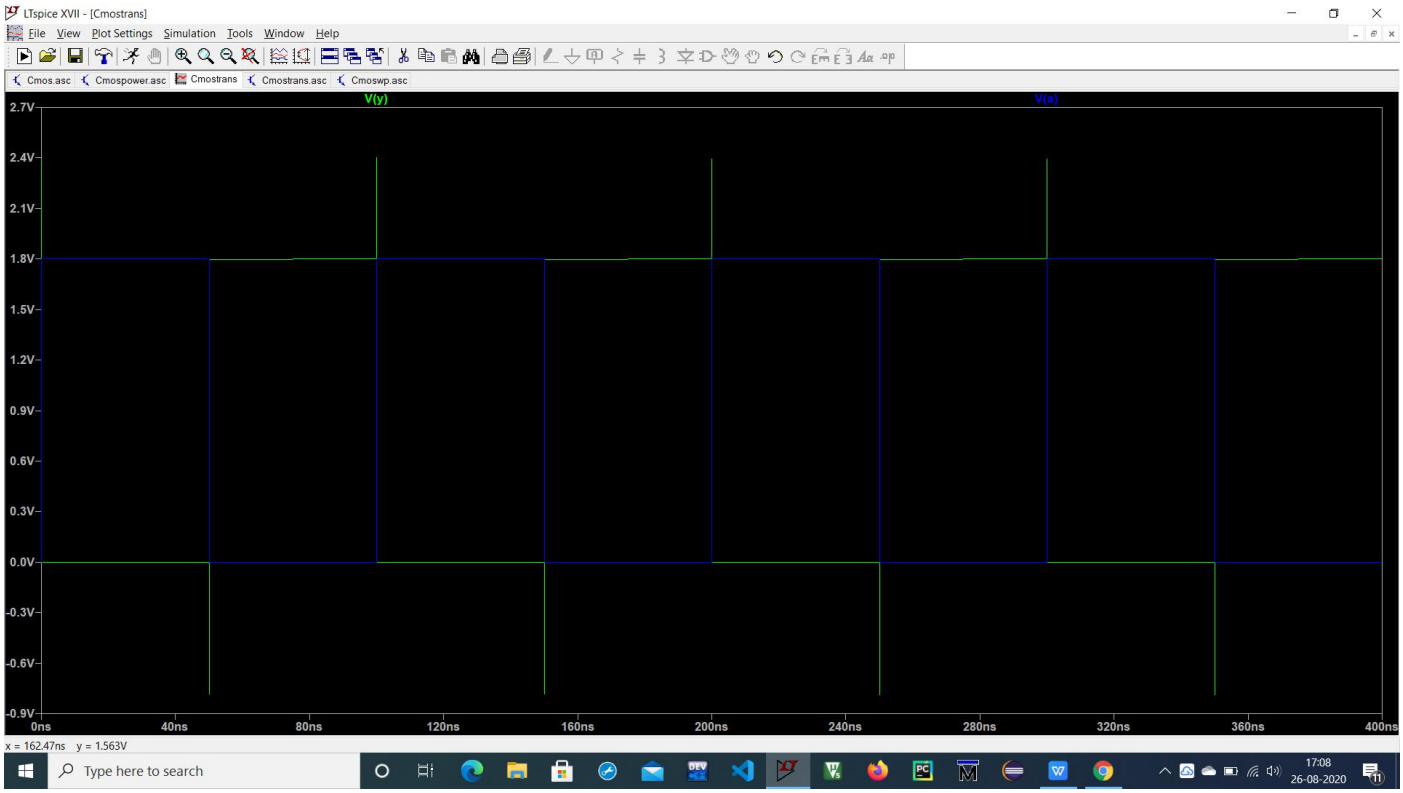
b)NMOS:- length=180n,Width=500n

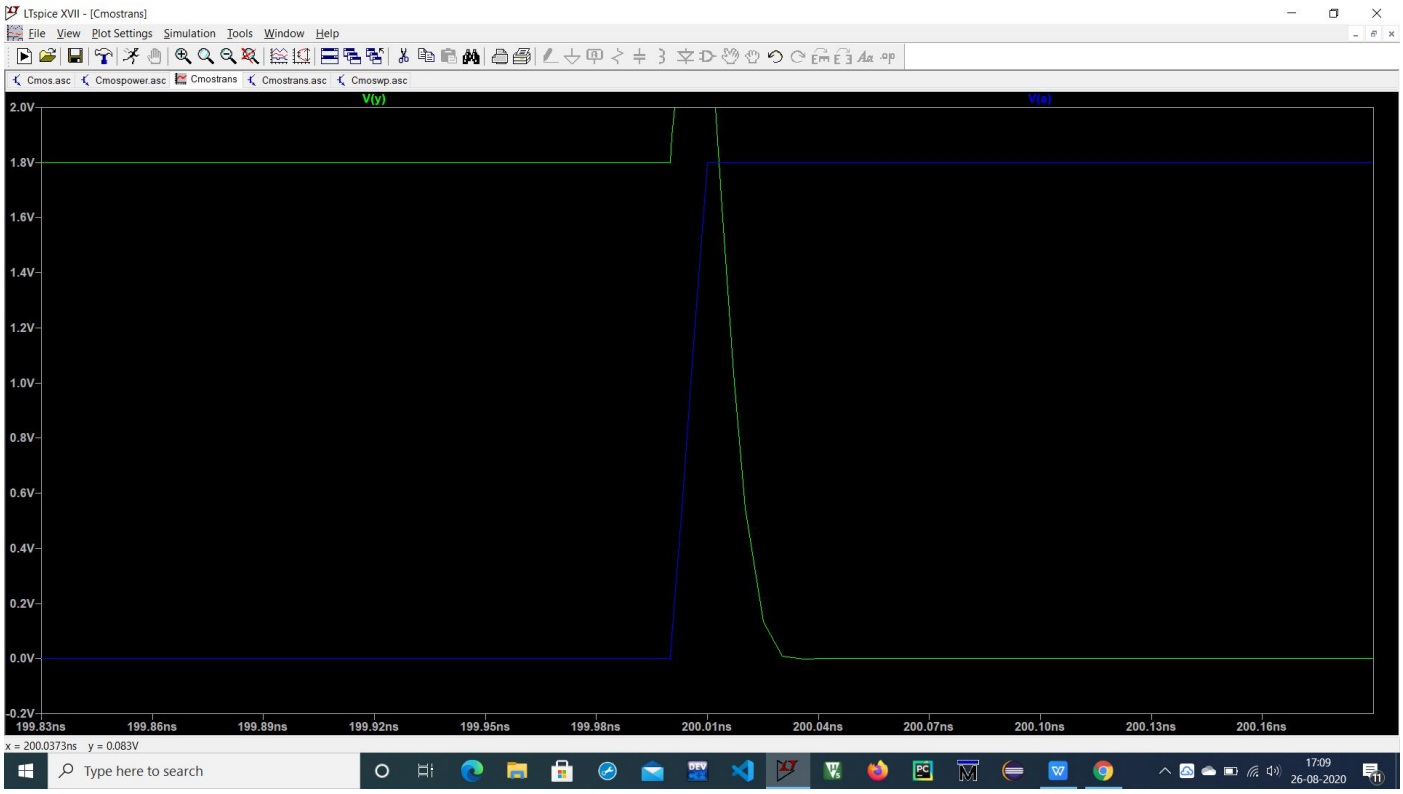
c)Vin-pulse

d)Vdd-1.8v

Screen Shot:-

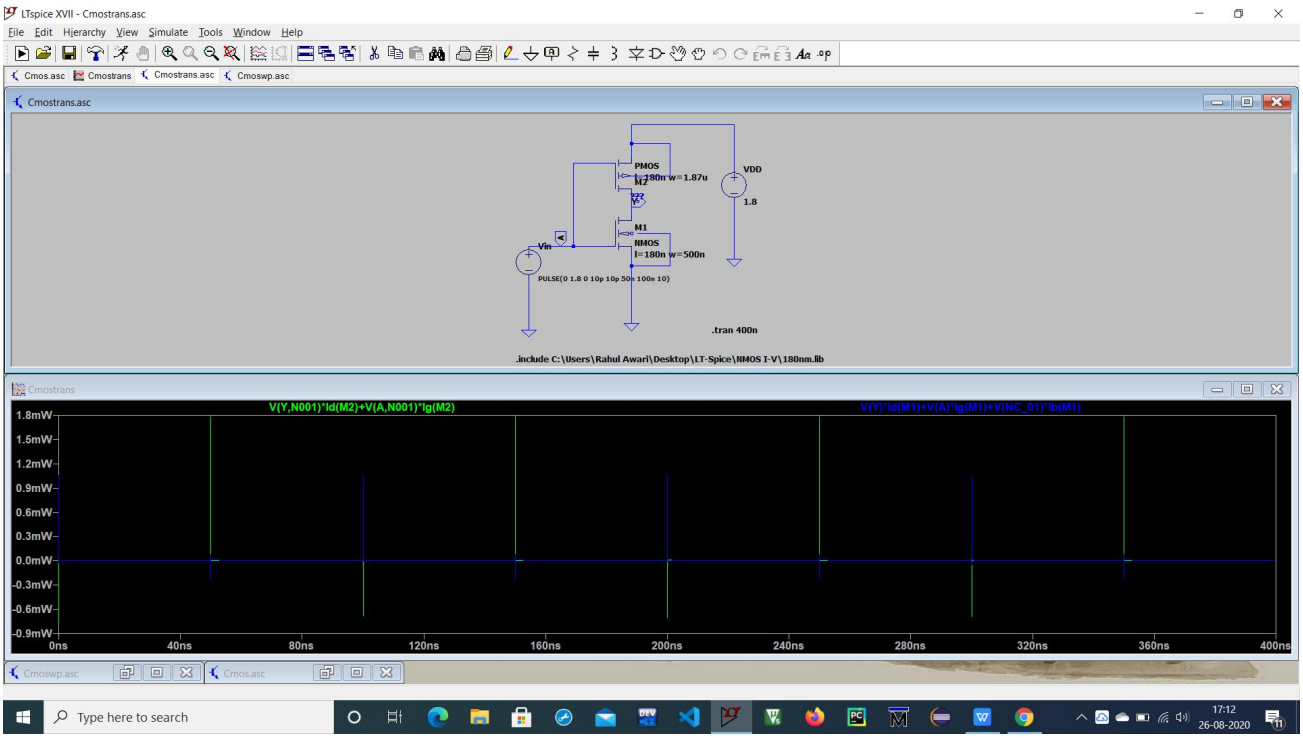


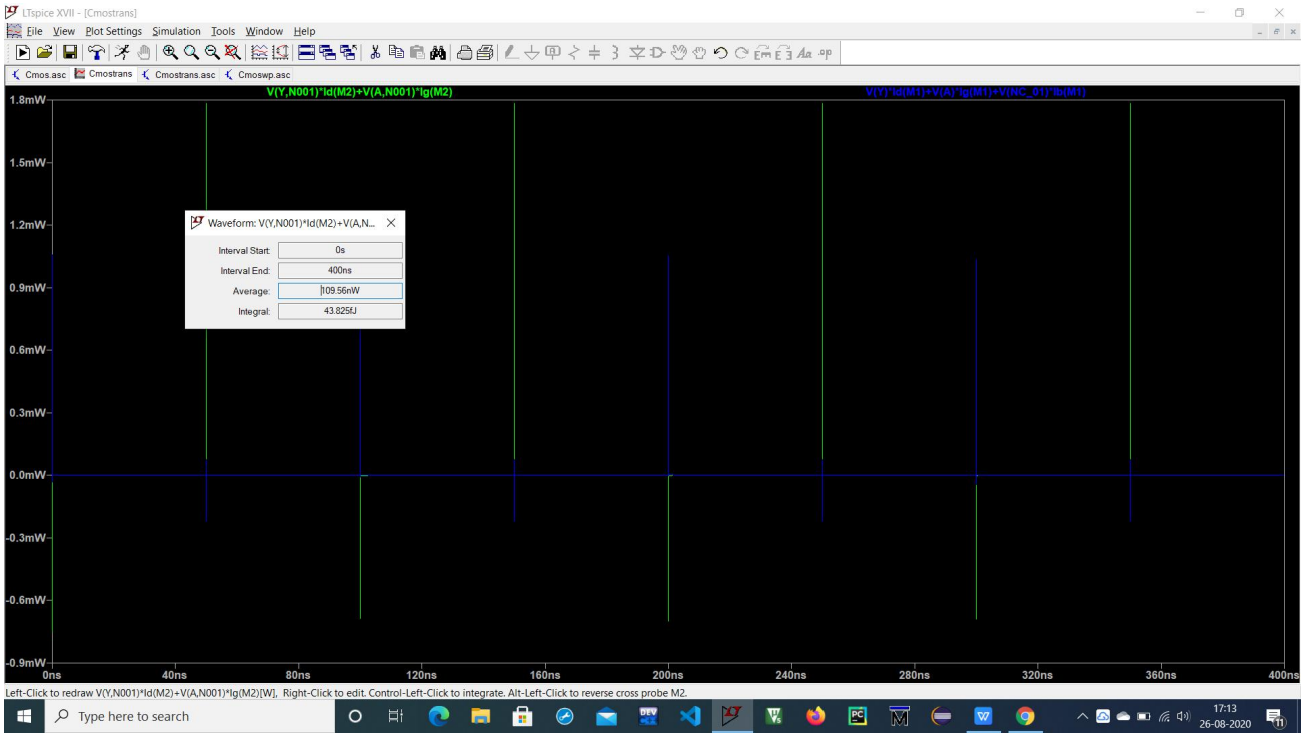

LTspice XVII - [Cmostrans]
File View Plot Settings Simulation Tools Window Help
Cmos.asc Cmospower.asc Cmostrans Cmostrans.asc Cmoswp.asc
V(y)
V(a)
2.7V
2.4V
2.1V
1.8V
1.5V
1.2V
0.9V
0.6V
0.3V
0.0V
-0.3V
-0.6V
-0.9V
0ns 40ns 80ns 120ns 160ns 200ns 240ns 280ns 320ns 360ns 400ns
x = 162.47ns y = 1.563V
Type here to search
17:08
26-08-2020


LTspice XVII - [Cmostrans]
File View Plot Settings Simulation Tools Window Help
Cmos.asc Cmospower.asc Cmostrans Cmostrans.asc Cmoswp.asc
V(y)
V(a)
2.0V
1.8V
1.6V
1.4V
1.2V
1.0V
0.8V
0.6V
0.4V
0.2V
0.0V
-0.2V
199.83ns 199.86ns 199.89ns 199.92ns 199.95ns 199.98ns 200.01ns 200.04ns 200.07ns 200.10ns 200.13ns 200.16ns
x = 200.0373ns y = 0.083V
Type here to search
17:09
26-08-2020

4) To plot and Calculate Average Power.
   a)PMOS :- length=180n,Width=1.87u
   b)NMOS:- length=180n,Width=500n
   c)Vin-pulse
   d)Vdd-1.8v

   Screen Shot:-





CALCULATIONS:

1) DC Analysis:-
   Horizontal - 62.93mV
   Vertical(Vin)-900mV

2) Voltage at which Vout=Vin for variable wp.
   Wp=1.87u

3) Falling (tpdf) =10.95ps
   Rising (tpdr) = 13.03 ps
   Avg Delay = 12.15ps

4) Avg PMOS Power:- 109.554nW
   Avg NMOS Power:-88.57nW.

INFERENCE:

1) The CMOS inverter consists of a PMOS and an NMOS.

2) Pulse Voltage is used with following input :-
a) V1=0
b) V2=1.8
c) Tdelay=0
d) Trise=10p
e) Tfall=10p
f) Ton=50n
g) Tperiod=100n
h) Ncycles=10.

3)For variable width of wp , wp=1.87u is observed to be width of NMOS at which Horizontal voltage is same as Vertical Voltage.

4)Doing transient analysis, we calculated the propagation delay from the input and output signal at the rising edge and falling edge of both the signal.For delay propagation time is calculated at which horizontal voltage is Vdd/2 for both input and output for both rising and falling output .

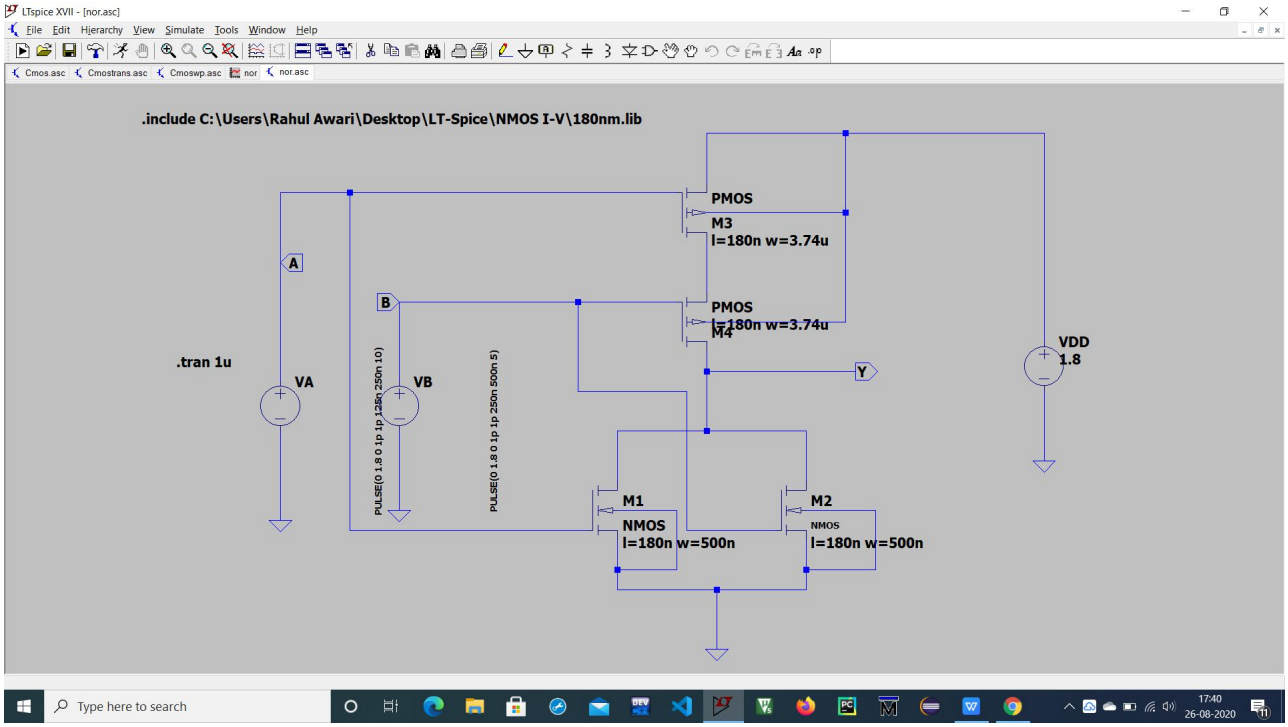
5)Average power for both CMOS and NMOS is calculated along with graph.

NOR Implementation

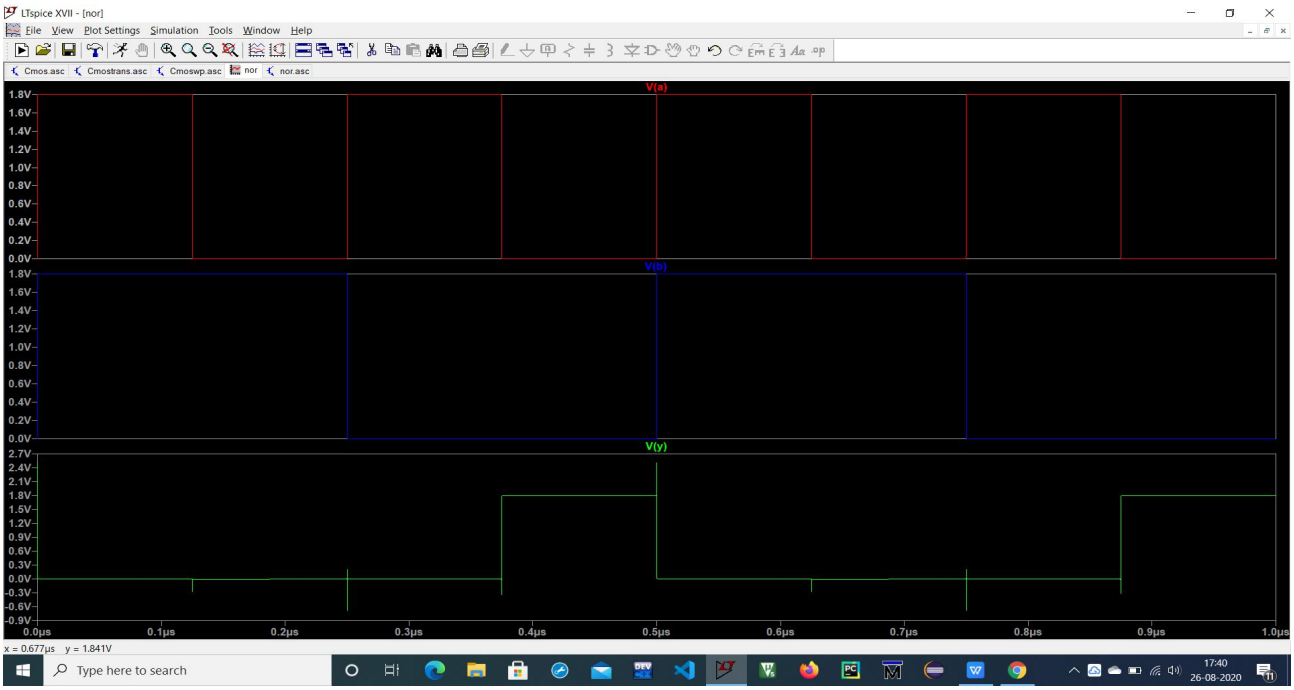
Aim:

1) To plot DC analysis of NOR logic implementation.
2) To observe output when propagated over both power source A,B.
3) Calculate Average Power.

SCHEMATIC:-



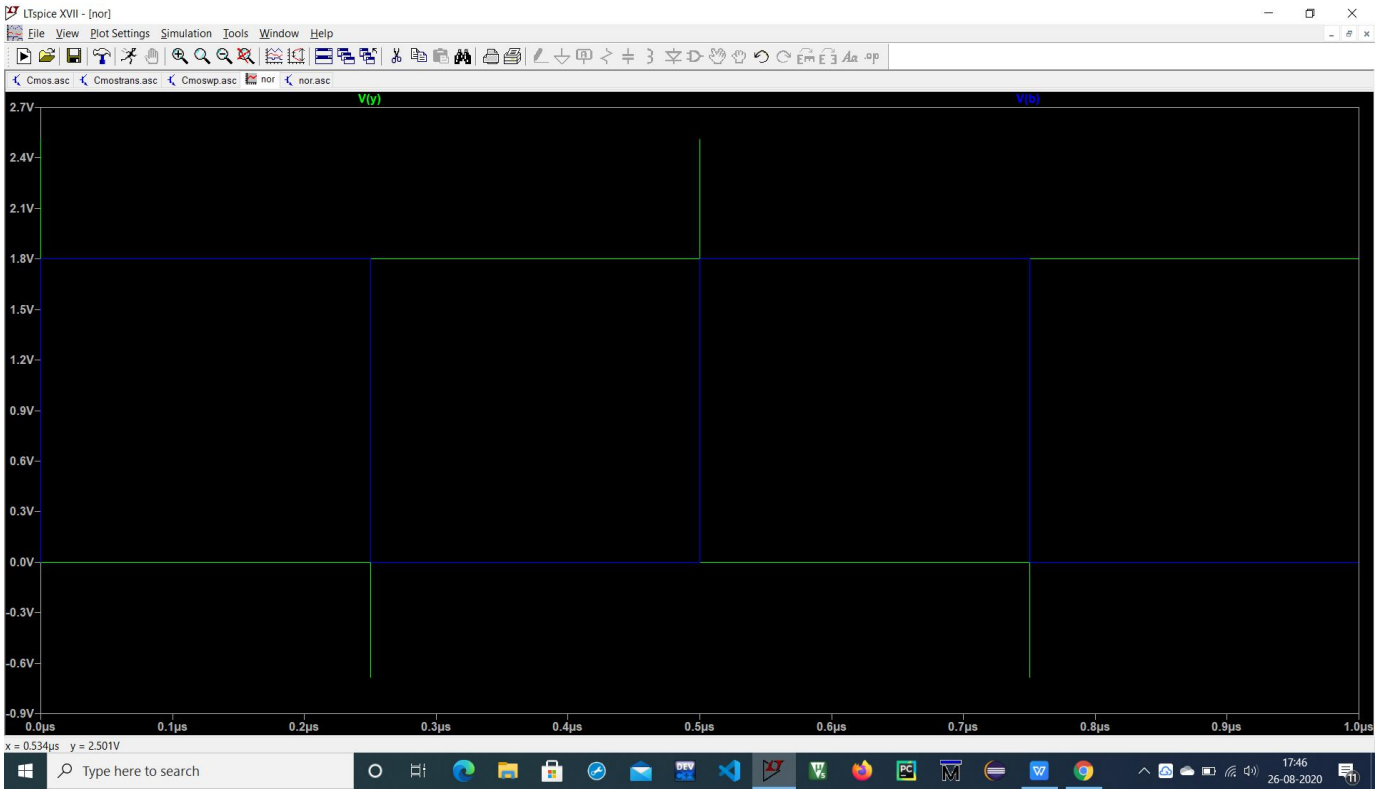
GRAPHS:-

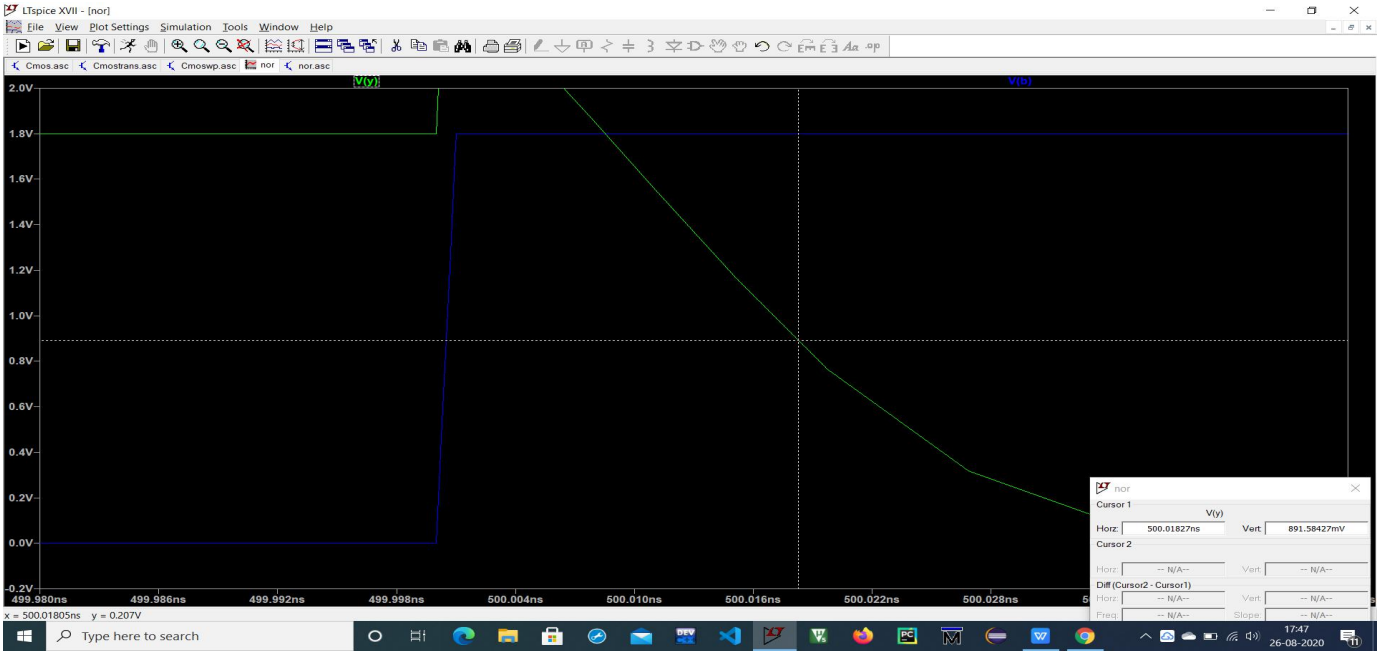


A) PMOS:-length=180n,width-3.74u
B) NMOS:-length=180n,width-500n
C) Va,Vb-pulse
D) Vdd-1.8v
E) .tran 1u

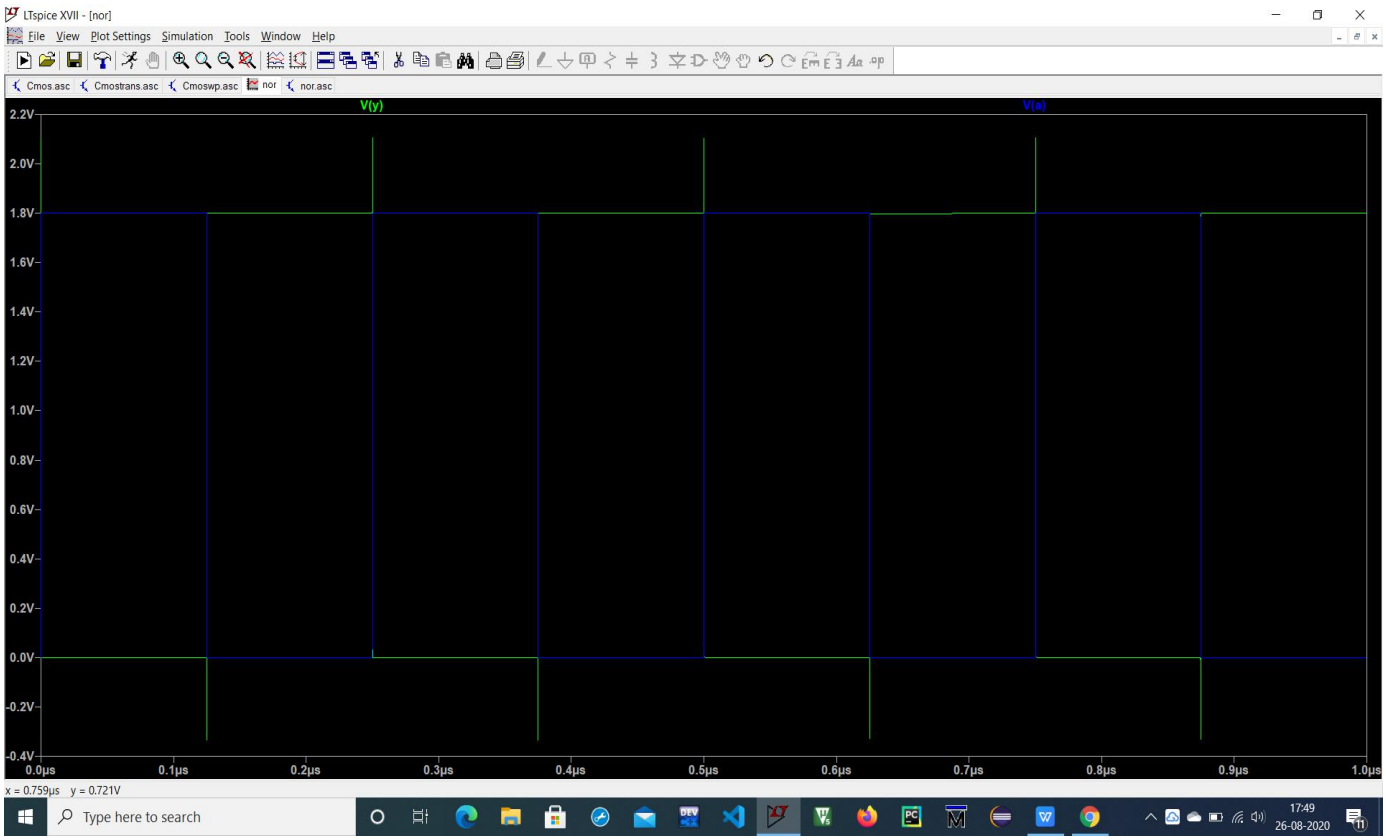
2)To observe output when propagated over both power source A,B.
When Propagated B 0 to 1.8 and A is kept off.

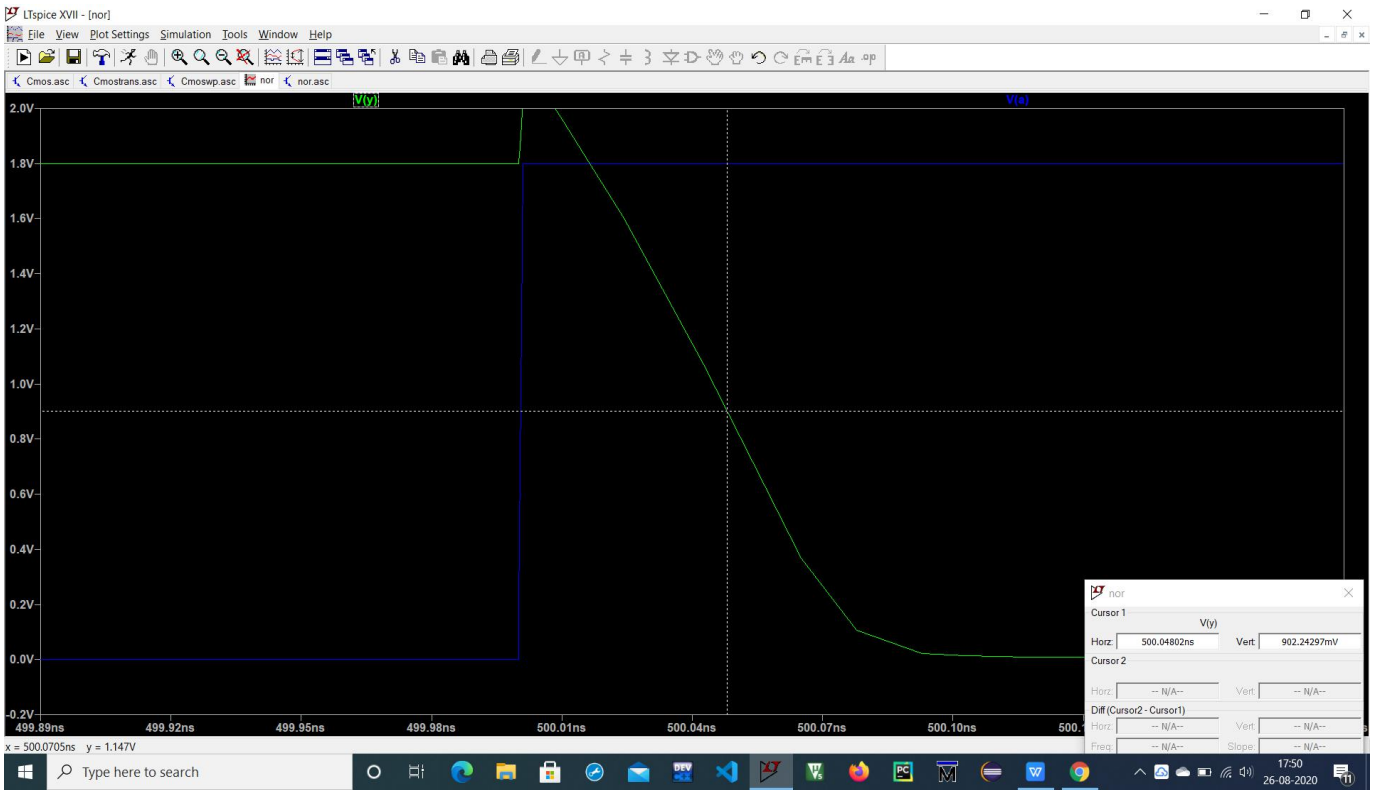
Screen Shot:-





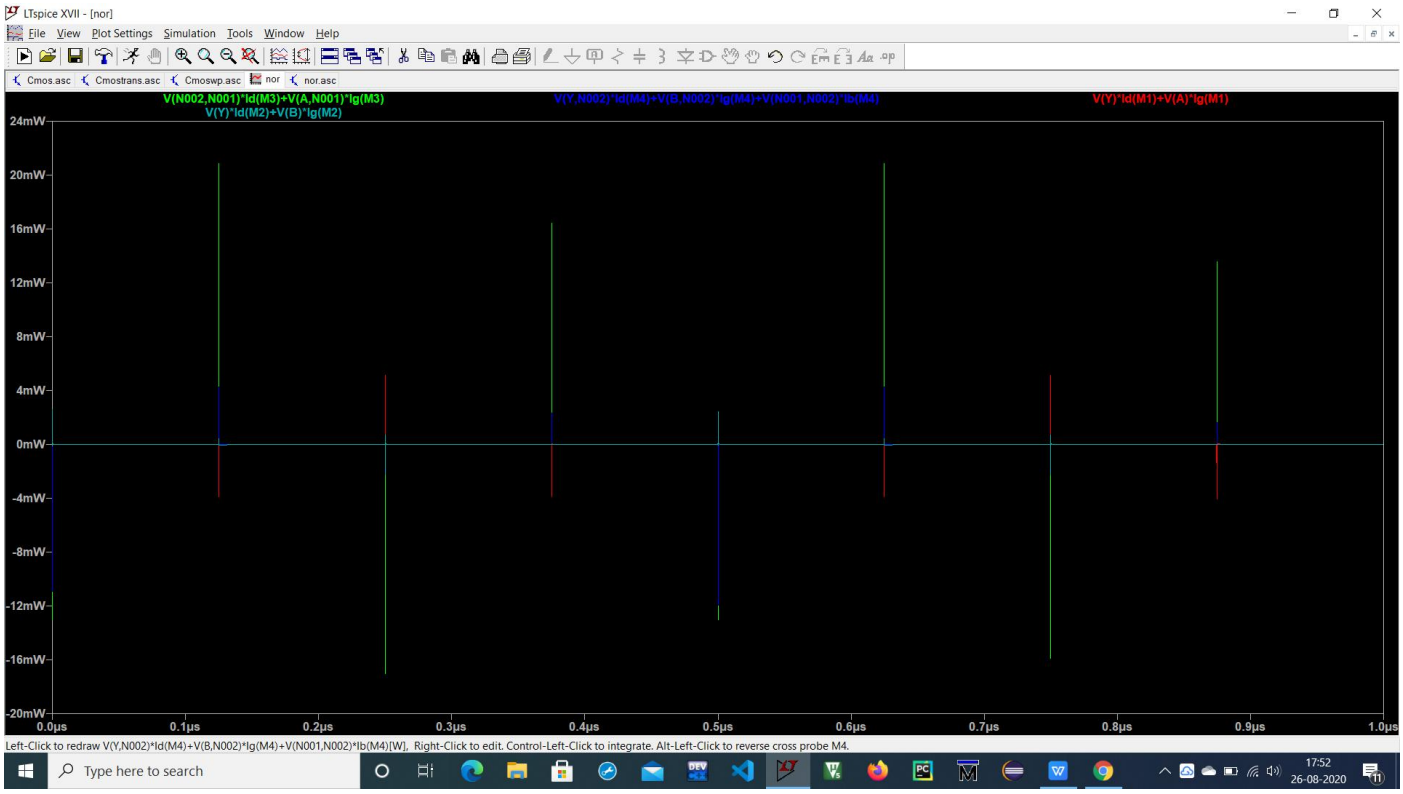
When propagated A 0 to 1.8, and B is kept off.

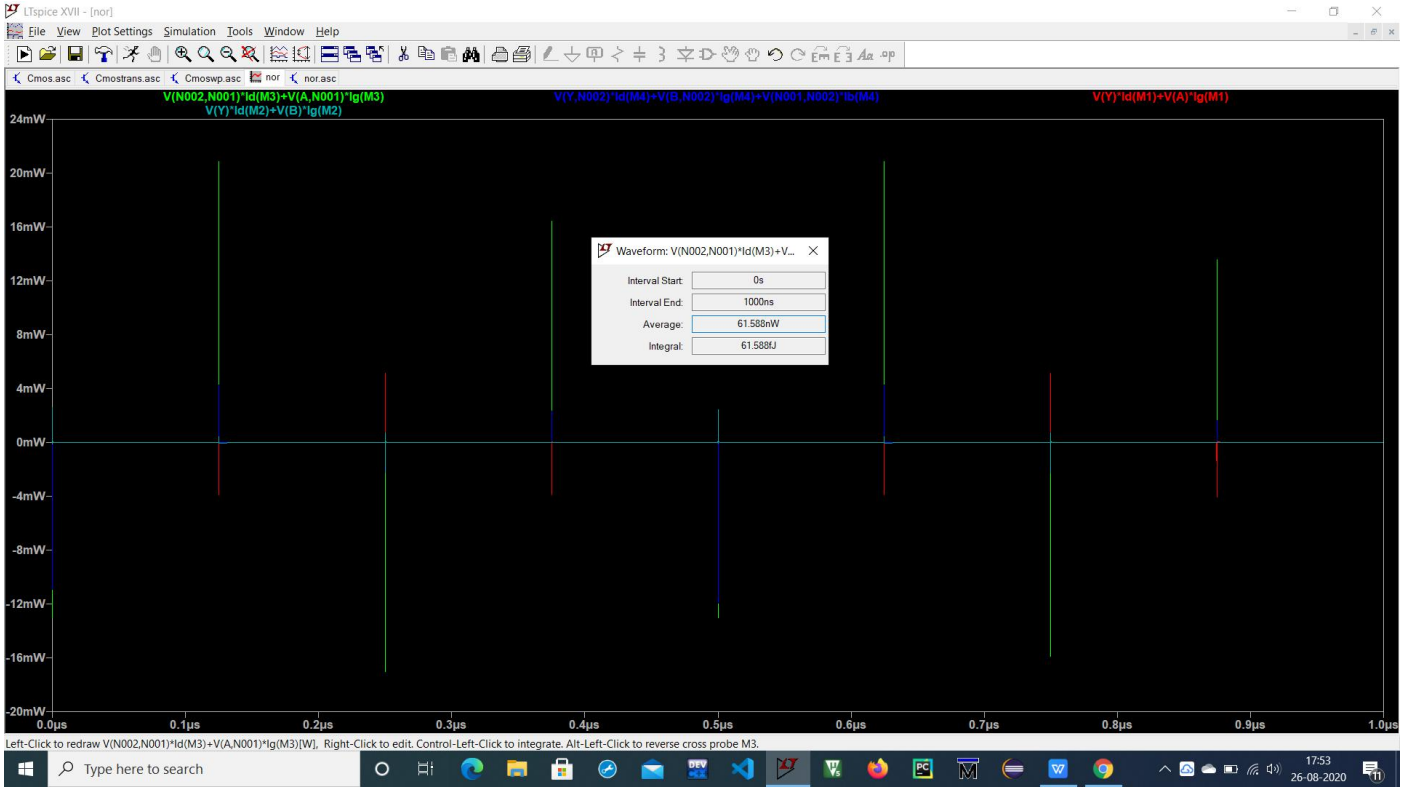




4) Avg Power

Screen Shot:-





CALCULATIONS:-

1)For B(0→1.8V)
A)Rise delay - 17.6ps
B)Fall delay - 16.5ps
C)Avg delay- 17.05ps

2)For A(0→1.8V)
A)Rise delay - 46.3ps
B)Fall delay - 26.41ps
C)Avg delay - 36.35ps.

3)Total Average Power:-

1)	M1(NMOS)	15.62nW
2)	M2(NMOS)	13.78nW
3)	M4(PMOS)	43.099nW
4)	M3(PMOS)	61.539nW

Total Power:- 139.107nW

Inference:-

1)

Inputs		Outputs
X	Y	Z
0	0	1
0	1	0
1	0	0
1	1	0

2) Output Voltage plot is observed for both input voltage A and B.

3)When B is propagated from 0 to 1.8v ,time is noted at which vertical is Vdd/2 For both cases,firstly for falling output and rising input and vice versa. Same Is observed for A as well.The difference of time calculated for both input and Output curve is time delay and average is calculated.

4)The average power calculated is the cummulative power of all the four transistor.

5)When the input is steady at either a high or a low voltage (static condition) then one transistor is always off. Hence the current flowing is extremely small - equal to the leakage current of the off transistor. As a result of this the static power dissipation is extremely low.