LAB ASSESSMENT -3

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SUBJECT : VLSI SYSTEM DESIGN (ECE3002-ELA)
SLOT : L43 + L44
FACULTY : PROF. JAGANNADHA NAIDU K

AIM:-Functions Implementation using PTL logic using NMOS only.

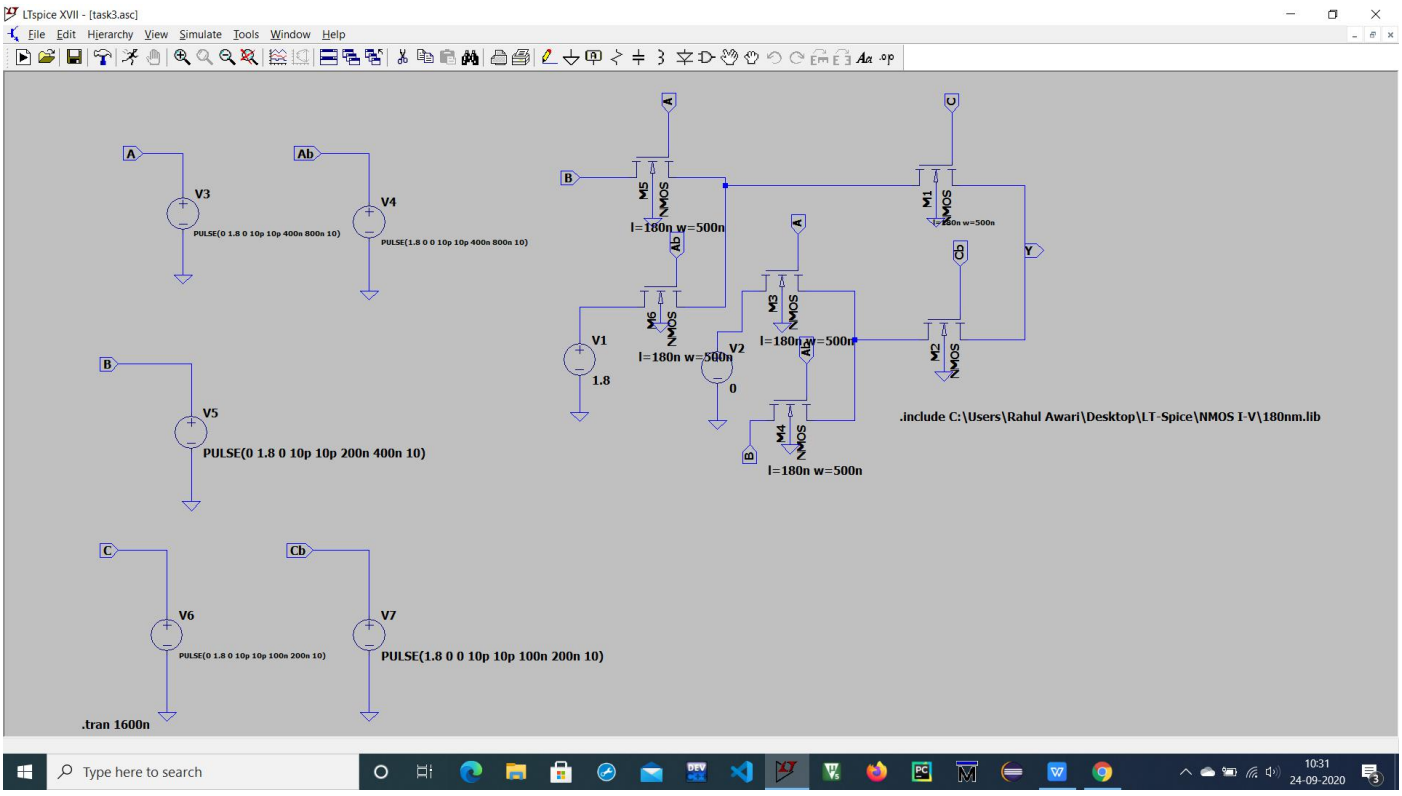
Given Boolean Expression:-

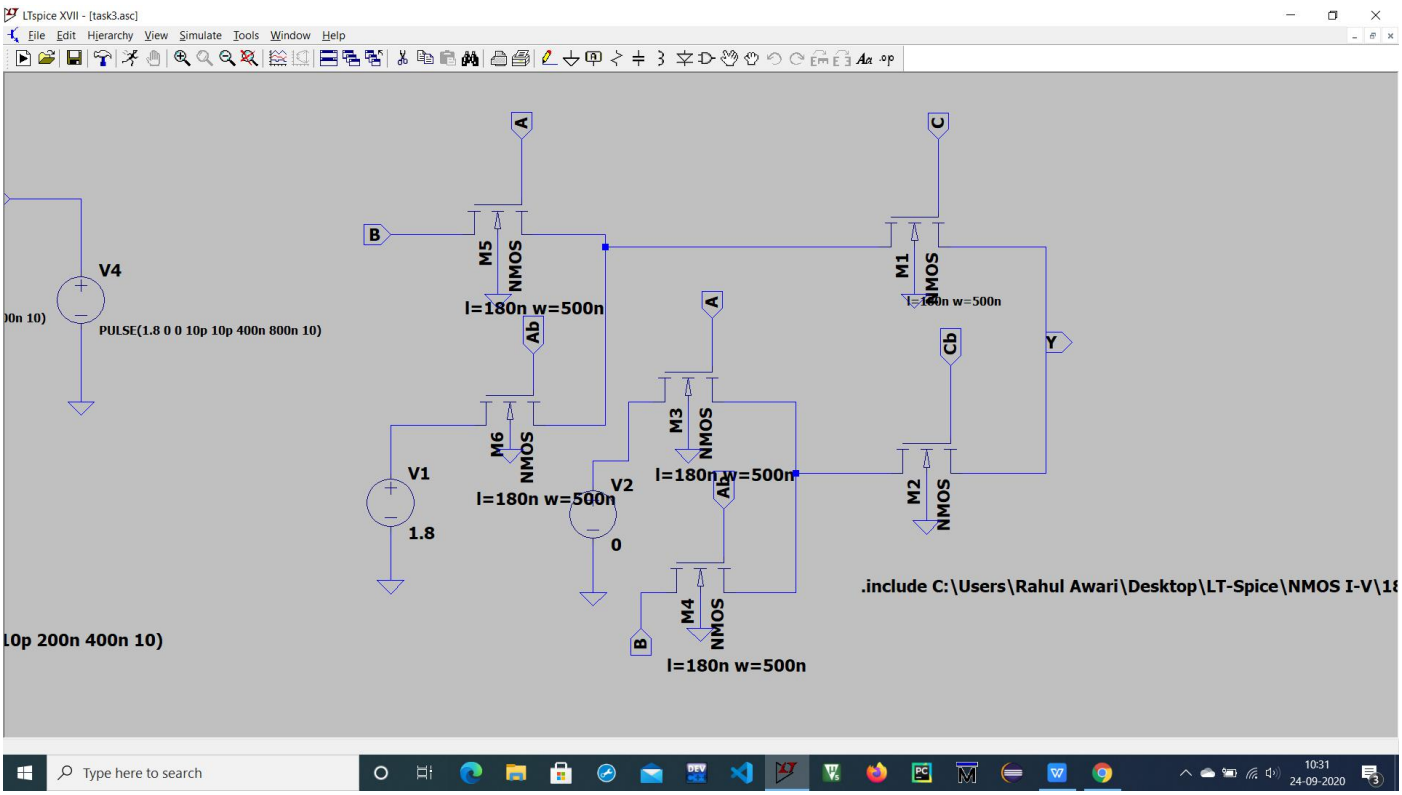
$Y=BC+A'(B \oplus C)$

TO FIND:-

1) Functionality
2) Delay Estimation
3) Average Power dissipation**.**

Circuit Schematic:-





TRUTH TABLE:-

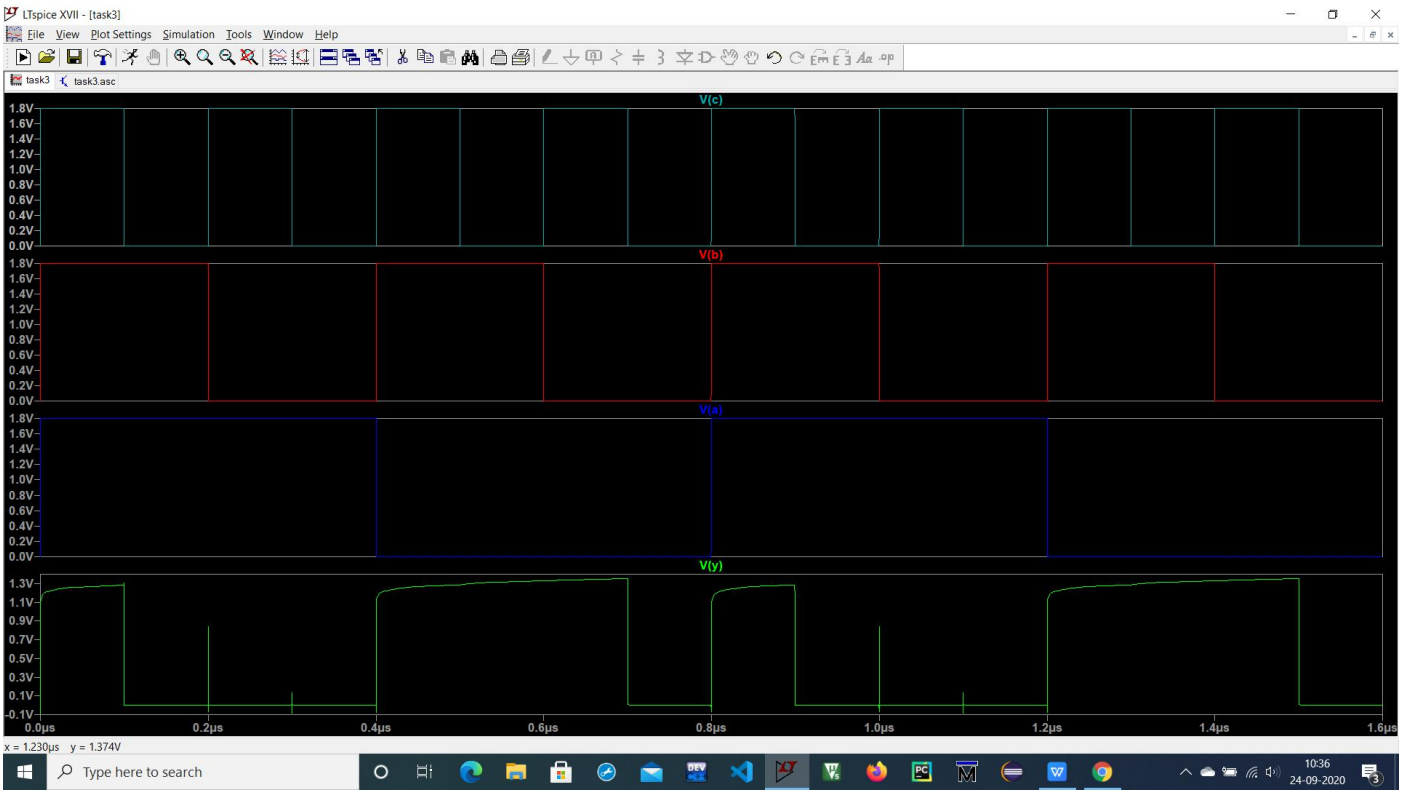
A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

OBSERVATION:-

It is observed that when A and C is low or high ,the input at B is propagrated and reflected at Y(output).

GRAPHS:-

I) Functionality



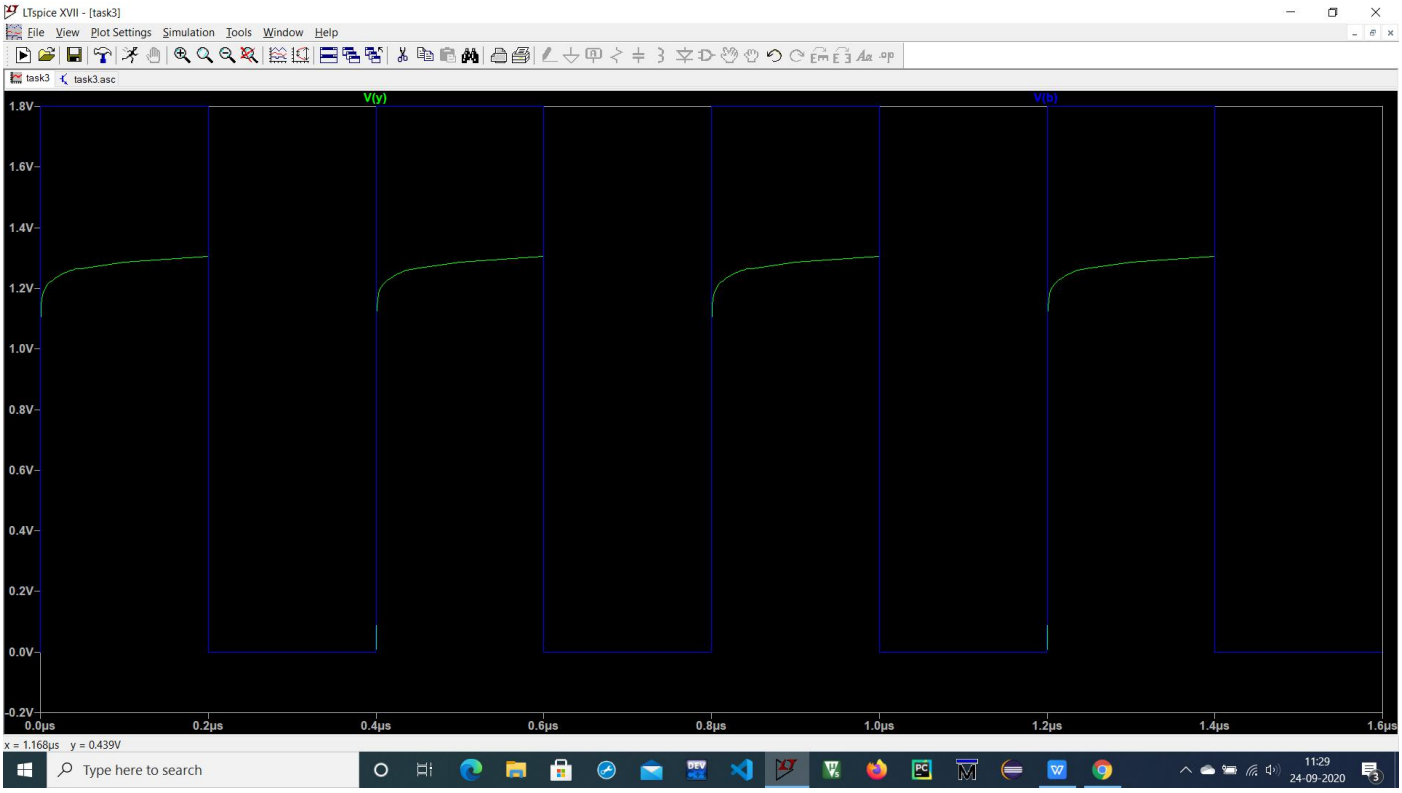
A) Length of NMOS-180nm
B) Width of NMOS-500nm

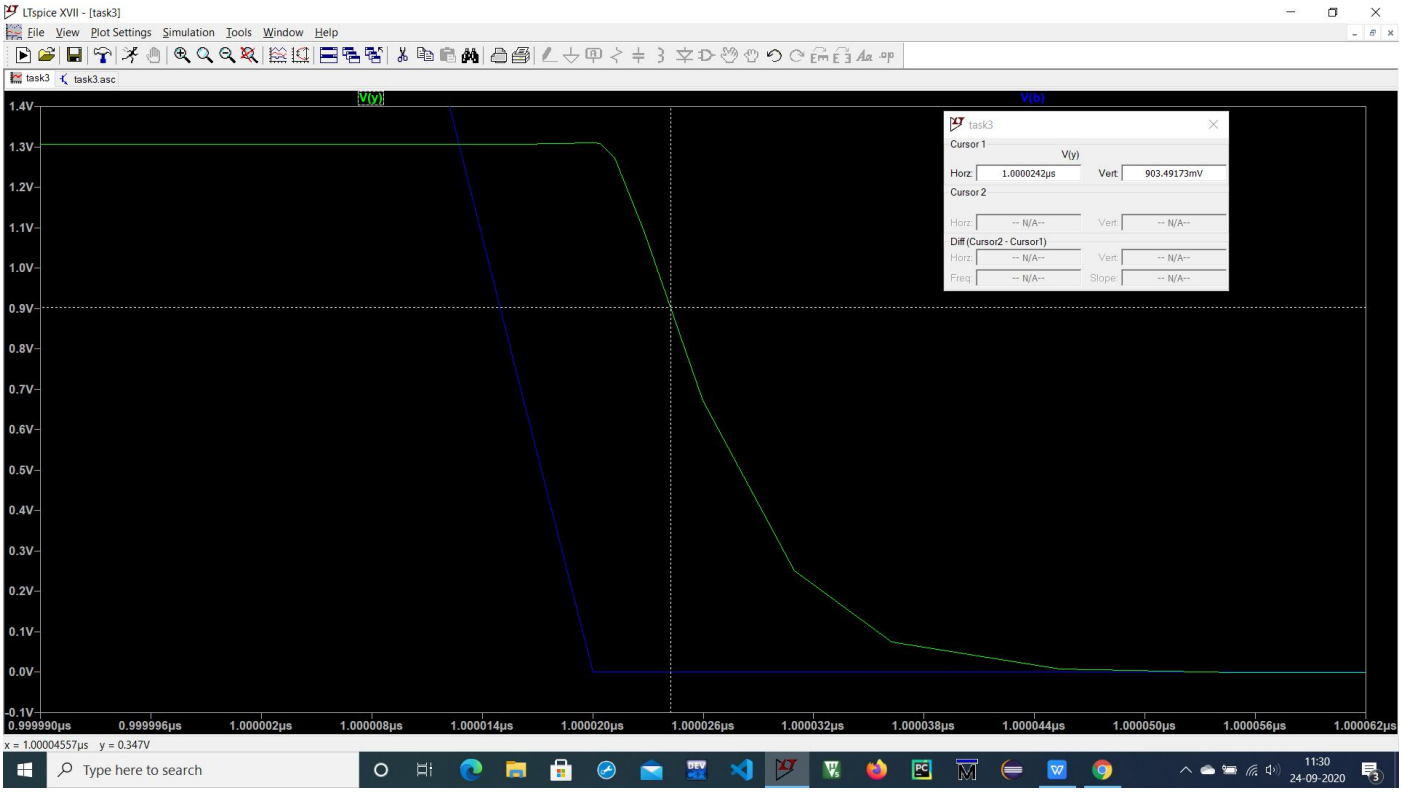
2) Pulse Voltage is used with following input :-
V1=0
V2=1.8
Tdelay=0
Trise=10p
Tfall=10p
Ton=400n
Tperiod=800n
Ncycles=10.

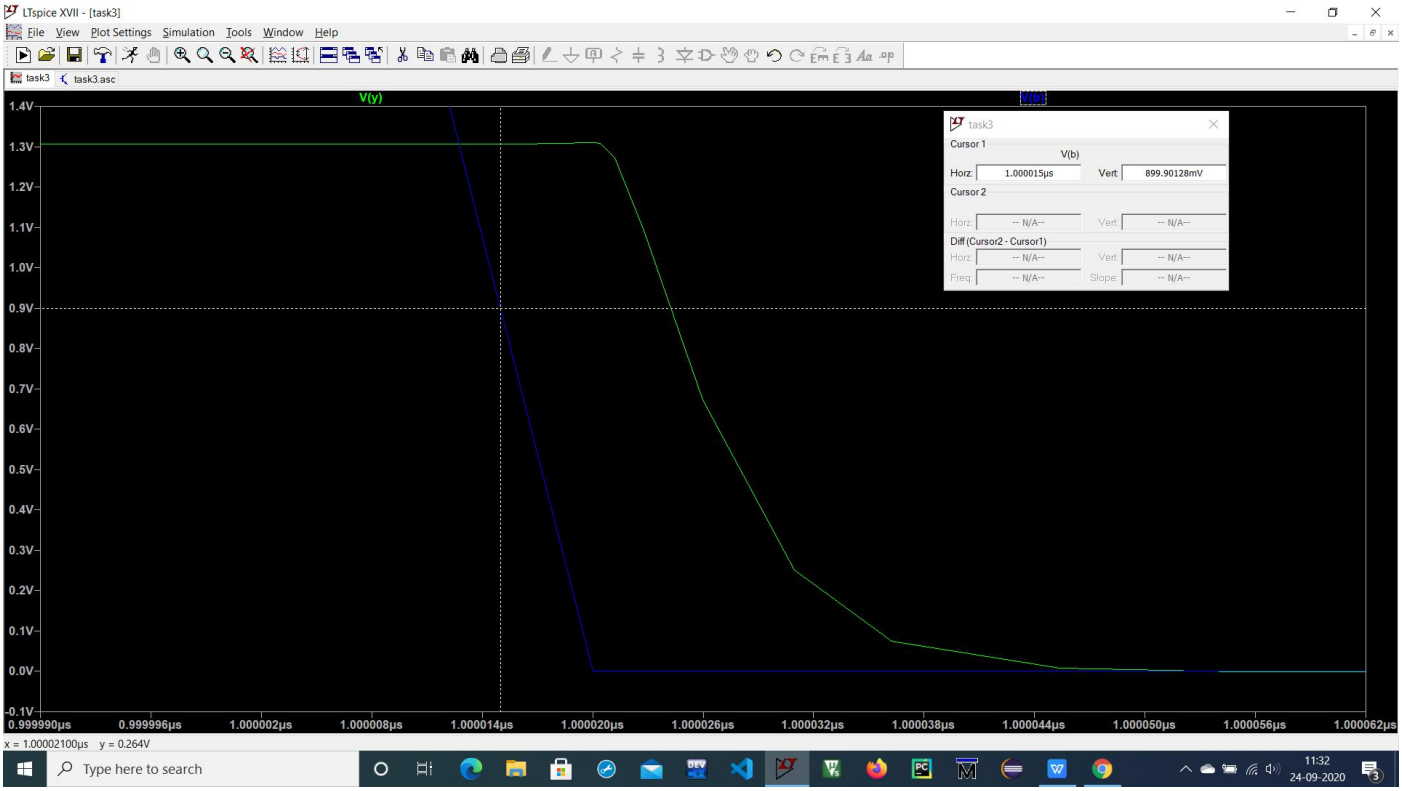
II) <u>DELAY ESTIMATION</u>

It is observed from truth table that when Input A and C is low or high the output observed At Y is same as input B.Hence This condition is used for delay estimation.
A=0,C=0, B(0→1.8)

GRAPHS:-


LTspice XVII - [task3]
File View Plot Settings Simulation Tools Window Help
task3 task3.asc
V(y)
V(b)
1.8V
1.6V
1.4V
1.2V
1.0V
0.8V
0.6V
0.4V
0.2V
0.0V
-0.2V
0.0µs 0.2µs 0.4µs 0.6µs 0.8µs 1.0µs 1.2µs 1.4µs 1.6µs
x = 1.168µs y = 0.439V
Type here to search
11:29
24-09-2020

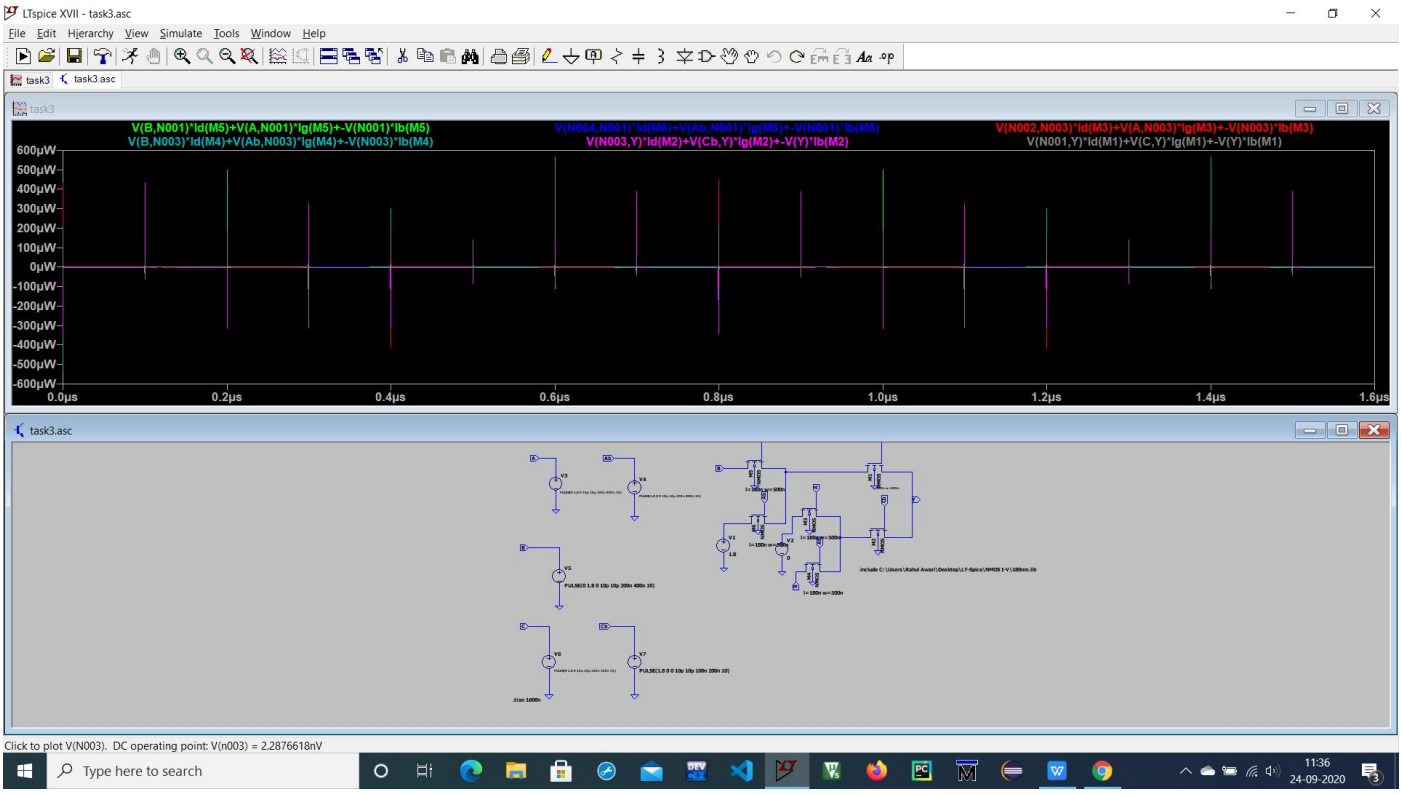

LTspice XVII - [task3]
File View Plot Settings Simulation Tools Window Help
task3 task3.asc
V(y)
V(b)
task3
Cursor 1
V(y)
Horz: 1.0000242µs
Vert: 903.49173mV
Cursor 2
Horz: -- N/A--
Vert: -- N/A--
Diff (Cursor2 - Cursor1)
Horz: -- N/A--
Vert: -- N/A--
Freq: -- N/A--
Slope: -- N/A--
1.4V
1.3V
1.2V
1.1V
1.0V
0.9V
0.8V
0.7V
0.6V
0.5V
0.4V
0.3V
0.2V
0.1V
0.0V
-0.1V
0.999990µs 0.999996µs 1.000002µs 1.000008µs 1.000014µs 1.000020µs 1.000026µs 1.000032µs 1.000038µs 1.000044µs 1.000050µs 1.000056µs 1.000062µs
x = 1.00004557µs y = 0.347V
Type here to search
11:30
24-09-2020

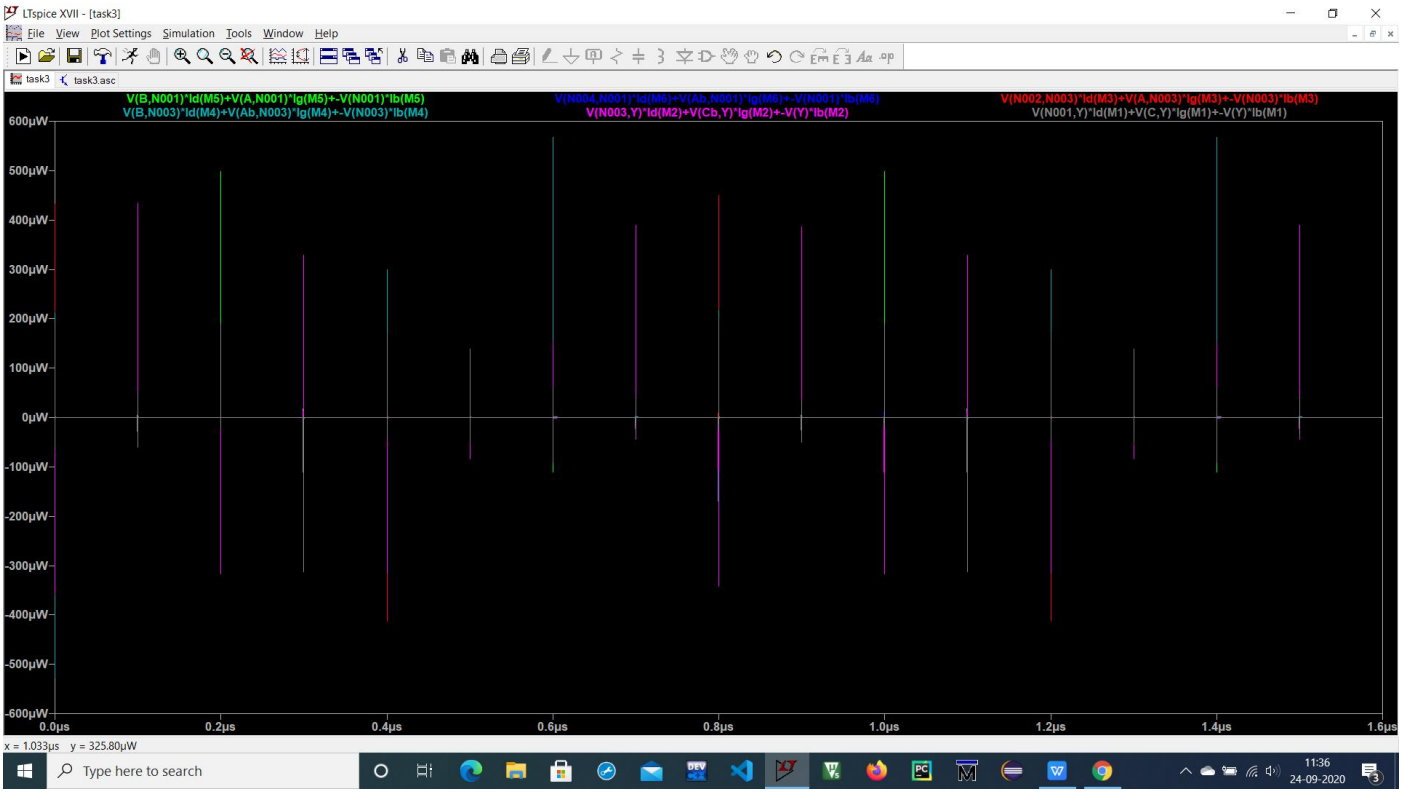


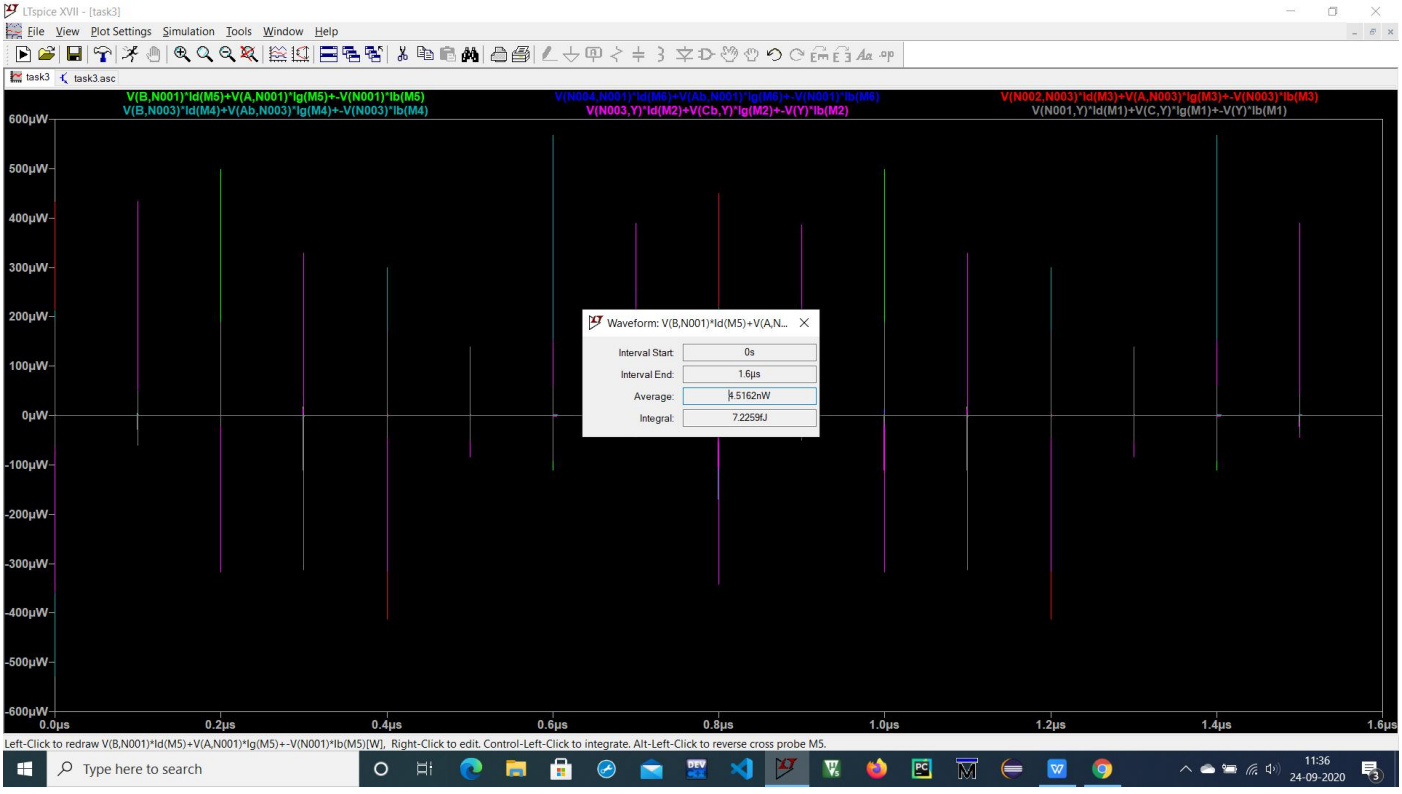
Iii)POWER ESTIMATION:-

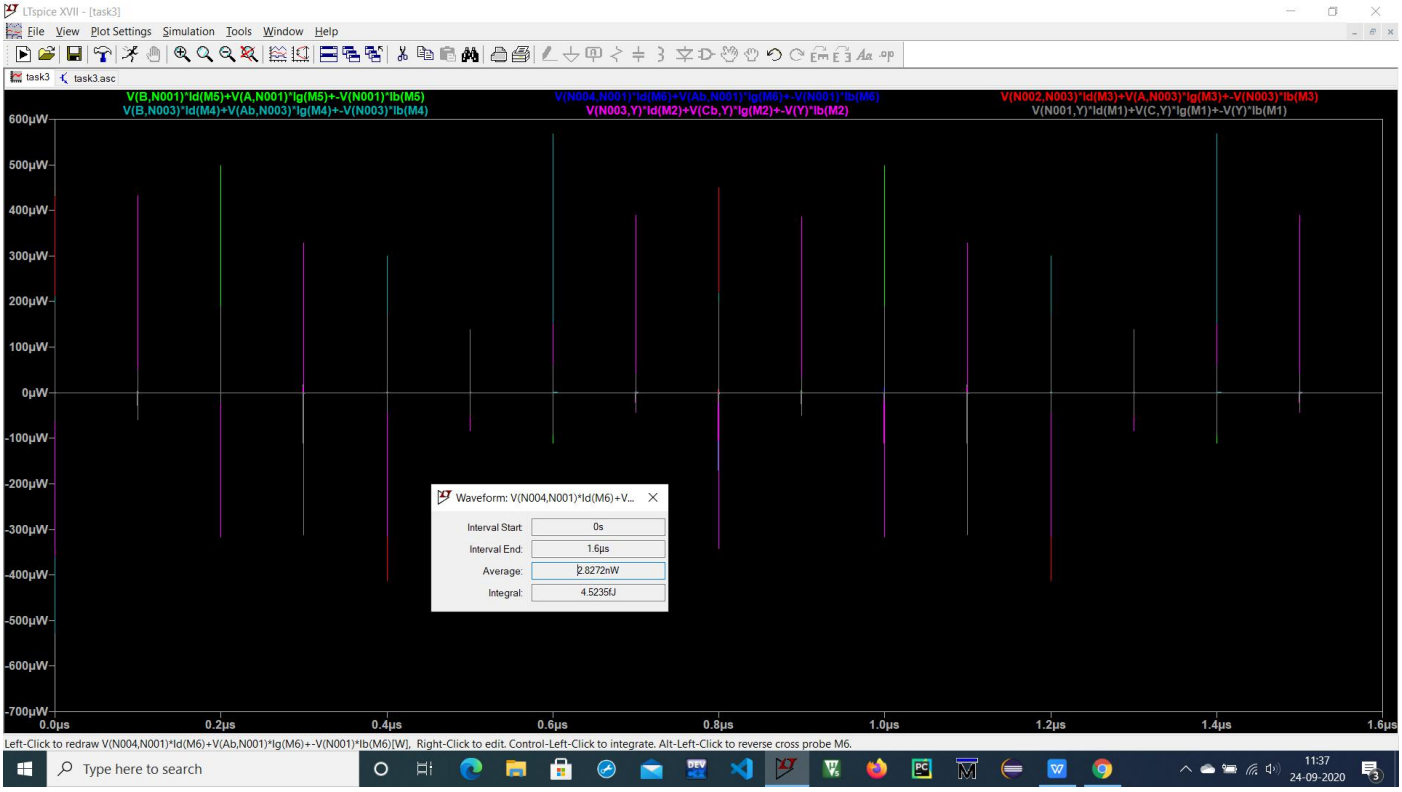
To Calculate Avg power emitted by each transistor.

GRAPHS:-




LTspice XVII - [task3]
File View Plot Settings Simulation Tools Window Help
task3 task3.asc
V(B,N001)*Id(M5)+V(A,N001)*Ig(M5)+-V(N001)*Ib(M5)
V(B,N003)*Id(M4)+V(Ab,N003)*Ig(M4)+-V(N003)*Ib(M4)
V(N004,N001)*Id(M6)+V(Ab,N001)*Ig(M6)+-V(N001)*Ib(M6)
V(N003,Y)*Id(M2)+V(Cb,Y)*Ig(M2)+-V(Y)*Ib(M2)
V(N002,N003)*Id(M3)+V(A,N003)*Ig(M3)+-V(N003)*Ib(M3)
V(N001,Y)*Id(M1)+V(C,Y)*Ig(M1)+-V(Y)*Ib(M1)
600µW
500µW
400µW
300µW
200µW
100µW
0µW
-100µW
-200µW
-300µW
-400µW
-500µW
-600µW
0.0µs
0.2µs
0.4µs
0.6µs
0.8µs
1.0µs
1.2µs
1.4µs
1.6µs
x = 1.033µs y = 325.80µW
Type here to search
11:36
24-09-2020


LTspice XVII - [task3]
File View Plot Settings Simulation Tools Window Help
task3 task3.asc
V(B,N001)*Id(M5)+V(A,N001)*Ig(M5)+-V(N001)*Ib(M5)
V(B,N003)*Id(M4)+V(Ab,N003)*Ig(M4)+-V(N003)*Ib(M4)
V(N004,N001)*Id(M6)+V(Ab,N001)*Ig(M6)+-V(N001)*Ib(M6)
V(N003,Y)*Id(M2)+V(Cb,Y)*Ig(M2)+-V(Y)*Ib(M2)
V(N002,N003)*Id(M3)+V(A,N003)*Ig(M3)+-V(N003)*Ib(M3)
V(N001,Y)*Id(M1)+V(C,Y)*Ig(M1)+-V(Y)*Ib(M1)
Waveform: V(B,N001)*Id(M5)+V(A,N...
Interval Start: 0s
Interval End: 1.6µs
Average: 4.5162nW
Integral: 7.2259fJ
600µW
500µW
400µW
300µW
200µW
100µW
0µW
-100µW
-200µW
-300µW
-400µW
-500µW
-600µW
0.0µs
0.2µs
0.4µs
0.6µs
0.8µs
1.0µs
1.2µs
1.4µs
1.6µs
Left-Click to redraw V(B,N001)*Id(M5)+V(A,N001)*Ig(M5)+-V(N001)*Ib(M5)[W], Right-Click to edit. Control-Left-Click to integrate. Alt-Left-Click to reverse cross probe M5.
Type here to search
11:36
24-09-2020



CALCULATIONS:-

I)DELAY ESTIMATIONS:-

Case1)

A=0

C=0

B(0→1.8)

T1=1.200005us
T2=1.2000359us
T3=1.0000243us
T4=1.000016us

Tpdr=30.9ps
Tpdf=9.3ps

Case2)

A=1

C=1

B(1.8→0)

T1=1.0000465us
T2=1.000015us
T3=1.2000143us
T4=1.2000050us

Tpdr=31.5ps
Tpdf=9.3ps

POWER ESTIMATION:-

M1	4.5162nW
M2	6.3008nW
M3	2.8272nW
M4	3.9735nW
M5	1.34nW
M6	4.12nW

Avg Power=23.2026nW

INFERENCE:-

1) The given boolean expression is implemented using pass transistor logic using only NMOS.

2) For Delay estimation ,It is observed from truth table that the input B Is reflected at output Y,irrespective of input A and C.

3) So for delay estimation we consider situation of A=0,C=0 and B(0→1.8) And Case 2 A=1.8,C=1.8 and B(1.8→0).

4) Time at which value is Vdd/2 is observed for both input B and output Y and The difference is used for the calculation of time delay.

5) The rise delay is observed to be around 30.9ps and fall delay to be 9.3ps

6) The average power calculated is the cummulative power of all the six transistor.

7) In functionality graph is can be observed that for A is on B is propagated and values similar to truth table.