LAB ASSESSMENT -4

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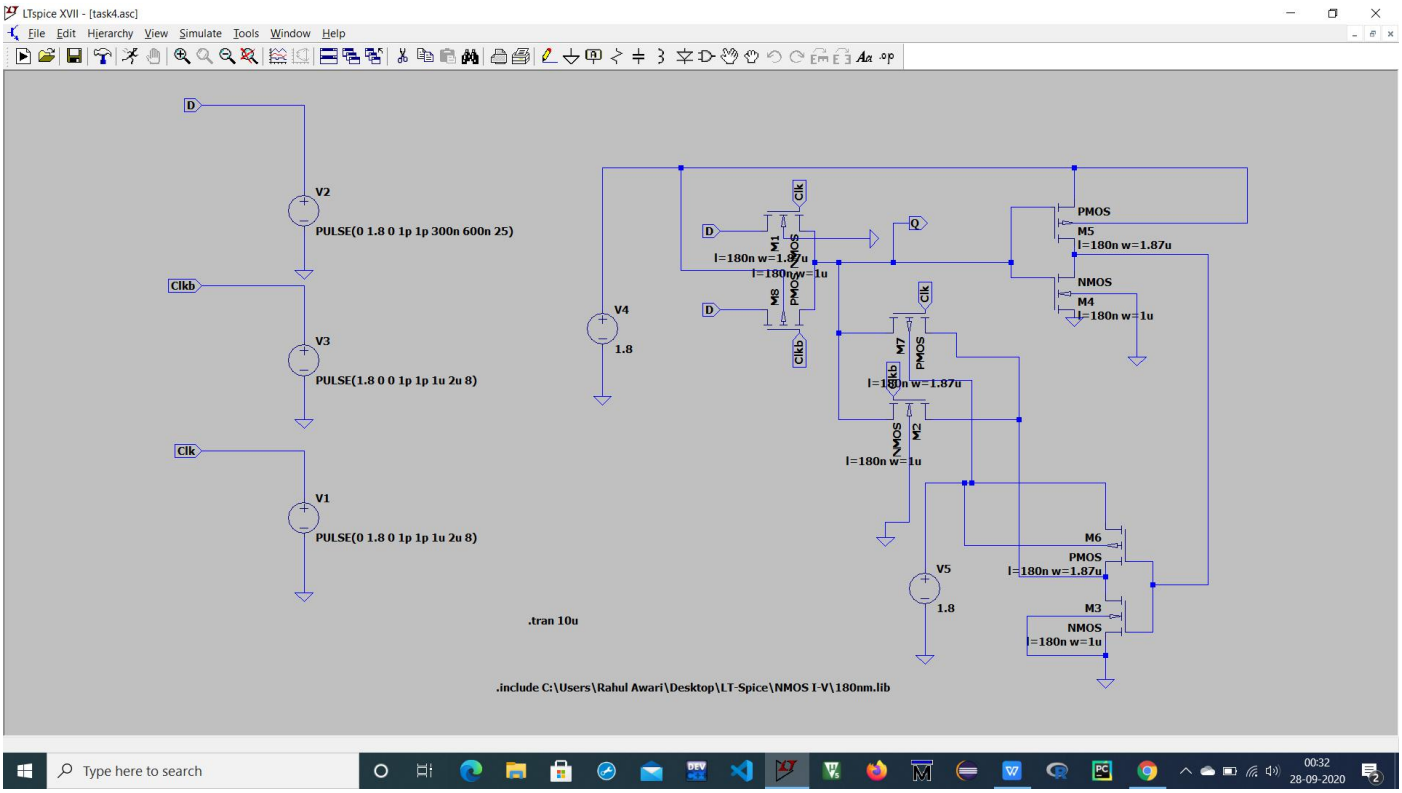
REGISTER NUMBER: 18BEC2014
SUBJECT : VLSI SYSTEM DESIGN (ECE3002-ELA)
SLOT : L43 + L44
FACULTY : PROF. JAGANNADHA NAIDU K

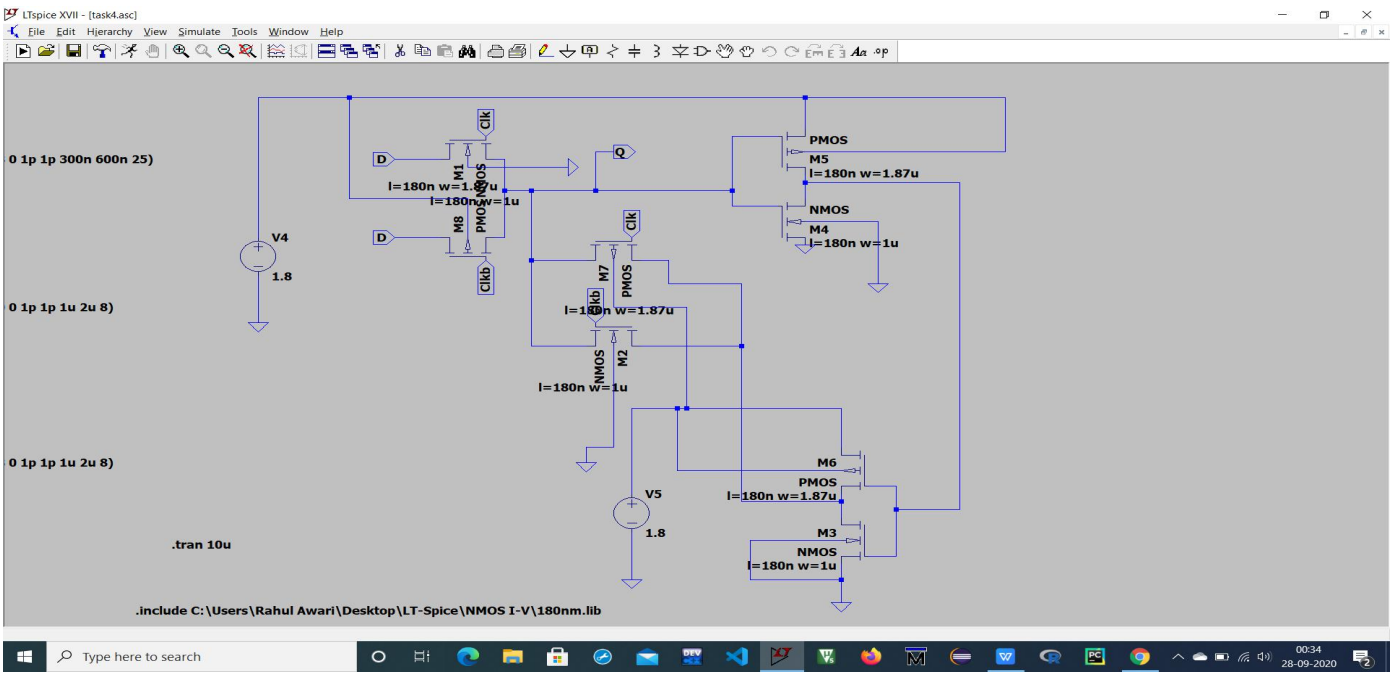
AIM:-Implementing Positive D-Latch using Transmission gate logic.

TO FIND:-

A) Functionality
B) Delay Estimation(D→Q)
C) Power Dissipation.

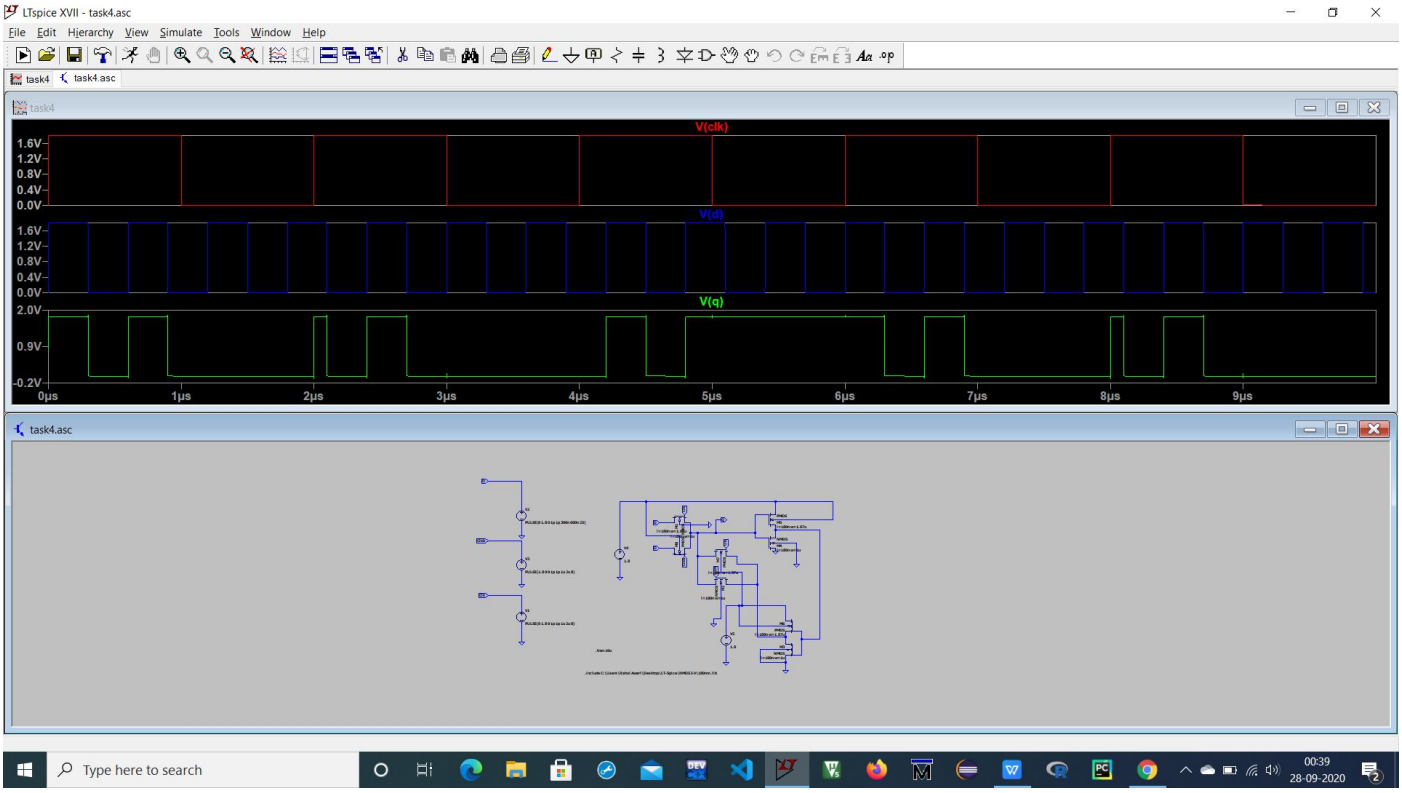
CIRCUIT SCHEMATIC:-

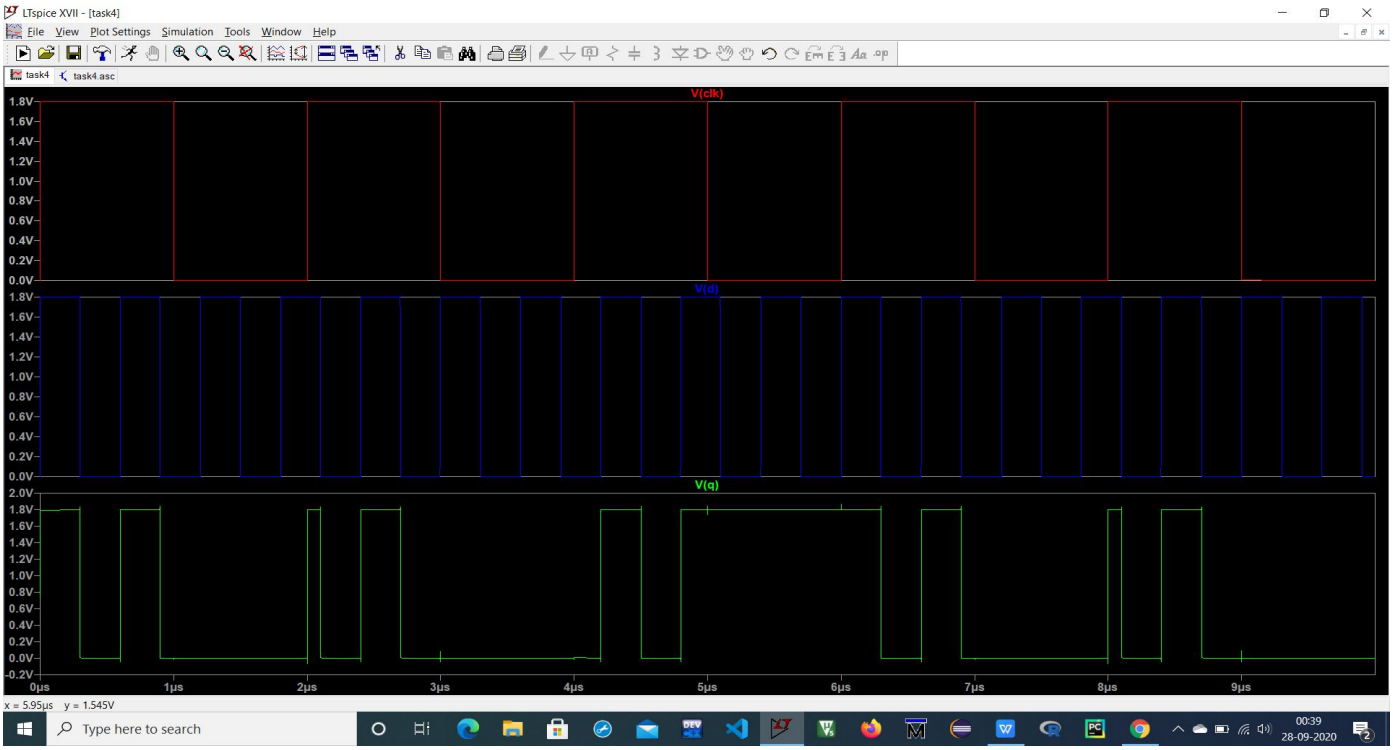




NMOS:-
Width=1um
Length=180nm
PMOS:-
Width=1.87um
Length=180nm

FUNCTIONALITY:-



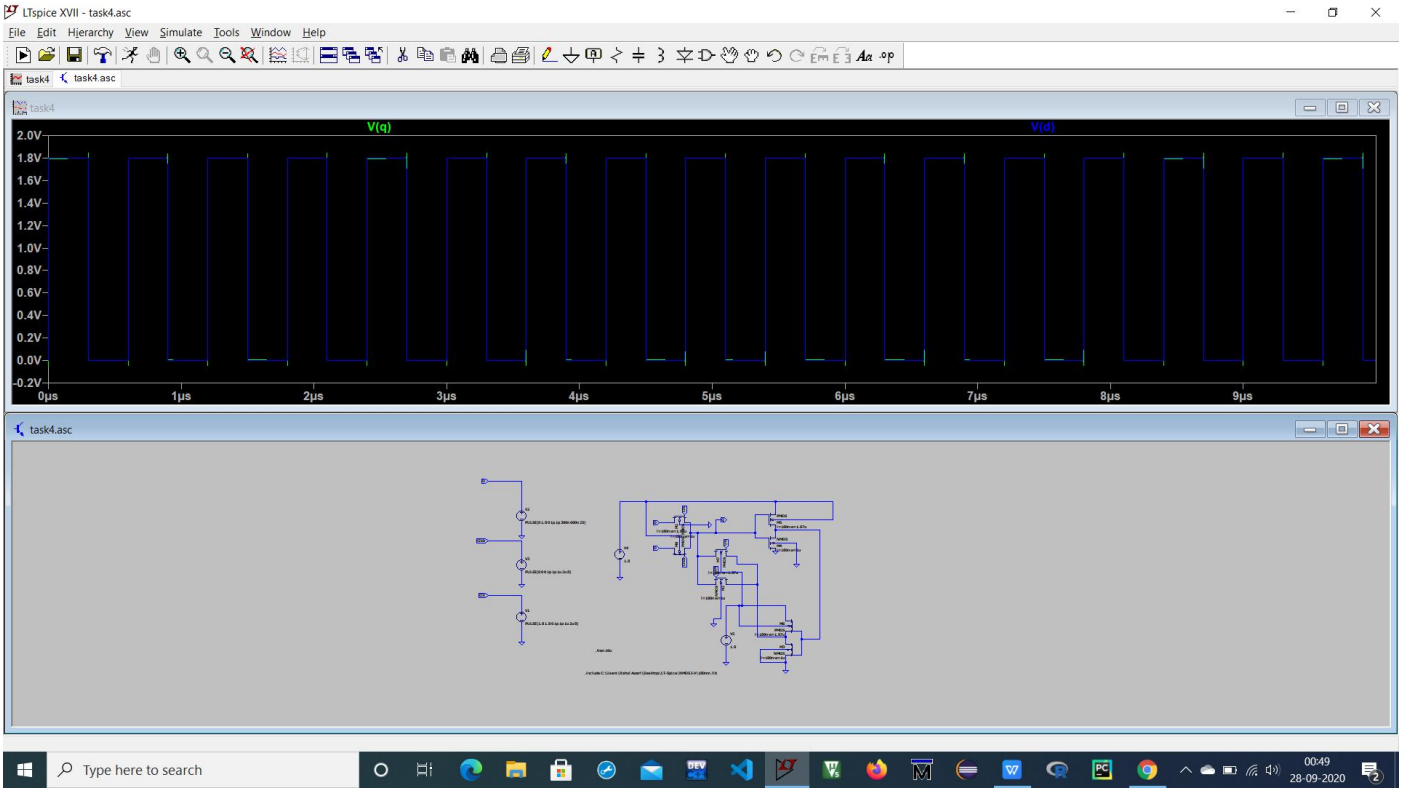


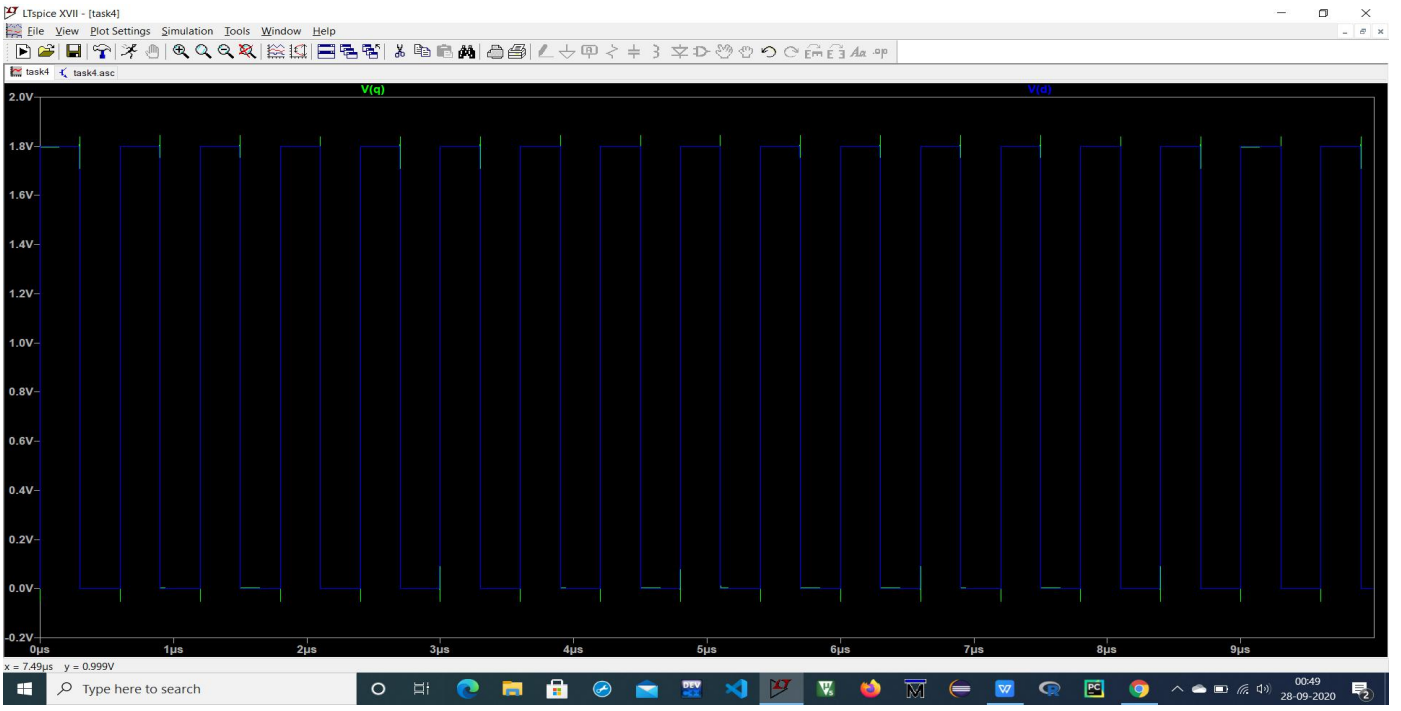
Observation:-
1) When clk=1 Q(Output) is D(Input).
2) When clk=0 Q(Output) is Q(Prev state).

DELAY ESTIMATION(D→q)

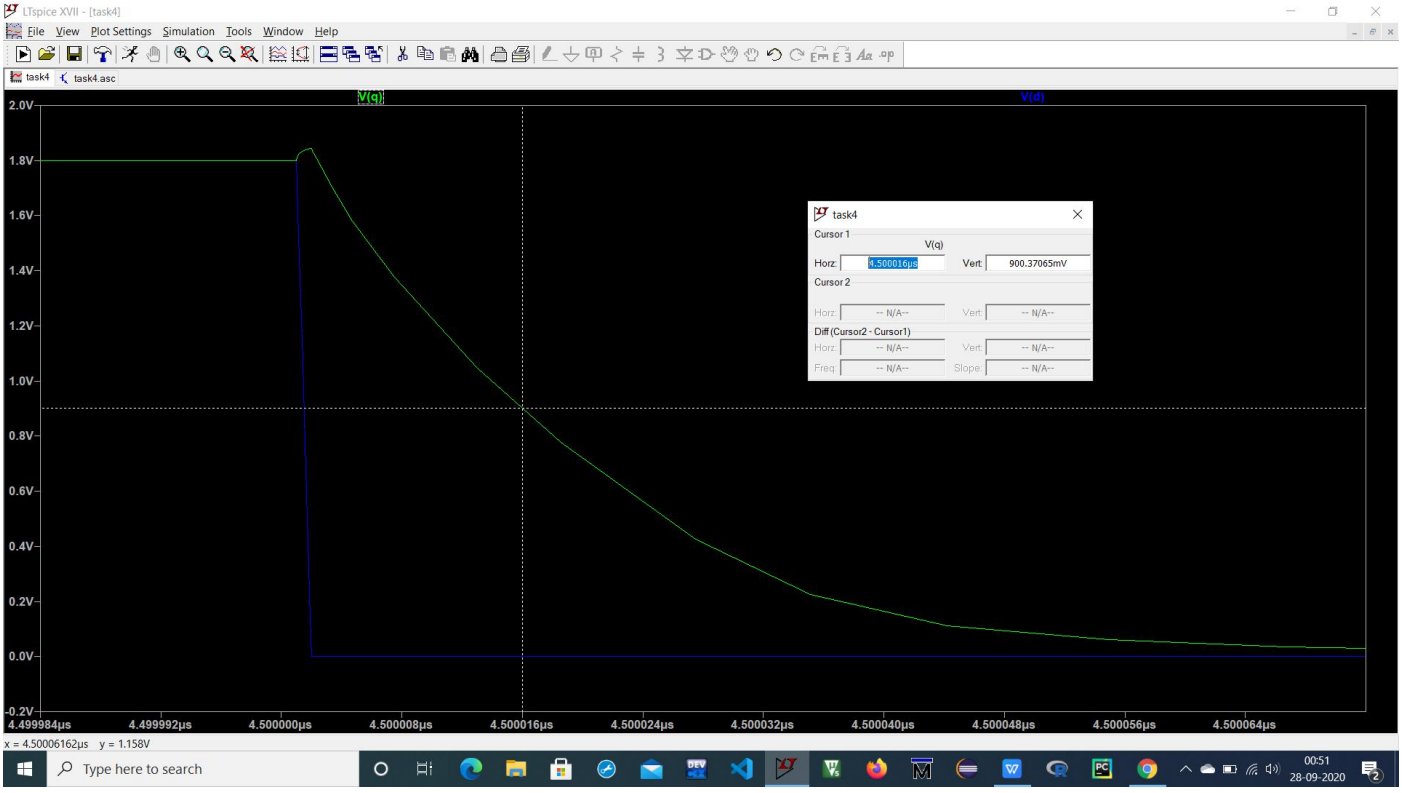
For calculating Delay clk is kept as 1.
Tpdr and Tpdf.

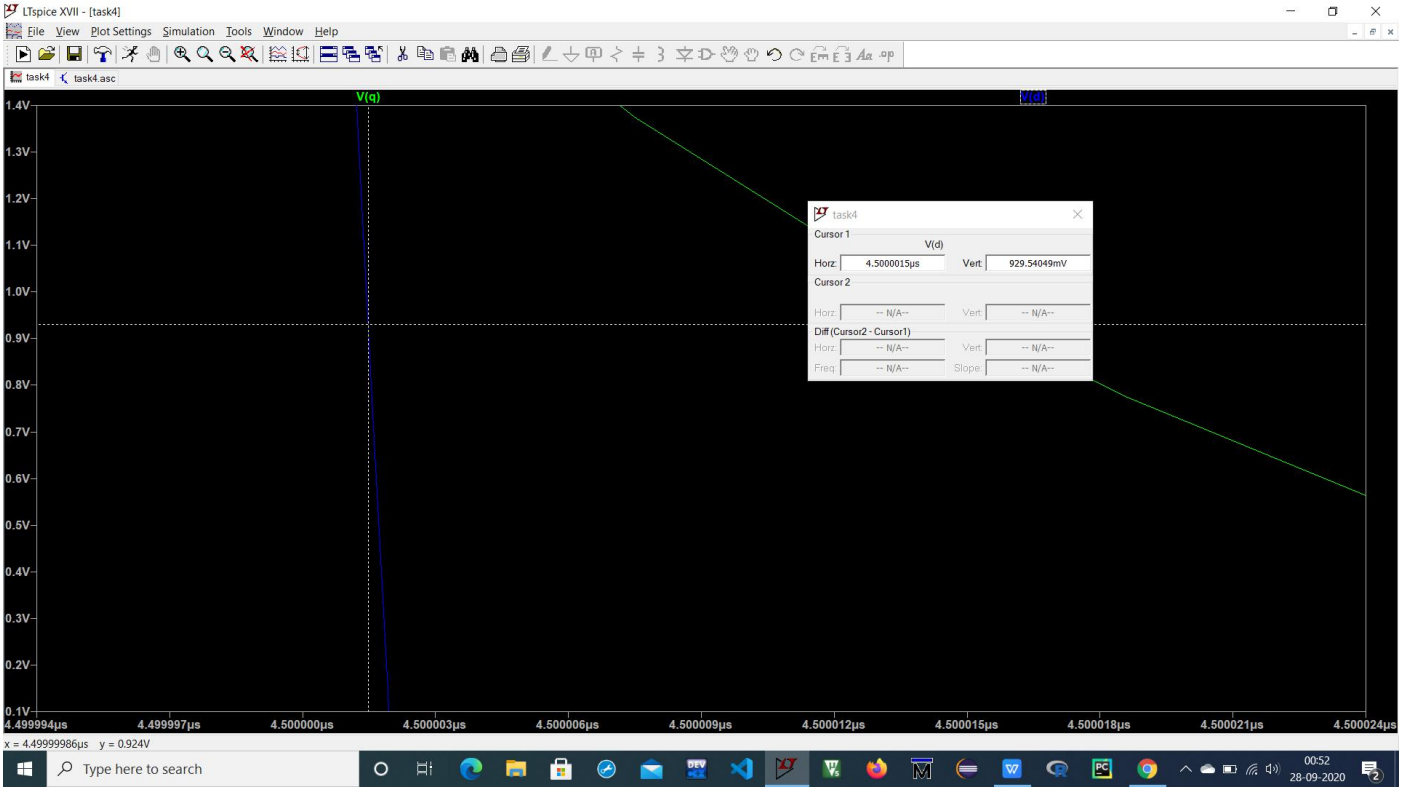
Clkb is kept as 0.



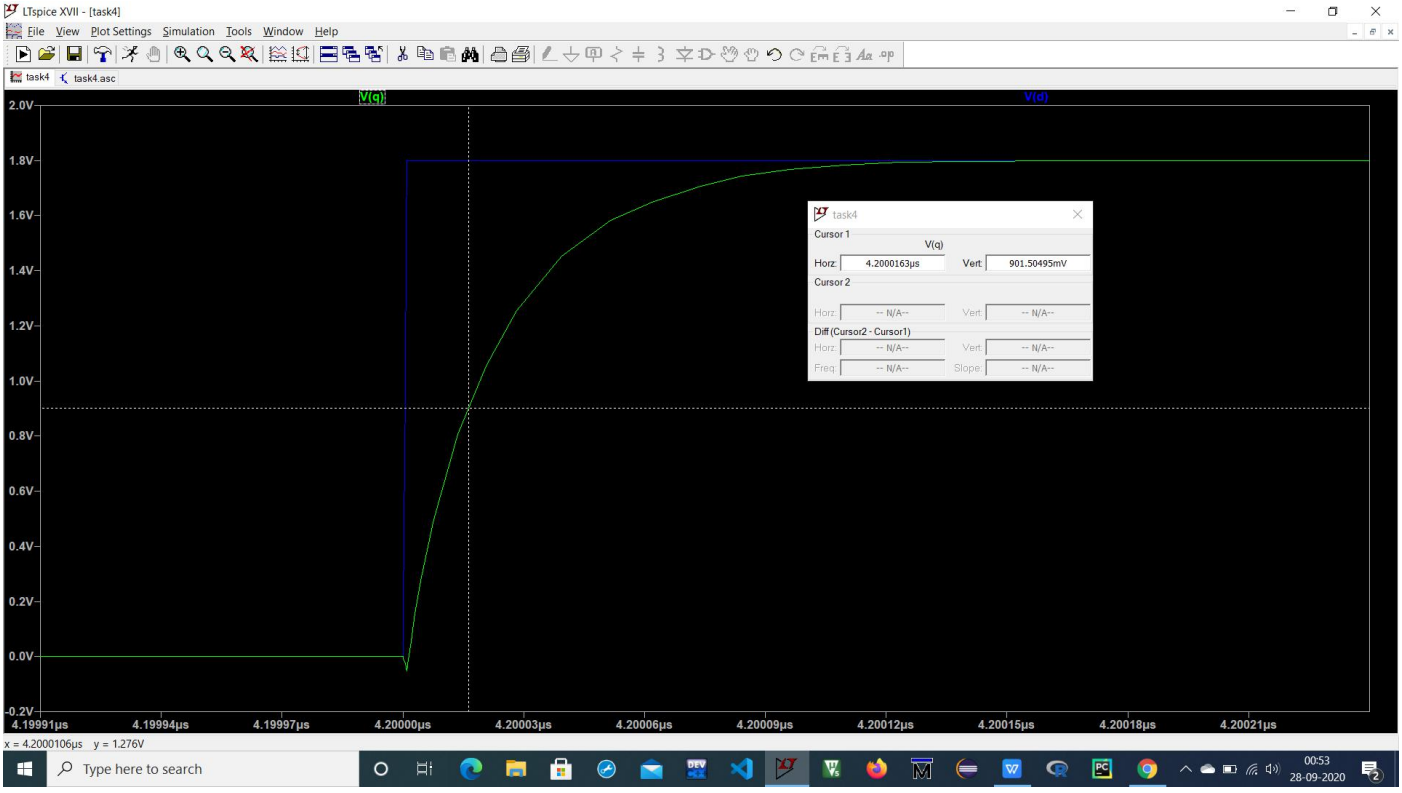


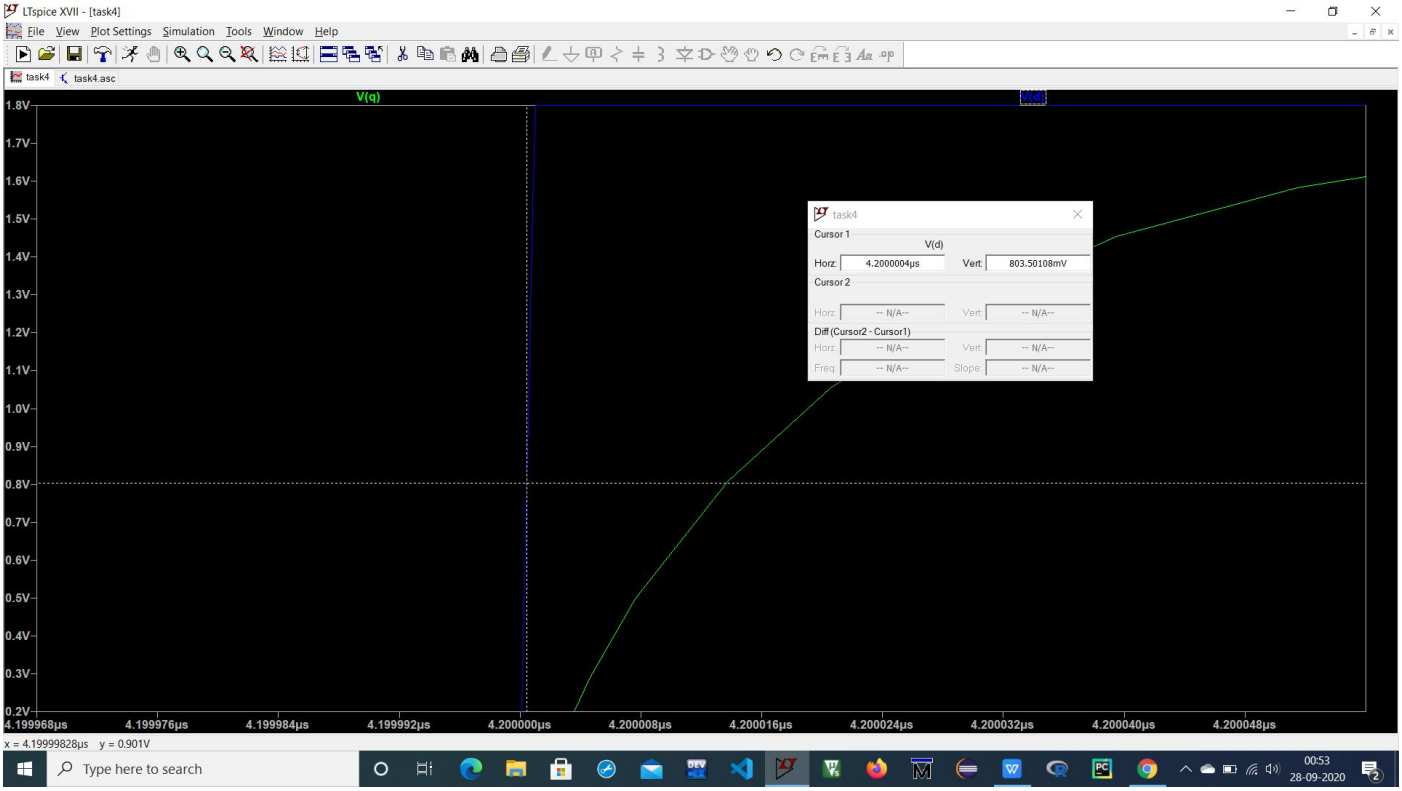
TPDF Observed at Vdd/2:-





TPDR Observation at Vdd/2:-





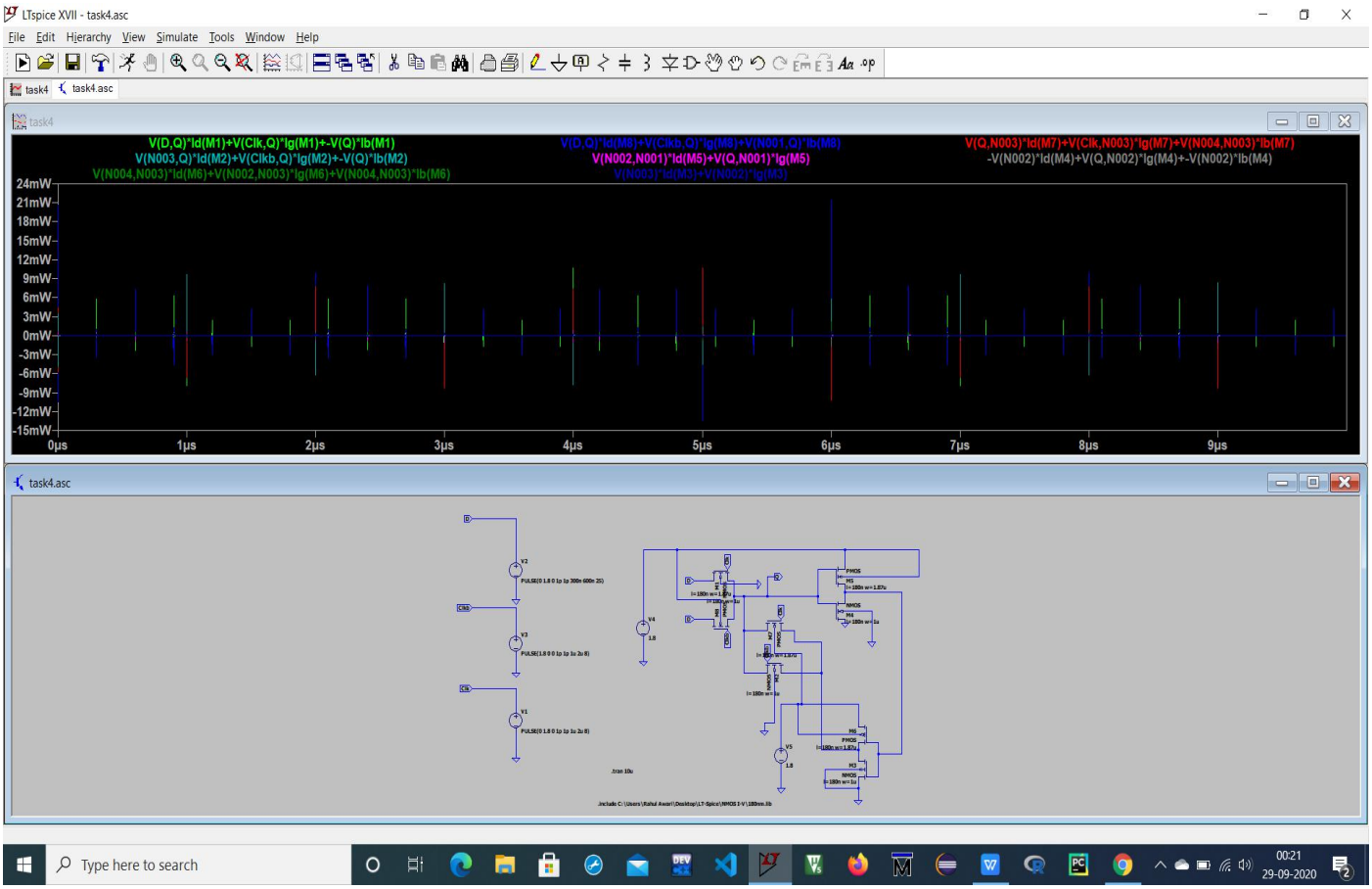
PULSE SPECIFICATION:-

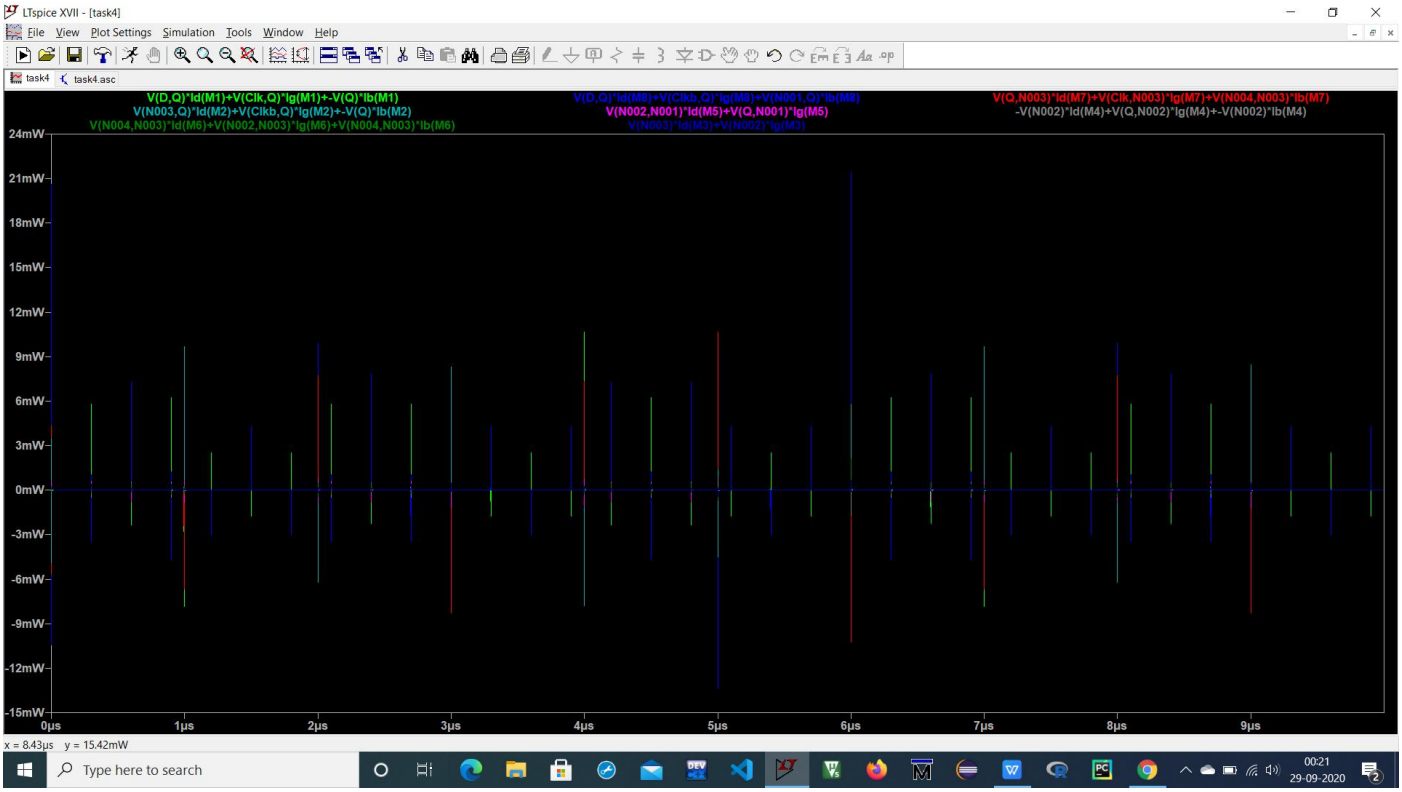
Clk=1
V1=1.8
V2=1.8
Tdelay=0
Trise=1p
Tfall=1p
Ton=2u
Tperiod=4u
Ncycles=10

OBSERVATION:-

1) When clk=1 as D rises Q also rises.
2) When clk=1 as D falls Q also falls.

POWER ESTIMATION:-




LTspice XVII - [task4]
File View Plot Settings Simulation Tools Window Help
task4 task4.asc
V(D,Q)*Id(M1)+V(Clk,Q)*Ig(M1)+-V(Q)*Ib(M1)
V(N003,Q)*Id(M2)+V(Clkb,Q)*Ig(M2)+-V(Q)*Ib(M2)
V(N004,N003)*Id(M6)+V(N002,N003)*Ig(M6)+V(N004,N003)*Ib(M6)
V(D,Q)*Id(M8)+V(Clkb,Q)*Ig(M8)+V(N001,Q)*Ib(M8)
V(N002,N001)*Id(M5)+V(Q,N001)*Ig(M5)
V(N003)*Id(M3)+V(N002)*Ig(M3)
V(Q,N003)*Id(M7)+V(Clk,N003)*Ig(M7)+V(N004,N003)*Ib(M7)
-V(N002)*Id(M4)+V(Q,N002)*Ig(M4)+-V(N002)*Ib(M4)
24mW
21mW
18mW
15mW
12mW
9mW
6mW
3mW
0mW
-3mW
-6mW
-9mW
-12mW
-15mW
0µs
1µs
2µs
3µs
4µs
5µs
6µs
7µs
8µs
9µs
x = 8.43µs y = 15.42mW
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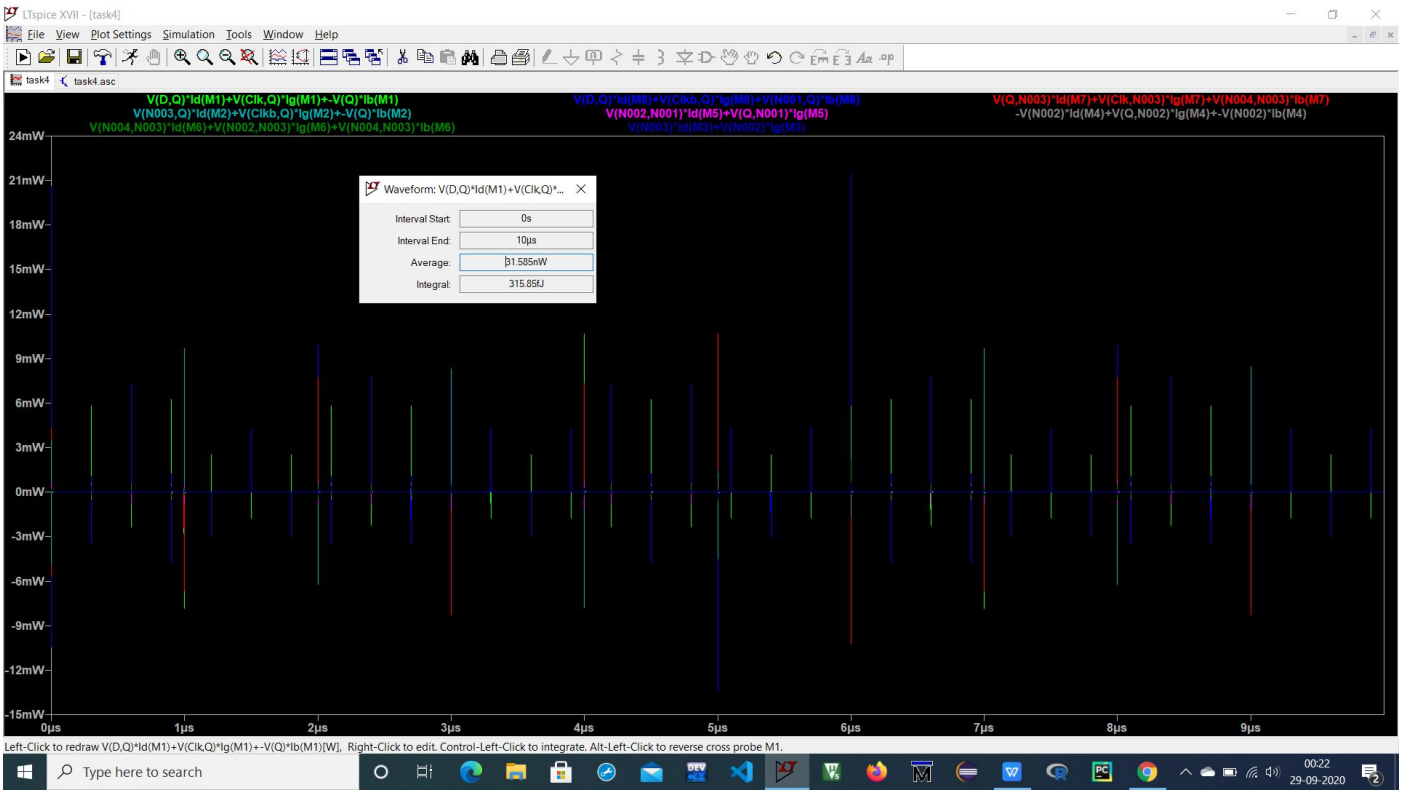
29-09-2020


LTspice XVII - [task4]
File View Plot Settings Simulation Tools Window Help
task4 task4.asc
V(D,Q)*Id(M1)+V(Clk,Q)*Ig(M1)+-V(Q)*Ib(M1)
V(N003,Q)*Id(M2)+V(Clkb,Q)*Ig(M2)+-V(Q)*Ib(M2)
V(N004,N003)*Id(M6)+V(N002,N003)*Ig(M6)+V(N004,N003)*Ib(M6)
V(D,Q)*Id(M8)+V(Clkb,Q)*Ig(M8)+V(N001,Q)*Ib(M8)
V(N002,N001)*Id(M5)+V(Q,N001)*Ig(M5)
V(N003)*Id(M3)+V(N002)*Ig(M3)
V(Q,N003)*Id(M7)+V(Clk,N003)*Ig(M7)+V(N004,N003)*Ib(M7)
-V(N002)*Id(M4)+V(Q,N002)*Ig(M4)+-V(N002)*Ib(M4)
Waveform: V(D,Q)*Id(M1)+V(Clk,Q)*...
Interval Start: 0s
Interval End: 10µs
Average: 31.585nW
Integral: 315.85fJ
24mW
21mW
18mW
15mW
12mW
9mW
6mW
3mW
0mW
-3mW
-6mW
-9mW
-12mW
-15mW
0µs
1µs
2µs
3µs
4µs
5µs
6µs
7µs
8µs
9µs
Left-Click to redraw V(D,Q)*Id(M1)+V(Clk,Q)*Ig(M1)+-V(Q)*Ib(M1)[W], Right-Click to edit. Control-Left-Click to integrate. Alt-Left-Click to reverse cross probe M1.
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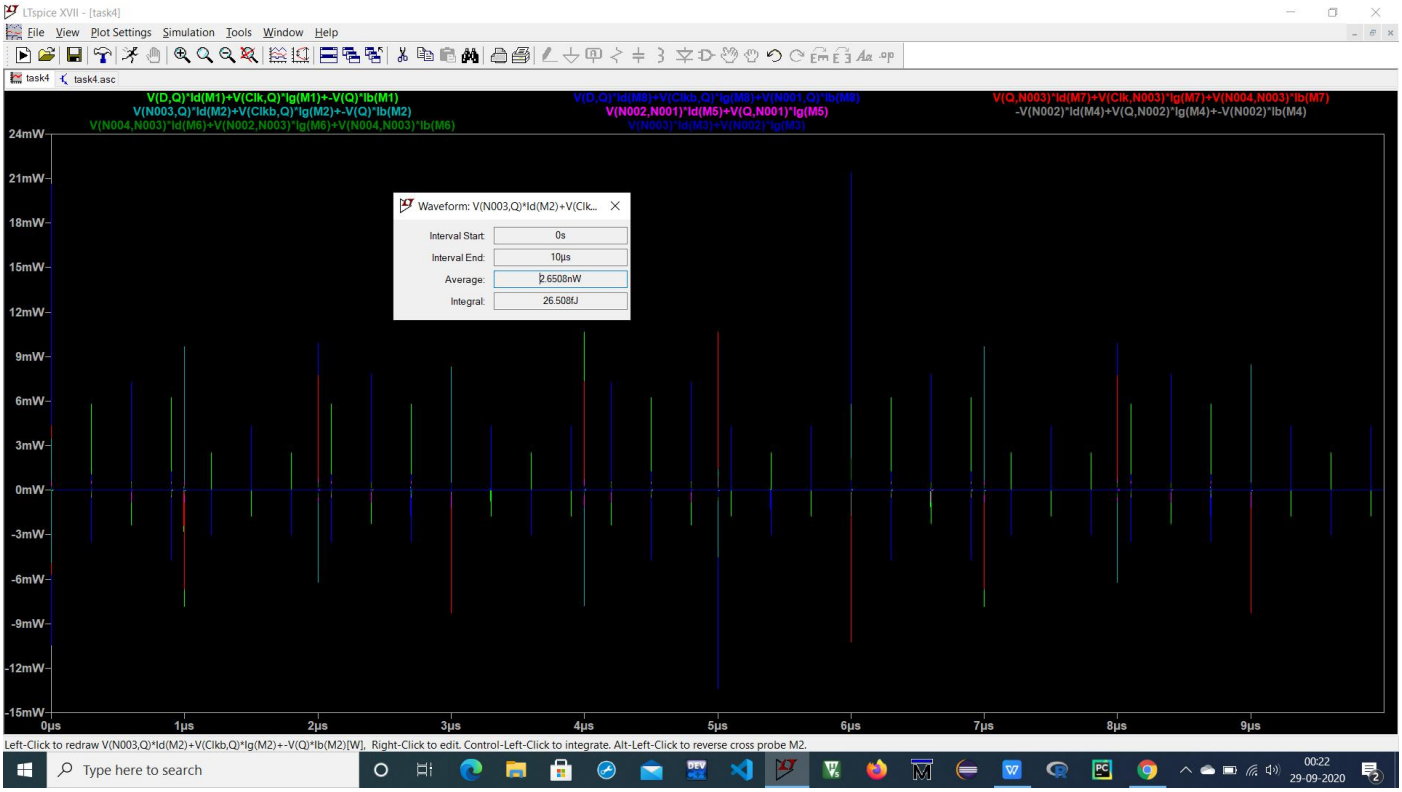
LTspice XVII - [task4]
File View Plot Settings Simulation Tools Window Help
task4 task4.asc
V(D,Q)*Id(M1)+V(Clk,Q)*Ig(M1)+-V(Q)*Ib(M1)
V(N003,Q)*Id(M2)+V(Clkb,Q)*Ig(M2)+-V(Q)*Ib(M2)
V(N004,N003)*Id(M6)+V(N002,N003)*Ig(M6)+V(N004,N003)*Ib(M6)
V(D,Q)*Id(M8)+V(Clkb,Q)*Ig(M8)+V(N001,Q)*Ib(M8)
V(N002,N001)*Id(M5)+V(Q,N001)*Ig(M5)
V(N003)*Id(M3)+V(N002)*Ig(M3)
V(Q,N003)*Id(M7)+V(Clk,N003)*Ig(M7)+V(N004,N003)*Ib(M7)
-V(N002)*Id(M4)+V(Q,N002)*Ig(M4)+-V(N002)*Ib(M4)
Waveform: V(N003,Q)*Id(M2)+V(Clk...
Interval Start: 0s
Interval End: 10µs
Average: 2.6508nW
Integral: 26.508fJ
24mW
21mW
18mW
15mW
12mW
9mW
6mW
3mW
0mW
-3mW
-6mW
-9mW
-12mW
-15mW
0µs
1µs
2µs
3µs
4µs
5µs
6µs
7µs
8µs
9µs
Left-Click to redraw V(N003,Q)*Id(M2)+V(Clkb,Q)*Ig(M2)+-V(Q)*Ib(M2)[W], Right-Click to edit. Control-Left-Click to integrate. Alt-Left-Click to reverse cross probe M2.
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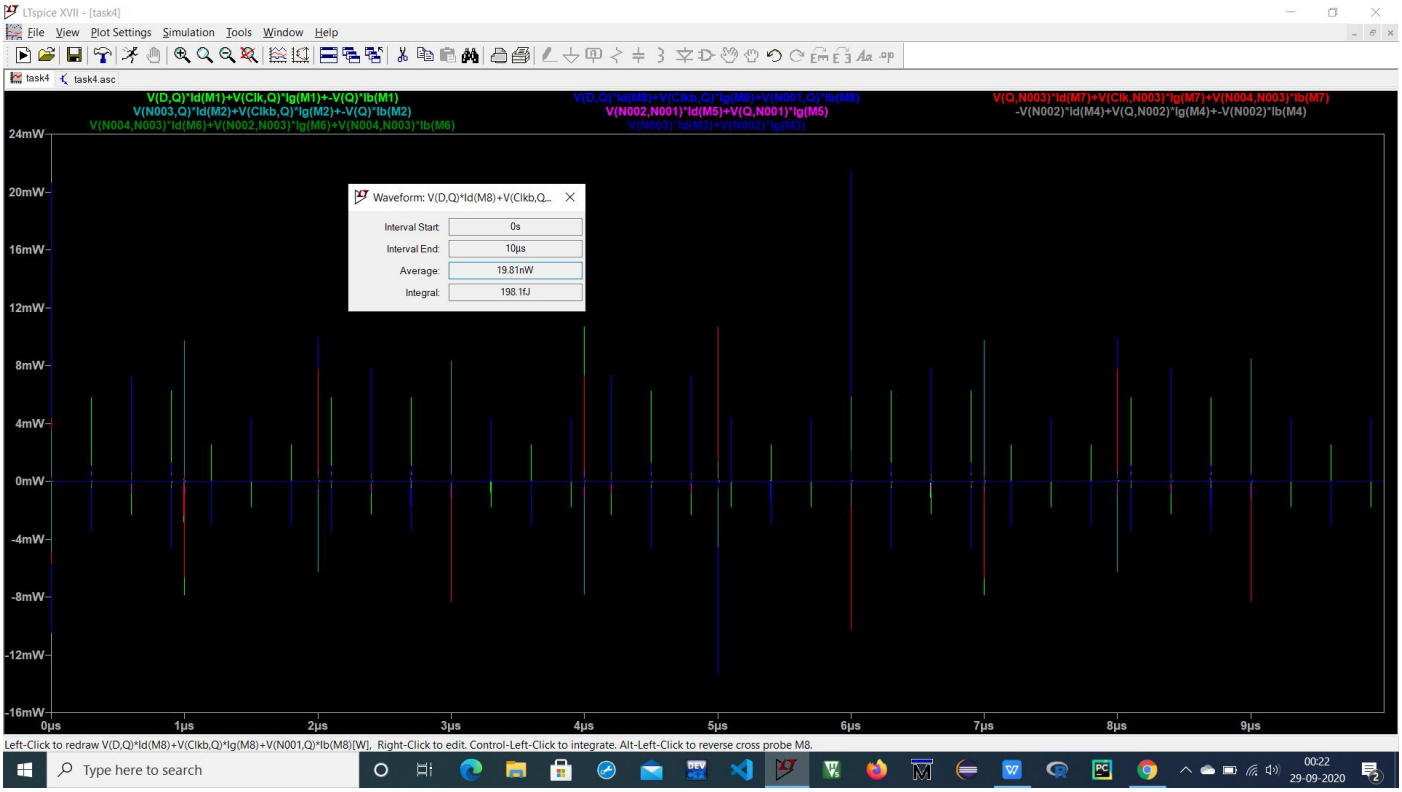
LTspice XVII - [task4]
File View Plot Settings Simulation Tools Window Help
task4 task4.asc
V(D,Q)*Id(M1)+V(Clk,Q)*Ig(M1)+-V(Q)*Ib(M1)
V(N003,Q)*Id(M2)+V(Clkb,Q)*Ig(M2)+-V(Q)*Ib(M2)
V(N004,N003)*Id(M6)+V(N002,N003)*Ig(M6)+V(N004,N003)*Ib(M6)
V(D,Q)*Id(M8)+V(Clkb,Q)*Ig(M8)+V(N001,Q)*Ib(M8)
V(N002,N001)*Id(M5)+V(Q,N001)*Ig(M5)
V(N003)*Id(M3)+V(N002)*Ig(M3)
V(Q,N003)*Id(M7)+V(Clk,N003)*Ig(M7)+V(N004,N003)*Ib(M7)
-V(N002)*Id(M4)+V(Q,N002)*Ig(M4)+-V(N002)*Ib(M4)
Waveform: V(D,Q)*Id(M8)+V(Clkb,Q...
Interval Start: 0s
Interval End: 10µs
Average: 19.81nW
Integral: 198.1fJ
24mW
20mW
16mW
12mW
8mW
4mW
0mW
-4mW
-8mW
-12mW
-16mW
0µs
1µs
2µs
3µs
4µs
5µs
6µs
7µs
8µs
9µs
Left-Click to redraw V(D,Q)*Id(M8)+V(Clkb,Q)*Ig(M8)+V(N001,Q)*Ib(M8)[W], Right-Click to edit. Control-Left-Click to integrate. Alt-Left-Click to reverse cross probe M8.
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CALCULATIONS:-

Propagation Delay:-

When clk=1;

Q=D

Hence
T1=5.700016us
T2=5.700005us

Hence Tpdf=T2-T1=11.01ps.

For Rise Delay

T1=1.8000163us
T2=1.8000005us

Hence Tdpr=T2-T1=15.8ps.

Average Power Calculation:-

M1	31.555nW
M2	2.650nW
M3	64.121nW
M4	19.81nW
M5	47.755nW
M6	24.617nW
M7	20.486nW
M8	65.755nW

Avg Power=276.775nW

INFERENCE:-

1) From Above Experiment it is observed that when clk=0 Q=Q and clk=1 Q=D.

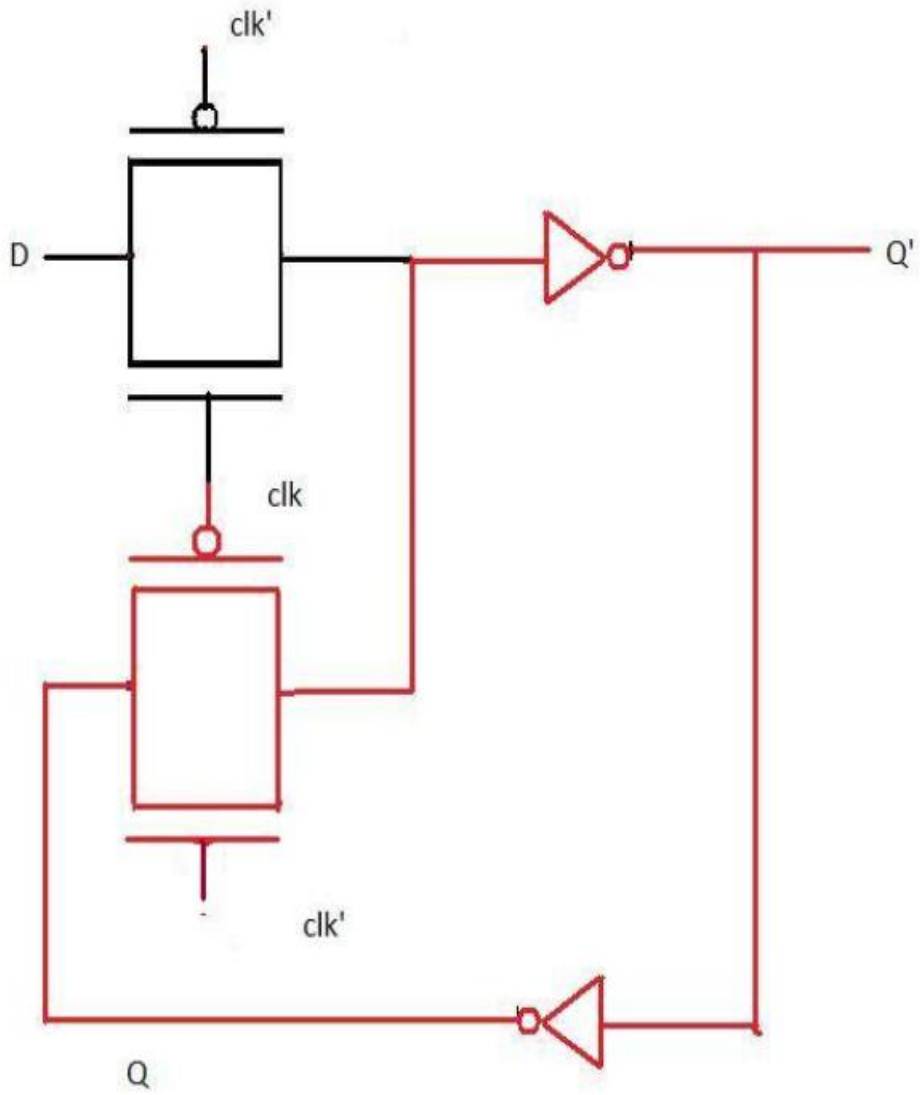
2) D flip flop can be considered as a basic memory cell because it stores the value on the data line with the advantage of the output being synchronised to a clock. D flip flops form the basis of shift registers that are used in many electronic device. Many

logic synthesis tool use only D flip flop or D latch. FPGA contains edge triggered flip flops. D flip flops are also used in finite state machines.

3) When clock is 1 the pass transistor in red is on (the input to the gate of nmos is 1 and to the gate of pmos is 0) therefore the output is D as D changes the output changes accordingly.The two inverters act as a buffer.

4) When clock is 0 the pass transistor in red is on and the one connected to the input D is off thus any changes in D does not affect the circuit.If we observe the transistor in red is connected to the buffer at the output which loops back to its input thus the same value occurs at Q' again and again till this pass transistor is on.

Diagram:-



TRUTH TABLE:-

Clk	D	Q		Description
↓ » 0	X	Q	$\overline{Q}$	Memory no change
↑ » 1	0	0	1	Reset Q » 0
↑ » 1	1	1	0	Set Q » 1