

INGENIØRHØJSKOLEN AARHUS

DIGITAL SYSTEM DESIGN

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## JOURNAL 1

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HOLD 50

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## Øvelse 2

### Opgave 1 - Half-adder

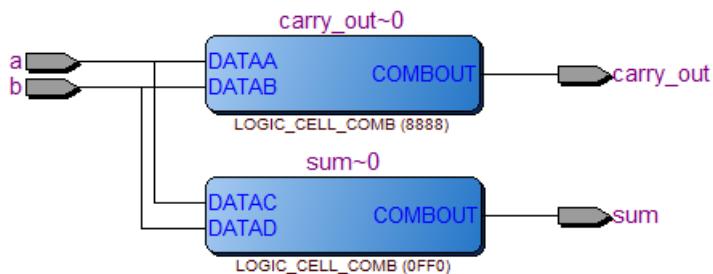
- 1) Architecture body i VHDL kan skrives på tre forskellige måder; dataflow, behavioral og structural.

Half-adder beskrives i Dataflow style ved hjælp af direkte implementering af logiske gates. Skrivemåden gør det nemt at overføre programmet direkte til hardware og de logiske gates.

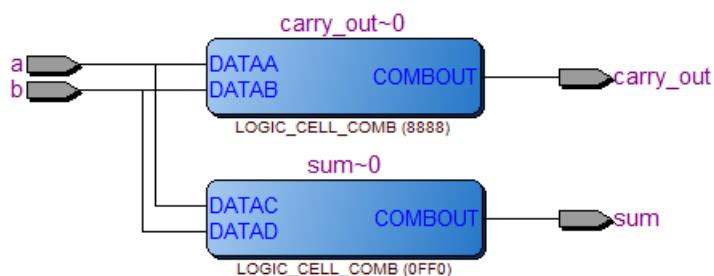
I Behavioral style opskrives half-adderen ved brug af if/else statements. Dette giver en god forståelse af selve half-adderens funktion, men det er kompliceret at overføre det til logiske gates ud fra kodens syntax.

I structural style laves et miks af de to ovenstående, da der først defineres en funktion for hver logisk gate som det ses i dataflow style, og derefter implementeres funktionerne i halfadder entity'en. Denne style er god at bruge, hvis man skal implementere en funktion flere gange.

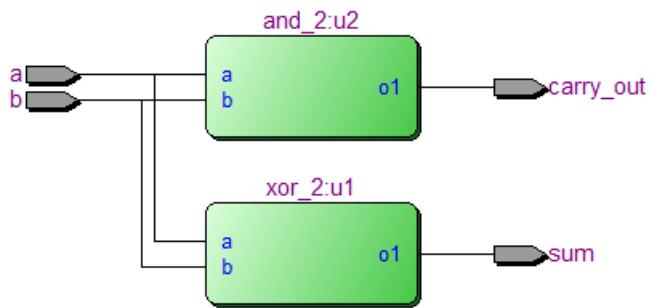
- 2) Et RTL view af de tre forskellige måder at skrive en half-adder på, giver følgende forskellige resultater:



Figur 1: Half-adder - Behavioral RTL view



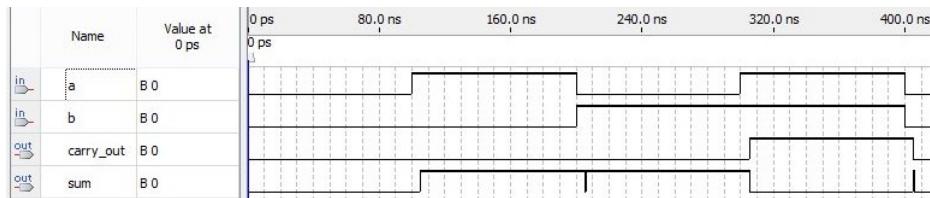
Figur 2: Half-adder - Dataflow RTL view



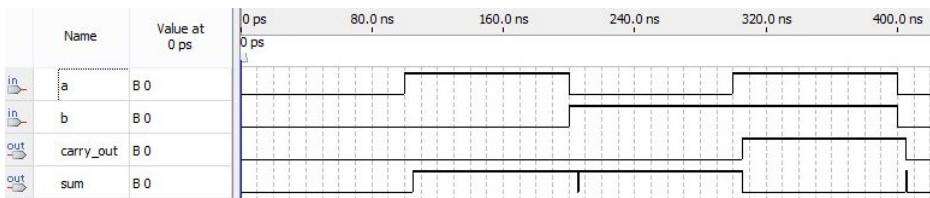
Figur 3: Half-adder - Structural RTL view

Ud fra ovenstående figurer ses det, at dataflow-style og behavioral-style "afkodes" på samme vis, hvor de blå bokse symboliserer en logisk funktion. I structural-style angiver de grønne bokse, også logiske funktioner, men disse er defineret af os, som hhv en AND-funktion og en XOR-funktion. Det er altså med structural-style at vi nemmest kan se, hvilke gates vi skal bruge i en fysisk opbygning af systemet.

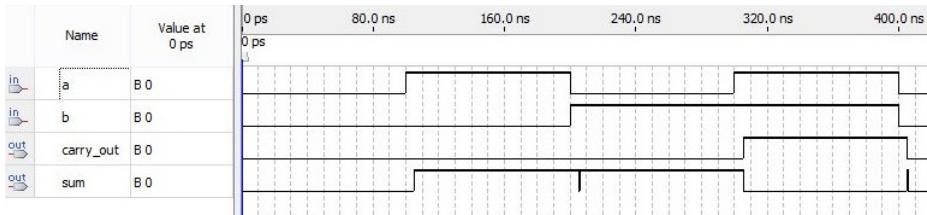
3) Følgende tre figurer viser en Timing simulation af hver style.



Figur 4: Half-adder - Behavioral Timing Simulation



Figur 5: Half-adder - Dataflow Timing Simulation

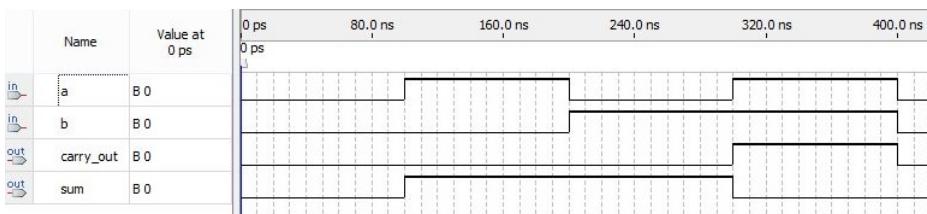


Figur 6: Half-adder - Structural Timing Simulation

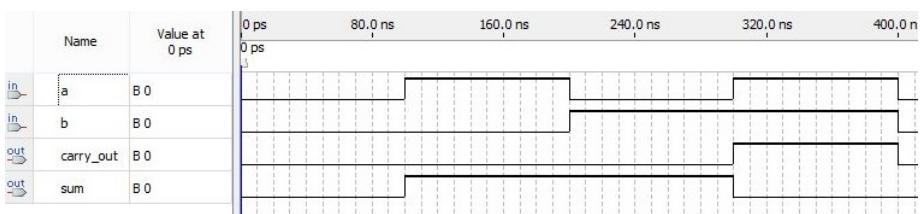
Som det ses på figurerne, forekommer der nogle spikes på funktionerne. Dette skyldes static hazard, da de "gates" vi bruger i vores half-adder, vil have en lille tidsforskydning fra hinanden, og dermed kan give forkerte resultater i brøkdelen af et nanosekund, som det eksempelvis ses når både a-signalet og b-signalet ændrer status.

- 4) For at undgå disse spikes laver vi en functional simulation. Denne slags simulering tager højde for static hazard, og optimerer diagrammet til at vise et "perfekt" resultat.

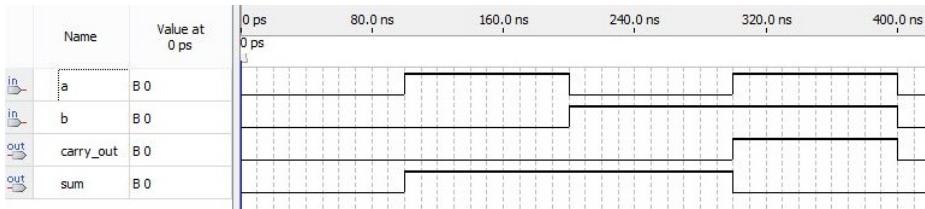
Figur 7, 8 og 9 viser denne type simulering.



Figur 7: Half-adder - Dataflow functional Simulation



Figur 8: Half-adder - Behavioral functional Simulation



Figur 9: Half-adder - Structural functional Simulation

## Opgave 2 - Full-adder

- Med to half-addere kan man lave en full-adder. Dette vil vi nu implementere i hhv. dataflow-style, behavioral-style og structural-style.

Kode 1: Full-adder Dataflow VHDL kode

```

1  library ieee;
2  use ieee.std_logic_1164.all;
3
4  entity full_adder_dataflow is
5  port (a, b, carry_in : in std_logic;
6        sum, carry_out : out std_logic);
7  end full_adder_dataflow;
8
9  architecture dataflow of full_adder_dataflow is
10
11 signal s1, s2, s3 : std_logic;
12 begin
13 s1 <= a xor b;
14 sum <= s1 xor carry_in;
15 s2 <= s1 and carry_in;
16 s3 <= a and b;
17 carry_out <= s2 or s3;
18
19 end dataflow;

```

Kode 2: Full-adder Behavioral VHDL kode

```

1  library ieee;
2  use ieee.std_logic_1164.all;
3
4  entity full_adder_behavioral is
5  port (a, b, carry_in : in std_logic;
6        sum, carry_out : out std_logic);
7  end full_adder_behavioral;
8
9  architecture behavioral of full_adder_behavioral
10
11 signal s1, s2, s3 : std_logic;

```

```

12  begin
13  fa: process (carry_in, a, b)
14  begin
15  if carry_in = '0' then
16
17  if a = '1' then
18  sum <= not b;
19  carry_out <= b;
20  else
21  sum <= b;
22  carry_out <= '0';
23  end if;
24  else
25  sum <= a xnor b;
26  carry_out <= a or b;
27  end if;
28  end process fa;
29
30  end behavioral;

```

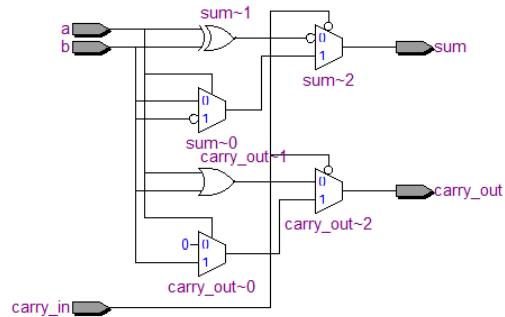
Kode 3: Full-adder Structural VHDL kode

```

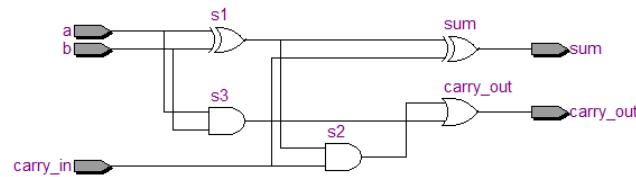
1  library ieee;
2  use ieee.std_logic_1164.all;
3
4  entity full_adder_structural is
5  port (a, b, carry_in : in std_logic;
6  sum, carry_out : out std_logic);
7  end full_adder_structural;
8
9  architecture structural of full_adder_structural
10 is
11
12 signal s1, s2, s3 : std_logic;
13 begin
14
15 ha1: entity work.half_adder_dataflow port map (a
16     => a, b => b, sum => s1, carry_out => s3);
17 ha2: entity work.half_adder_dataflow port map (a
18     => s1, b => carry_in, sum => sum, carry_out
     => s2);
19 or1: entity work.or_2 port map (i1 => s2, i2 =>
     s3, o1 => carry_out);
20
21 end structural;

```

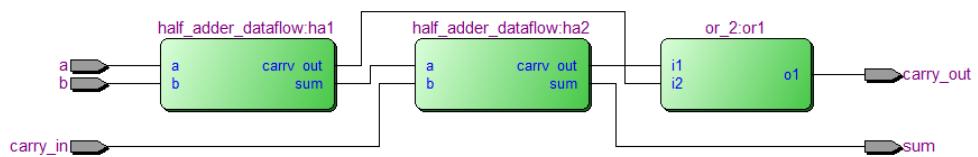
2) Med et RTL view kan vi se hvordan de tre forskellige koder vil blive omdannet til logiske gates.



Figur 10: Full-adder - Behavioral RTL view

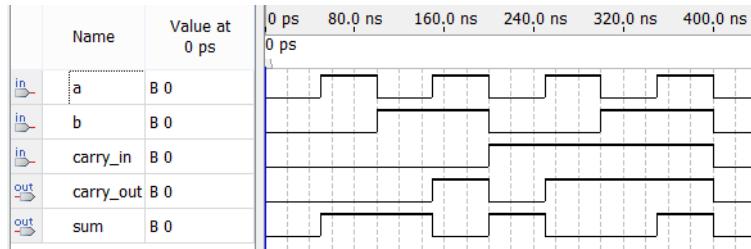


Figur 11: Full-adder - Dataflow RTL view

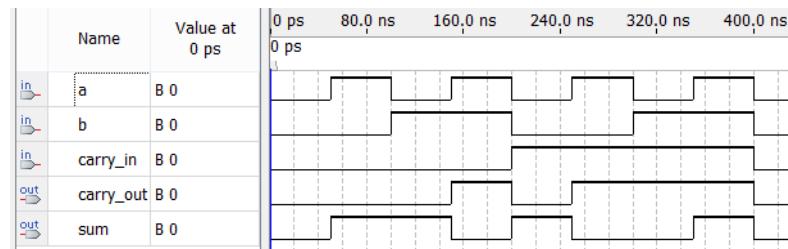


Figur 12: Full-adder - Structural RTL view

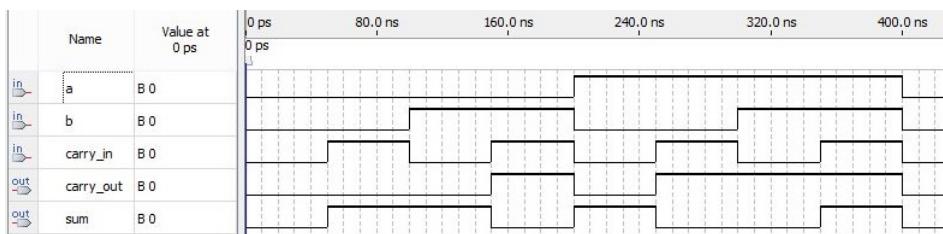
- 3) Til sidst laver vi en functional simulering for at se om vores tre full-adder koder opfører sig som vi ønsker.



Figur 13: Full-adder - Dataflow functional Simulation



Figur 14: Full-adder - Behavioral functional Simulation



Figur 15: Full-adder - Structural functional Simulation

## Øvelse 3

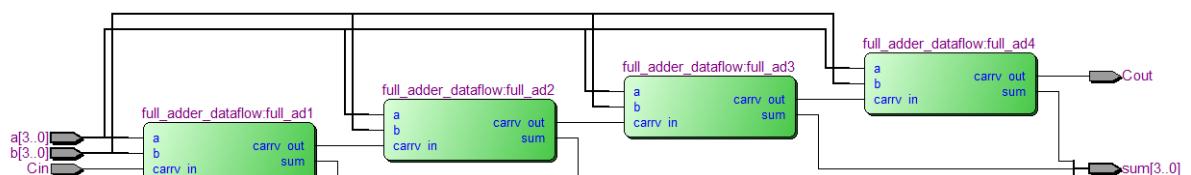
### Opgave 1 - Four bit parallel adder

- Vi designer en 4 bit parallel adder i structural style ved hjælp af den dataflow-style four bit full adder, vi har lavet i øvelse 2 (se Kode 1)

Kode 4: Four bit parallel adder Structural VHDL kode

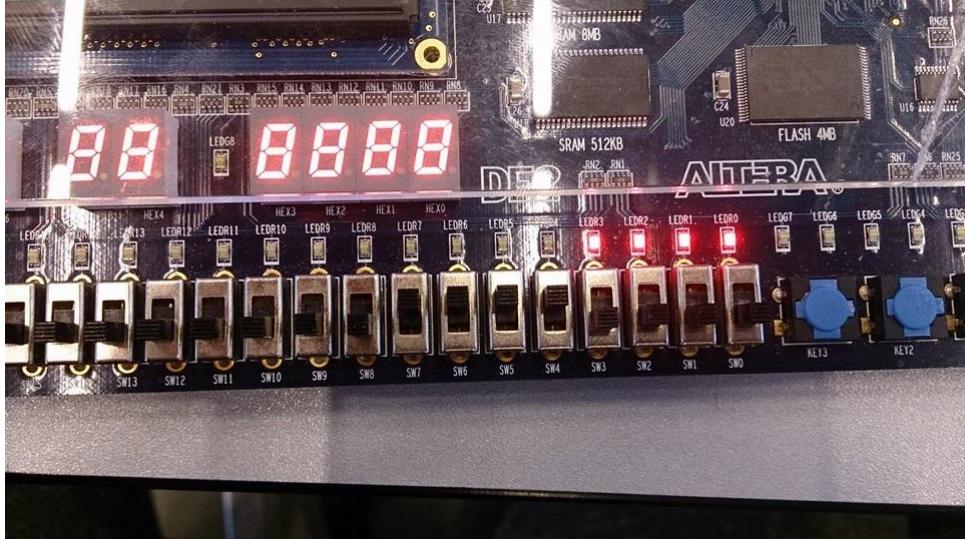
```
1  library ieee;
2  use ieee.std_logic_1164.all;
3
4  entity four_bit_full_adder is
5    port (a: in std_logic_vector (3 downto 0);
6          b: in std_logic_vector (3 downto 0);
7          Cin: in std_logic;
8          sum: out std_logic_vector (3 downto 0);
9          Cout: out std_logic);
10
11 end four_bit_full_adder;
12
13 architecture structural of four_bit_full_adder is
14
15   signal i1, i2, i3 : std_logic;
16 begin
17   full_ad1 : entity work.full_adder_dataflow port
18     map (a => a(0), b => b(0), carry_in => cin,
19           sum => sum(0), carry_out => i1 );
20   full_ad2 : entity work.full_adder_dataflow port
21     map (a => a(1), b => b(1), carry_in => i1,
22           sum => sum(1), carry_out => i2 );
23   full_ad3 : entity work.full_adder_dataflow port
24     map (a => a(2), b => b(2), carry_in => i2,
25           sum => sum(2), carry_out => i3 );
26   full_ad4 : entity work.full_adder_dataflow port
27     map (a => a(3), b => b(3), carry_in => i3,
28           sum => sum(3), carry_out => Cout );
29
30 end structural;
```

- Vi kan ved hjælp af RTL-viewer se, om vores full adders er forbundet korrekt:



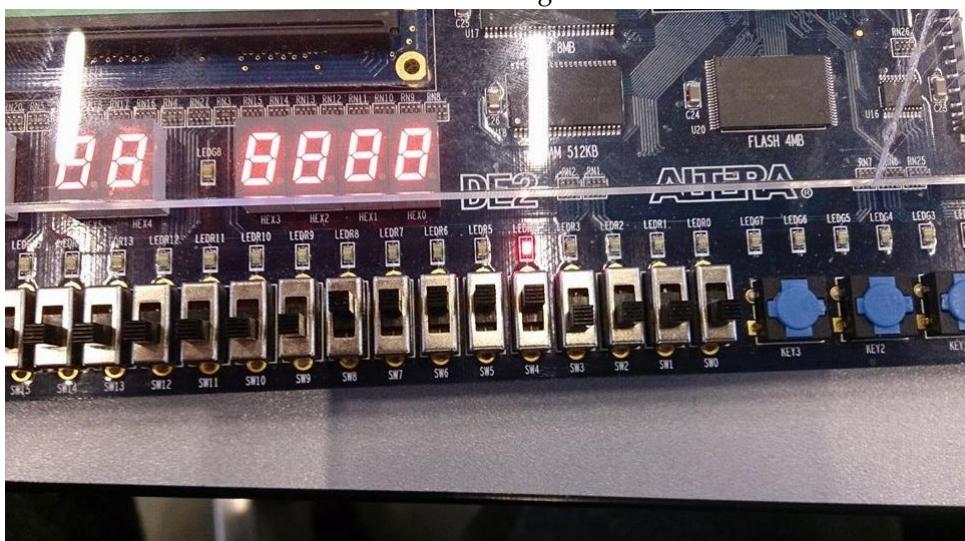
Figur 16: Four bit parallel adder - Structural RTL view

- 3) Vi starter med at sætte bits til 00001111 samt cin 0 og får det forventede resultat:



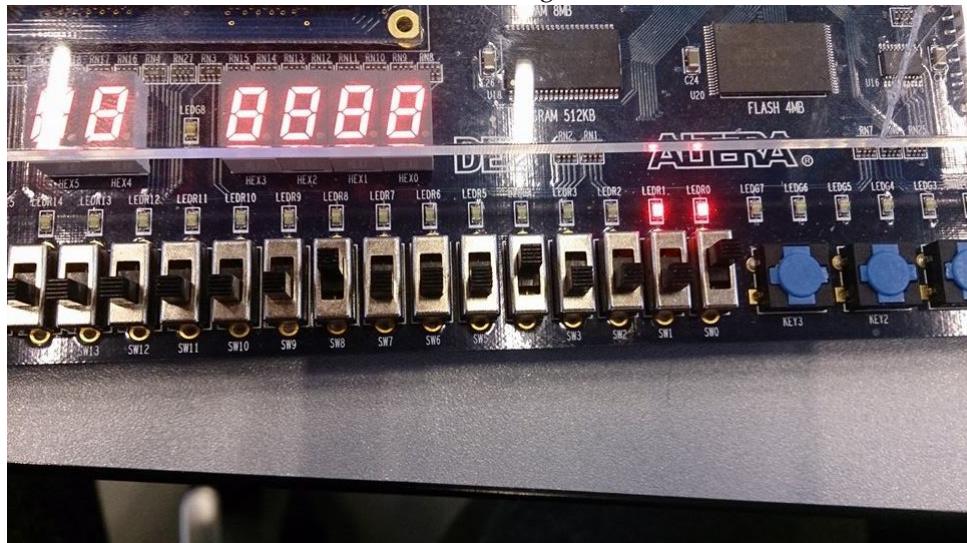
Figur 17: Four bit parallel adder - 00001111,  $\text{cin}=0$

Vi sætter nu bits til 11110000 samt cin 1 og får det forventede resultat:



Figur 18: Four bit parallel adder - 11110000,  $\text{cin}=1$

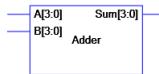
Vi sætter nu bits til 00010001 samt cin 1 og får det forventede resultat:



Figur 19: Four bit parallel adder - 00010001, cin=1

## Opgave 2 - Four bit adder - using signed/unsigned logic

- 1) Vi laver en unsigned adder i dataflow style som vist på figur 20. Da input og output skal være af std logic vector typen, og vi skal bruge + operatoren, bliver vi nødt til at konvertere til unsigned først. Se Kode 5



Figur 20: Four bit unsigned adder

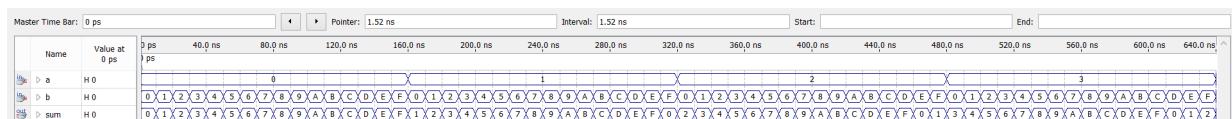
Kode 5: Four bit unsigned adder Dataflow VHDL kode

```

1 library ieee;
2 use ieee.std_logic_1164.all;
3 use ieee.numeric_std.all;
4
5 entity unsigned_adder is
6 port (a: in std_logic_vector (3 downto 0);
7 b: in std_logic_vector (3 downto 0);
8 sum: out std_logic_vector (3 downto 0));
9 end unsigned_adder;
10
11 architecture dataflow of unsigned_adder is
12 begin
13
14     sum <= std_logic_vector(unsigned(a) + unsigned(b))
15     );
16 end dataflow;

```

- 2) Vi tester nu vores kode med en functional simulation:



Figur 21: Four bit unsigned adder Functional simulation

- 3) Vi sætter nu bits til 1000 + 0100 og får det forventede resultat som det ses på Figur 22



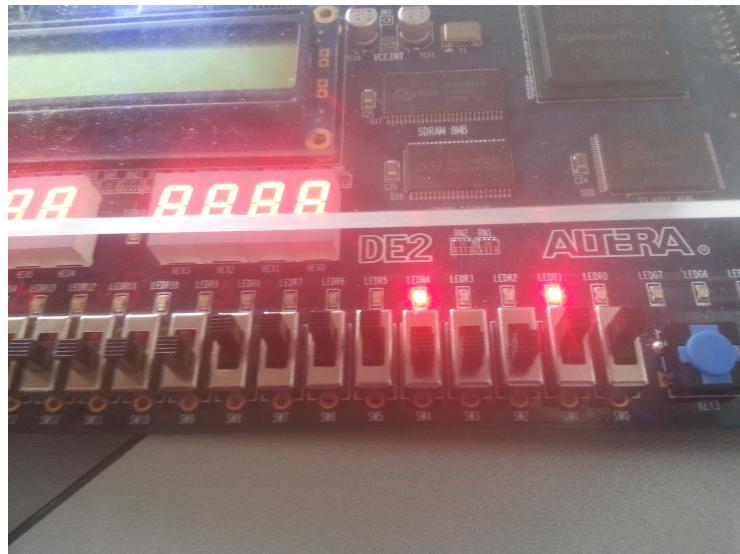
Figur 22: Four bit unsigned adder - 1000 + 0100

- 4) Vi ændrer nu koden så det bliver en signed adder som det ses i Kode 6. Vi tester det på vores DE2 board, og ser at der ingen forskel er på unsigned adderen og signed adderen som det ses på Figur 23. Dette skyldes at selve bit'sne ikke er anderledes, men det er kun måden de skal tolkes på.

Kode 6: Four bit signed adder Dataflow VHDL kode

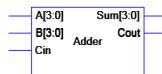
```

1  library ieee;
2  use ieee.std_logic_1164.all;
3  use ieee.numeric_std.all;
4
5  entity unsigned_adder is
6  port (a: in std_logic_vector (3 downto 0);
7  b: in std_logic_vector (3 downto 0);
8  sum: out std_logic_vector (3 downto 0));
9  end unsigned_adder;
10
11 architecture dataflow of unsigned_adder is
12 begin
13
14  sum <= std_logic_vector(unsigned(a) + unsigned(b))
15  );
end dataflow;
```



Figur 23: Four bit signed adder - 1000 + 0100

- 5) Vi laver nu vores unsigned adder om, så den også virker med et carry in, og leverer et carry out som vist på Figur 24. Vi benytter os af resize funktionen, samt laver nogle interne signaler, inden vi sender resultatet ud igen. Koden ses i Kode 7.



Figur 24: Four bit unsigned adder with carry

Kode 7: Four bit unsigned adder with carry Dataflow VHDL kode

```

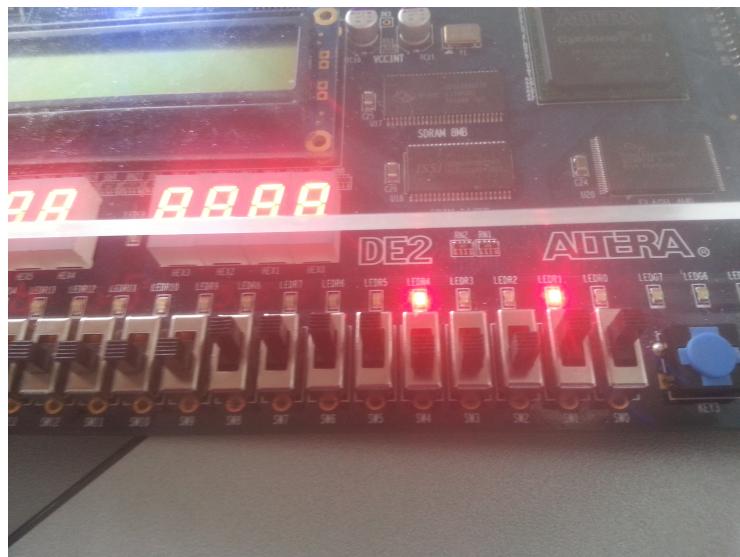
1  library ieee;
2  use ieee.std_logic_1164.all;
3  use ieee.numeric_std.all;
4
5  entity unsigned_adder_carry is
6    port (a: in std_logic_vector (3 downto 0);
7          b: in std_logic_vector (3 downto 0);
8          carry_in: in std_logic;
9          carry_out : out std_logic_vector (0 downto 0);
10         sum: out std_logic_vector (3 downto 0));
11  end unsigned_adder_carry;
12
13  architecture dataflow of unsigned_adder_carry is
14    signal c : unsigned (3 downto 0);
15    signal s : unsigned (4 downto 0);
16    begin
  
```

```

17   c <= "000" & carry_in;
18   s <= resize(unsigned(a),5) + resize(unsigned(b)
19     ,5) + resize(c,5) ;
20   sum <= std_logic_vector(s(3 downto 0));
21   carry_out <= std_logic_vector(s(4 downto 4));
end dataflow;

```

- 6) Vi overfører vores adder til DE2 boardet. Her adderer vi  $1110 + 0011$  samt carry in = 1, og får det forventede resultat som ses på figur 25.



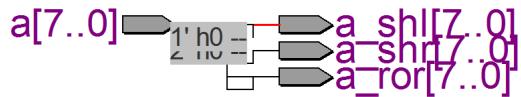
Figur 25: Four bit unsigned adder with carry

### Opgave 3 - Concatenation

Kode 8: Concatenation kode

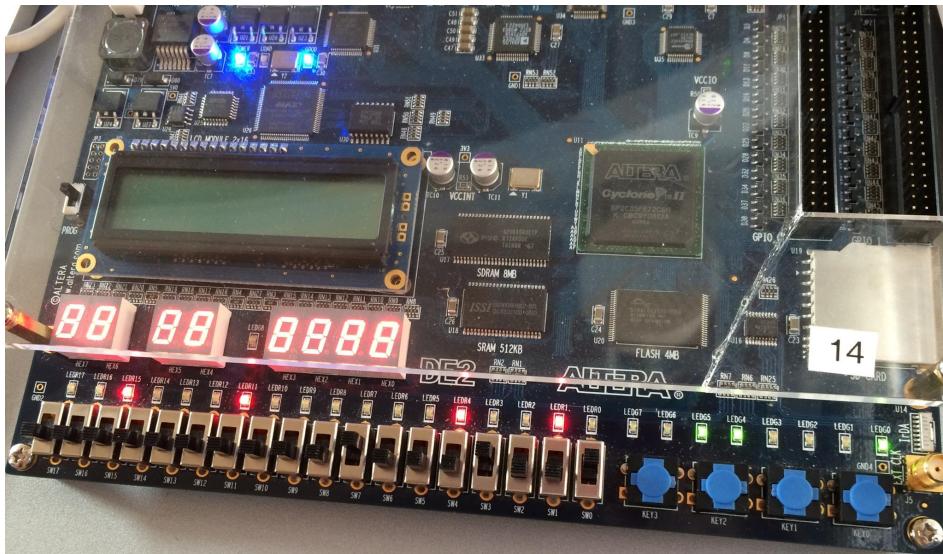
```
1) 1) library ieee;
2)  use ieee.Std_logic_1164.all;
3)
4) entity shift_div is
5) port (a : in std_logic_vector(7 downto 0);
6)       a_shl,a_shr,a_ror: out std_logic_vector(7 downto
7)           0));
8) end shift_div;
9)
10) architecture dataflow of shift_div is
11) begin
12)   a_shl <= a(6 downto 0) & '0';
13)
14)   a_shr <= "00" & a(7 downto 2);
15)
16)   a_ror <= a(2 downto 0) & a(7 downto 3);
17)
18) end dataflow ;
```

- 2) Vi kan se på figur 26 fra RTL-viewer, at der ikke er nogen logiske elementer i kodestykket:



Figur 26: Concatenation RTL

- 3) Vi overfører programmet til DE2-boardet. Inputtet a sættes som SW[7:0], output a-shl sættes til LEDR[7:0], a-shr sættes til LEDR[17:10] og a-ror sættes til LEDG[7:0]. Dette kan ses på figur 27.



Figur 27: Concatenation på DE2-board

#### Opgave 4 - Subtype

- 1) Vi opskriver koden for en 4-bit subtractor som ses i kode 9

Kode 9: Subtractor kode

```

1 library ieee;
2 use ieee.std_logic_1164.all;
3
4 entity Subtypes is
5 port (a,b : in std_logic;
6 c : out std_logic);
7 end Subtypes;
8
9 architecture dataflow of Subtypes is
10 subtype bool is std_logic range '1' to 'Z';
11 signal tmp : bool;
12 begin
13 tmp<= 'U';
14 c<= b and tmp;
15 end dataflow;
```

Grunden til at vi får fejlen at U er udenfor rækkevidde ses på figur 28 nedenfor:

Value	State	Strength
U	uninitialized	none
X	unknown	forcing
0	0	forcing
1	1	forcing
Z	none	high impedance
W	unknown	weak
L	0	weak
H	1	weak
-	don't care	none

Figur 28: Stater og styrker for std\_ulogic værdier

Derfor retter vi til koden

Kode 10: Rettet subtractor kode

```

1 library ieee;
2 use ieee.std_logic_1164.all;
3
4 entity Subtypes is
5 port (a,b : in std_logic;
6 c : out std_logic);
7 end Subtypes;
8
9 architecture dataflow of Subtypes is
10 subtype bool is std_logic range 'U' to 'Z';
11 signal tmp : bool;
12 begin
13 tmp<= 'U';
14 c<= b and tmp;
15 end dataflow;
```

## Øvelse 4

### Opgave 1: Combinational VHDL

- 2) WHAT DA FUCK IS WRONG WITH UUU!

### Opgave 2: Binary to Decimal Conversion

- 1) Vi har læst koden for BCD decoderen og er indforstået med hvad der fungerer hvordan, og hvorfor.
- 2)