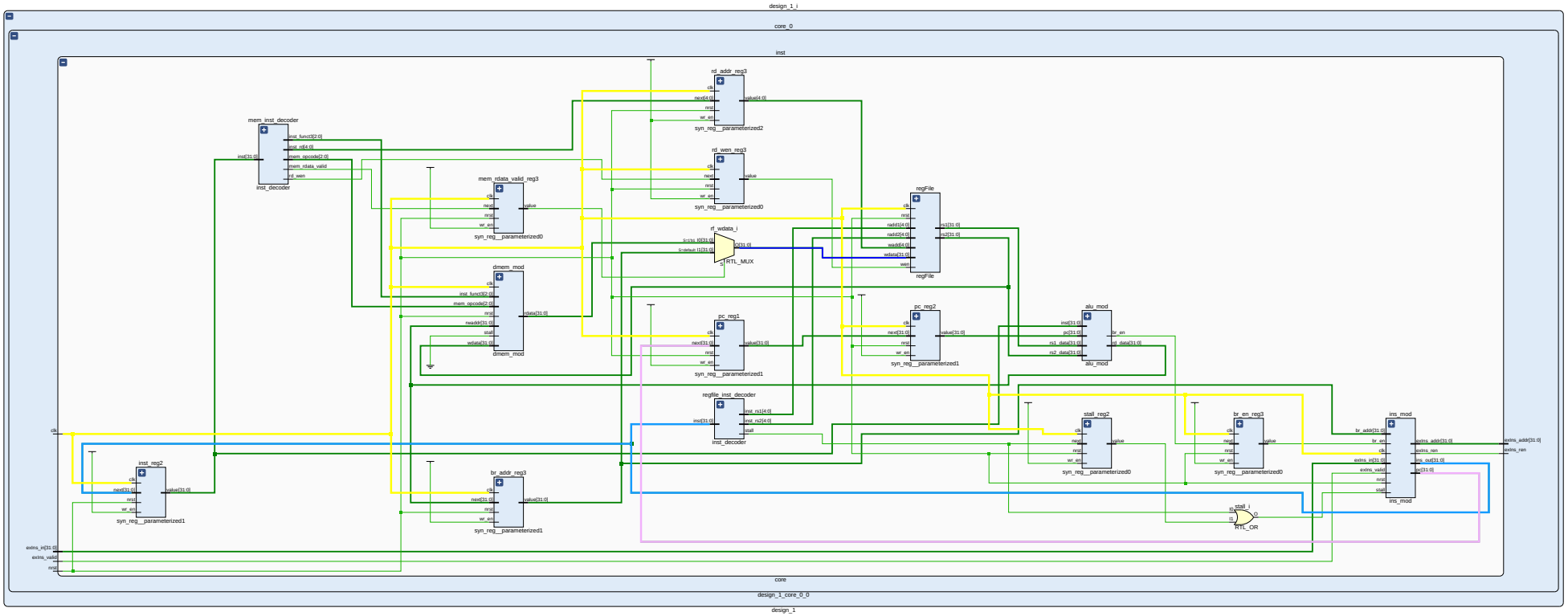
design_1_i
core_0
inst
mem_inst_decoder
inst_decoder
rd_addr_reg3
syn_reg__parameterized2
rd_wen_reg3
syn_reg__parameterized0
mem_rdata_valid_reg3
syn_reg__parameterized0
rf_wdata_i
RTL_MUX
regFile
dmem_mod
pc_reg1
syn_reg__parameterized1
pc_reg2
syn_reg__parameterized1
alu_mod
regfile_inst_decoder
inst_decoder
stall_reg2
syn_reg__parameterized0
br_en_reg3
syn_reg__parameterized0
ins_mod
inst_reg2
syn_reg__parameterized1
br_addr_reg3
syn_reg__parameterized1
stall_i
RTL_OR
clk
exins_in[31:0]
exins_valid
nrst
exins_addr[31:0]
exins_ren
core
design_1_core_0_0
design_1