RMIT UNIVERSITY

SCHOOL OF ENGINEERING

EEET2162 / 2035 – ADVANCED DIGITAL DESIGN 1 / DESIGN WITH HARDWARE DESCRIPTION LANGUAGES

LABORATORY PROJECT

TOPIC LIST AND ASSESSMENT GUIDELINES - 2022

1 AIMS

(i) To design, simulate, implement and test a digital circuit using the Quartus Prime toolchain.

(ii) To demonstrate the workflow when using the Verilog HDL to construct a design for a physical Field Programmable Gate Array (FPGA) target.

(iii) To develop a hierarchical design where an emphasis is placed on the development of small sub-modules which can be replicated to form a complete system.

(iv) To develop a large-scale Verilog HDL project that will require numerous sub-modules that are required to work together to achieve a common complex task.

2 INTRODUCTION

Students are expected to work in pairs and submit a combined report / Verilog project which will be assessed by the Course Coordinator. The projects will run for four weeks (Weeks 8, 9, 10, 11), however the submissions and demonstration will occur in Week 12. Students will need to strictly select a project partner from the same laboratory session (whether online or face-to-face classes) and in the same course.

The aim of the projects is to allow groups (maximum of two) of students to build relatively complex designs in Verilog HDL that can be deployed on the DE-10 Nano Development Platform. All work must be original, and plagiarism will be taken very seriously. The projects are expected to require approximately 36 hours per student to be completed successfully.

The topics have also been devised to allow students with varying skill levels to select a project that is suitable for their knowledge. The entire assessment (report and demonstration) will be scaled according to the difficulty level. As the semester is not yet complete, not all relevant material has been presented, however all students should have enough knowledge to begin working on the actual topic as of week 8. More details will be presented during the remainder of the lecture series.

The topics and outcomes presented in Section 3.0 are non-negotiable and students must select from the provided list unless a prior arrangement has been made with the Course Coordinator. Furthermore, students are required to inform their Laboratory Demonstrator as to which project they have selected.

Where possible the designs should be constructed from the 'fundamental units'. As example, a full-adder should be built (as demonstrated in Lecture 7) rather than the "+1'b1" code segment be used as this would allow the design to be further developed into an Application Specific Integrated Circuit (ASIC).

3 TOPIC LIST 2022

a) HDMI processing and overlay (on-screen display) using the Cyclone V

Difficulty Level: Distinction.

The DE-10 Nano Development Platform contains an Analog Devices ADV7513 HDMI Transmitter. This particular device is connected to the FPGA using a 24-bit wide bus as well as an array of control signals. The aim of this project is to use both the FPGA and the ADV7513 to produce an on-screen display.

As an example, an image can be loaded into the onboard RAM (FPGA or SoC DDR3 RAM) and then displayed over the HDMI interface. Once the image has been loaded an onscreen overlay should present some user-configurable text over the image. Whilst a static image is acceptable, higher marks will be awarded to students who can display a moving image loaded from one of the other interfaces available on the development platform.

The ADV7513 also contains a series of configuration registers which will need to be made accessible over an interface such as I2C.

b) Platform Designer implementation of an SPI communication interface

Difficulty Level: High Distinction.

One issue with the DE-10 Nano Development Platform is that it is quite difficult to interface with using standardised interfaces such as SPI or I2C. This is due to the fact that the FPGA needs to be configured with a block that contains the required functionality as the Hard Processor System (HPS) contains limited external interfaces. In this project, students will need to develop a configurable width (minimum 1-bit, maximum 32-bits) SPI interface that can be used to transmit data / receive data. A maximum serial clock (SCLK) of 25MHz is required.

It is suggested that the interface is modelled on a standard ARM processor such as the STM32F4. Note that IP Blocks (with the exception of a PLL) are not permitted in this project. The system is also required to interface with the HPS embedded in the Cyclone V. Additional material will be made available that discusses the software drivers required to communicate with an Avalon Memory Mapped Slave via Platform Designer.

At a minimum, the developed SPI peripheral should be able to have the clock phase and polarity configured, the number of bits transmitted / received configurable and have the ability to act as a master or slave device.

c) Audio signal capture and processing using the onboard ADC.

Difficulty Level: High Distinction.

As the need for real-time processing of multiple channels of audio data increases with more advanced musical instruments many manufacturers are beginning to use FPGAs to perform data processing. This is mainly due to the fact that FPGAs can have multiple parallel data paths that can process each signal independently. If signals need to be combined, then a final stage

can be used to synchronise the audio sources as well as perform and further processing such as equalisation.

The aim of this project will to be capture four channels of audio data using the onboard LTC2308 produced by Analog Devices. A Fast Fourier Transform (using an IP Block) is to then be used on the incoming data and an audio level spectrum analyser developed. The audio signal FFT is to be displayed over the HDMI interface.

Additional hardware will be required to interface the audio sources to the LTC header on the DE-10 Nano Development Platform. Please see the course coordinator for the additional resources if this project is selected.

d) ATmega32A Emulation.

Difficulty Level: High-Distinction.

This project requires students to develop a functionally equivalent micro-controller design that executes a reduced version of the instruction set of the ATmega32A. For the complete instruction set please see the Microchip website (www.microchip.com).

For simplicity, the design does not have to maintain the 4-state timing of the ATmega32A but the implementation must maintain its single level pipelining characteristic. Students will need to investigate techniques to implement the program and data memories.

Omit the reset timer, power-on reset and watchdog circuits. A suggested partitioning is shown below:

Sub-task 1 = Memory and I/O section (includes program memory I-reg & RAM)

Sub-task 2 = All timing functions (includes Timer0 and watchdog – omit power-on reset)

Sub-task 3 = CPU functions.

e) Floating-point Unit Development

Difficulty Level: Credit.

In this project, students are required to develop a structural Floating-Point Unit (FPU) for use with a microprocessor. The processor needs to be capable of floating-point addition and multiplication. The numbers are to be encoded into IEEE 754 single precision 32-bit format. The FPU should also be able to detect and flag the ‘NaN’ cases.

For the project demonstration, interface the FPU to the DE-10 RAM and perform the operation (A* B) + C on 1000 data triplets (A, B, C). Transfer the results back to the RAM, then upload to the PC for display. Verify the results by comparing them with another method (e.g., C program, spreadsheet etc.). It is essential that an external interface is used to transfer the data back to a host PC.

4 ASSESSMENT SCHEDULE

To assess the project both a combined final technical report and group presentation / demonstration are required. The report and Quartus Prime project sources files are due on Friday, Week 12 at 11:59pm and must be submitted electronically to the subject Canvas website. Furthermore, the informal demonstration will nominally occur on both Thursday / Friday of Week 12 (subject to timetable availability). Students are requested to regularly check the Canvas website for updates to the demonstration schedule. Students completing the laboratory component online will be able to schedule an appointment with the Course Coordinator to discuss their outcomes (whether via simulation or deployment to a physical DE-10 Nano).

a) Project Technical Report

Students are required to individually submit a final project technical report (maximum of twelve (15) pages in body of report) describing the work undertaken during the project. The report should be written in such a way that it can be read and understood by another Engineer with a background in FPGA design and development. Note that the same report is to be submitted by both group members. The report (and background material relating to the development of the project including schematics, PCB layouts and source code) must be submitted to the subject Canvas website by Friday, Week 12 at 11:59pm. A late penalty of 10 marks per day (including weekends) will apply if the required content is note received by the due date / time.

As a general guideline the project report should include, but not be limited to, the following sections:

- Title page: include the project title, the date, student ID and name(s) and the revision number.
- Acknowledgements: note (and references) any IP blocks or source code.
- Executive summary: state the main achievements of the project. This is a summary of key findings, achievements, and measurements. It is not an introduction. The words limit is 150.
- Table of contents: section titles and page numbers for your report.
- Introduction: provide an overview and define the scope of the project.
- Literature search: a brief indication of what references and external information were sought and used. The literature review should be limited to technical information that is relevant to explain the concepts and problems addressed in the project.
- Technical work and Results (Students may choose own section titles here): this part may contain a description of the process used to develop the deliverables and a complete description of what has been created. Students can elaborate on their contribution to the project and compare obtained results with those in literature or other known solutions. A clear delineation should exist between existing techniques and solutions and student work. A comparison should be undertaken against the original deliverables of the project and what has been delivered. If discrepancies exist then the reasons should be elaborated (even incorrect or unexpected results and still worth discussing). This section should form the bulk of the report. Technical content may include state diagrams, relevant truth-tables and block diagrams explaining the HDL used in realising the solution. A discussion should be held on the HDL modules developed and their interconnections. Simulation results can also be included in the report to explain / demonstrate project outcomes.
- Discussion and Conclusion: Students should provide a discussion of the (simulation) results, clearly stating their achievements, lessons learnt and possible future works.
- References: All references quoted in the report (where relevant) should be listed down in the manner and style indicated below and numbered sequentially in the order as they appear in the main text. However, the list should not contain any entry that has not been quoted anywhere in the report. The IEEE reference format is to be used.

- Appendices: These must also be properly titled and should contain details which are of secondary importance in understanding the report. Examples include program listings, schematics and detailed specifications of important components. Note that the full HDL solution does not need to appear in the appendices as it is to be submitted electronically.

b) Project Technical Demonstration

Students will be required to demonstrate their complete project to the Course Coordinator in Week 12 at their scheduled time. Each student group will have approximately seven (7) minutes to describe and demonstrate their technical achievements. A further three (3) minutes will be made available for questions. Additional material, such as diagrams and images can be used to support the discussion. The demonstration component accounts for 15% of the overall subject grade and will be individually graded. Note that the demonstration is informal and will generally involve viewing the project outcomes around one of the laboratory computers. Students are requested to ensure that their project is functional prior to the assessment time. No time compensation will be given if the project is not ready to view at the schedule time.

EEET2162 / EEET2035 – Technical Report Assessment Schedule

The EEET2162 / EEET2035 Project Technical Report accounts for a total of 20% of the overall grade for EEET2162 and 25% for EEET2035. The report is to be marked out of 100 and then will be converted to an appropriate percentage. When marking the report factors such as technical complexity, clarity of discussion, background technical literature review, appropriate choice of detail, demonstrated technical skills and analysis of results should be considered. Important concepts must be clearly explained, and sources quoted appropriately.

	0 – 49 (NN)	50 – 59 (PA)	60 – 69 (CR)	70 – 79 (DI)	80 – 100 (HD)
Reference Reading and Theoretical Backing (10%)	Report contains limited relevant background information and restates simple facts. Significant technical errors are present in the report illustrating gaps in knowledge. Irrelevant technical references are included or no references at all. References are not listed in IEEE format.	Basic background theory presented covering the topic on a superficial level and missing key technical details. Technical errors exist in the document which raises concerns on the presented outcome. References may be inappropriate and/or lack technical depth (e.g. use of Wikipedia or opinion pieces). References are not listed in IEEE format.	Technical literature review is sound and covers many of the relevant areas of the project. Report is technically sound, however may be lacking in appropriate technical detail. References are mostly appropriate and show some variation in type. Reference style correct (IEEE format).	Technical literature review shows good research abilities and covers most of the relevant areas of the project. A solid technical discussion has been held demonstrating an in-depth understanding of the topic. References used are all appropriate and cover many perspectives.	Technical literature review demonstrates exceptional research skills covering all relevant topics for the project. A comprehensive summary of considered techniques have been presented and fully discussed which have led the successful completion of the stage of the project. Students have obtained references from technically sound sources/ (IEEE format).
Logical and Convincing Presentation / Layout Diagrams and Photographs (10%)	Report contains a large number of spelling and grammatical errors. Figures are incorrect / difficult to interpret and no discussion has been held on the material presented.	Some spelling and grammatical errors present. Supporting figures are present however may not be 100% clear or limited discussion has been held on their meaning.	Spelling and grammar was of an acceptable level. Graphs and figures were clear but may have had unclear titles/captions. Figures have been linked back to the main text.	Spelling and grammar mostly correct. Graphs and figures are mostly clear and labelled. A discussion has been held on the figure and how it relates to the project.	Exceptional use of language. No spelling / grammatical errors. All figures are clear and well labelled. A thorough discussion has been held on their meaning and purpose.
Technical Merit (80%)	Functional block design and Algorithmic State Machine (ASM) diagram of system is not present / does not describe the relevant I/O. Logic / Design simulation is inadequate or not discussed.	Functional block design and Algorithmic State Machine (ASM) diagram of system is present however does not describe the relevant I/O or is lacking in detail. Logic / Design simulation has been performed,	Functional block design and Algorithmic State Machine (ASM) diagram of system is sufficient and describes the basic I/O and state requirements. Logic / Design simulation is suitable and important features noted.	Functional block design and Algorithmic State Machine (ASM) diagram of system is well constructed and includes appropriate states / resets. Simulation output demonstrates a fully operational design and	A comprehensive functional block and ASM diagram has been developed listing essential details. Logic / Design simulation is exceptional and comparisons have been clearly drawn between

	Deployed FPGA configuration was non-functional / results incorrect. (online students – simulation only). State Machine design details not present / not discussed. Design / schematic / HDL code not presented. Investigation method not discussed or described poorly. No analysis performed on results obtained. Unable to make links to theoretical concepts and / or irrelevant facts were used to try to explain results. The techniques employed do not demonstrate a sound technical understanding of the topic. Results have not been presented in a coherent fashion with limited discussion. Conclusions are not present or are technically flawed. Significant issues exist with the outcome of the project.	however has no discussion has been held. Partially functional FPGA configuration with poor verification and justification. (online students – simulation only). State Machine design details not discussed. Design / schematic / HDL code presented. Simulation was partially functional with questionable results. Superficial analysis of results presented. Results have not been linked back to existing theory presented. Can make basic links to theoretical concepts but lacks in-depth understanding. Significant gaps exist in the analysis of the results. Inappropriate conclusions have been drawn from the presented results. Outcomes are marginal and rely on existing work rather than demonstrating the students' ability. The techniques demonstrated highlight sufficient gaps in the students' knowledge. Conclusions are lacking detail.	Simulation output was operational however results were not explained. FPGA configuration is functional however limited discussion on design verification / justification (online students – simulation only). State Machine design details is presented and briefly discussed. Design / schematic / HDL code presented. A reasonable analysis has been made of results, but may be lacking some depth. Can make reasonable links to theoretical concepts to explain results. Investigation method undertaken is adequate, but student may not have considered more effective alternatives. Slight gaps exist in the students' knowledge. Conclusions are sufficiently detailed however no technical justification has been presented. Outcomes are acceptable however a more thorough analysis should have been performed to explain unexpected results.	important features discussed. FPGA configuration is functional and described in detail (online students – simulation only). Design / schematic / state machine / HDL code presented and appropriately justified. A good analysis of results presented. Investigation method undertaken was sound and appropriate for the project and student demonstrates they have a firm grasp of the theoretical aspects of the project. Outcomes are well documented and have been thoroughly explained. Unexpected results have been considered and an appropriate hypothesis formed. Conclusions and recommendations are justified, and a solid technical discussion is present.	theoretical and experimental results. Simulated design was fully operational and a complete comparison drawn between the theoretical and experimental results. FPGA configuration clearly meets all prescribed targets and verified with supporting documentation (online students – simulation only). Design / schematic / state machine / HDL code presented and fully explained. In-depth analysis of results presented. Advanced investigation method proposed that shows solid understanding of project requirements. Student demonstrates an advanced comprehension of the topic and has successfully completed the project. Conclusions made should be justified and well explained. Outcomes are exceptional.

EEET2162 / EEET2035 – Technical Demonstration Assessment Schedule

The EEET2162 / EEET2035 Project Technical Demonstration accounts for a total of 15% of the overall grade for EEET2162 and EEET2035. The content is to be marked out of 100 and then will be converted to an appropriate percentage. When marking the demonstration factors such as technical complexity, clarity of presentation, technical content, demonstrated technical skills and analysis of results should be considered.

	0 – 49 (NN)	50 – 59 (PA)	60 – 69 (CR)	70 – 79 (DI)	80 – 100 (HD)
Presentation - Style (10%)	Relies entirely on reading from notes and / or did not look at assessor. Unable to convey to assessor the nature of the project. Unable to answer questions posed by the assessor. Vague contribution to the discussion / relies on other group member(s).	Relies heavily on notes and / or makes little eye contact with assessor. Struggles to clearly explain the nature of the project to assessor. Struggles to answer questions posed by the assessor. Limited contribution to the discussion / relies on other group member(s).	Refers to notes at times but makes reasonable eye-contact with assessor. Nature of the project is conveyed reasonably well and is generally understandable. Responds to most questions but answers some incorrectly / lack of confidence. Discussion is vague and relies on prompts from group member(s).	Has little to no reliance on notes and makes good eye contact with audience. Shows an understanding of the nature of the project and conveys this well to assessor. Can answer all questions with reasonable confidence. Time is evenly split between group member(s) however limited indication on the individual contributions.	No reliance on notes and presents in an effective and innovative style. Clearly explains the nature of the project and generates enthusiasm for the topic with the assessor. Answers questions confidently and correctly. Time equally divided between both group member(s) with clear evidence of individual contributions.
Presentation / Demonstration - Technical Content (90%)	Minimal technical content presented. Inappropriate or insufficient details to support results, e.g. opinions stated instead of facts. No analysis of results or comparison against original aims. System has not been simulated to determine whether it is functionally operational. Investigation method not discussed or described poorly. Has not been able to solve technical problems at an appropriate level. Technical skill and complexity of solution are	Understands some of the topic but struggles to make connections with the results. Investigation method discussed but is flawed. No alternative methods described. The simulations developed do not demonstrate sufficient technical complexity or are lacking in analysis. Poor comparisons drawn between original specifications and the presented outcomes. Limited ability to solve technical problems or incorrect / inappropriate methods applied. Technical skill and complexity of the solution are	Superficial evaluation of results presented. Investigation method is generally sound, mention has been made to alternative methods but justifications may not have been given for why one method was used over another. Functional simulations have been performed to verify the sub-module design, however may not include all possible states / or contain minor errors or invalid assumptions. Comparison between expected outcomes and actual results lacks technical detail.	Sound analysis of results presented. Investigation method used has been described and justified. Some alternative methods have been considered and described. Functional simulations are verified against the system output. Advanced tools such as 'SignalTap' have been used to determine (and rectify errors) where appropriate. Comparison of actual results versus original specifications is sound. Technical detail is correct and informative. Has demonstrated an ability	In-depth analysis of results presented. Investigation method(s) well demonstrated and justified. Alternative methods have been thoroughly researched. Functional simulations are complete and verify complete system functionality. Demonstrated ability to resolve errors and implement appropriate solutions. Where appropriate output has been verified with tools such as 'SignalTap' or logic analysis. Excellent comparison

	inadequate. Presented outcomes are not satisfactory. System is not in working condition and / or system is not available for assessor to see.	marginal. Relies on existing products (IP Blocks) / solutions to demonstrate outcomes. Individual student has performed little technical work over the project. Minor parts of the system may be working but largely it does not work to specifications.	Technical problems have been addressed and solution is adequate although cumbersome. Fair progress has been demonstrated by the student. System achieves most of its specifications but may stop working intermittently or have an inconsistent output. System may need to be constantly reset to negate errors in the design.	to solve technical problems using standard accepted techniques. Good progress has been demonstrated by the student. A system has been developed that works to required specifications. System was well demonstrated to show its effectiveness and reliability.	between actual and expected results. Clearly demonstrated ability to solve technical problems using advanced methods. Exceptional progress has been demonstrated by the student. An innovative system / solution has been developed that works exactly as specifications require. Extra functionality may have also been included.