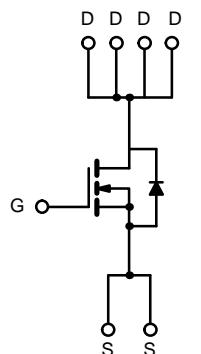
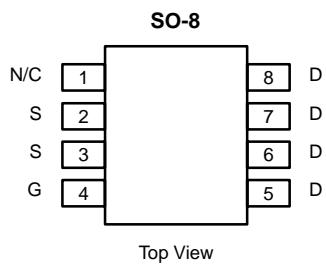


N-Channel Enhancement-Mode MOSFET

PRODUCT SUMMARY

V_{DS} (V)	R_{DSON} (Ω)	I_D (A)
200	1.0 @ V _{GS} = 10 V	± 1.0



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V _{DS}	200	V
Gate-Source Voltage	V _{GS}	± 20	
Continuous Drain Current (T _J = 150°C) ^A	I _D	± 1.0	A
		± 0.8	
Pulsed Drain Current	I _{DM}	± 10	
Avalanche Current	I _{AS}	5	
Single Avalanche Energy	E _{AS}	1.3	mJ
Continuous Source Current (Diode Conduction) ^A	I _S	1.0	A
Maximum Power Dissipation ^A	P _D	2.5	W
		1.6	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	-55 to 150	°C

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	LIMIT	UNIT
Maximum Junction-to-Ambient ^A	R _{thJA}	50	°C/W

Notes

A. Surface Mounted on FR4 Board, t ≤ 10 sec.

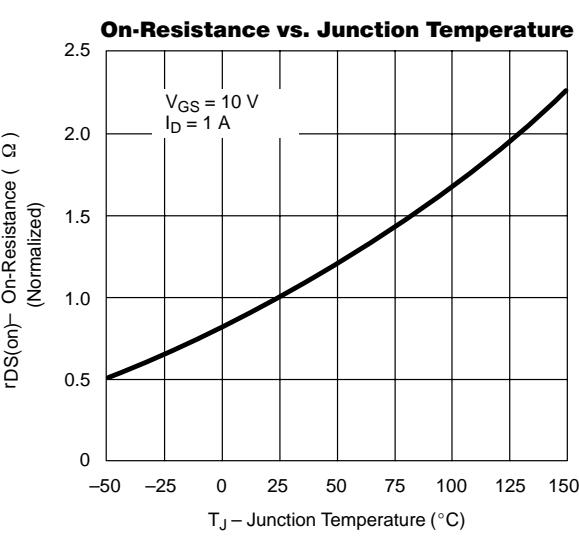
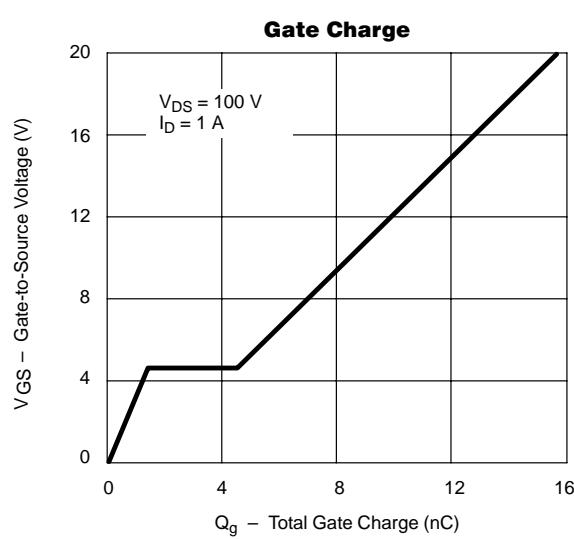
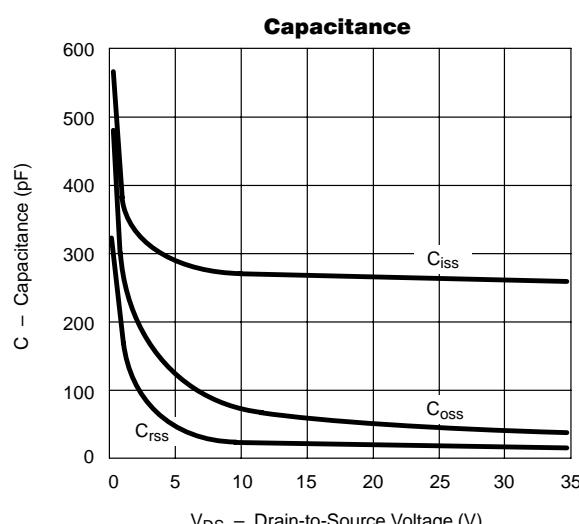
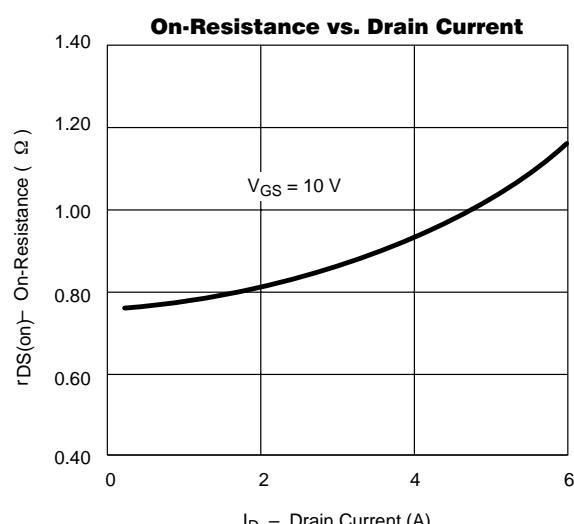
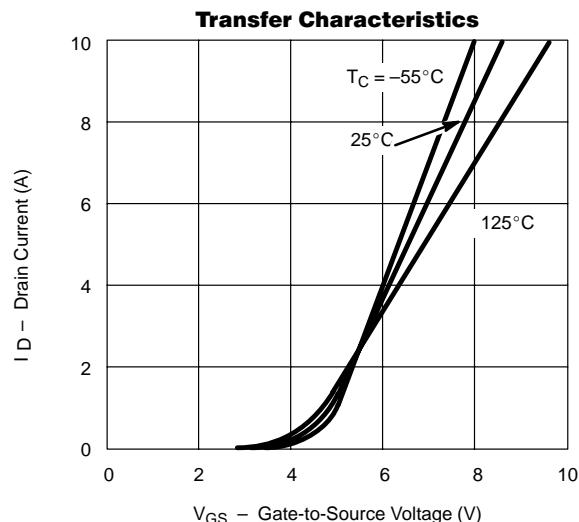
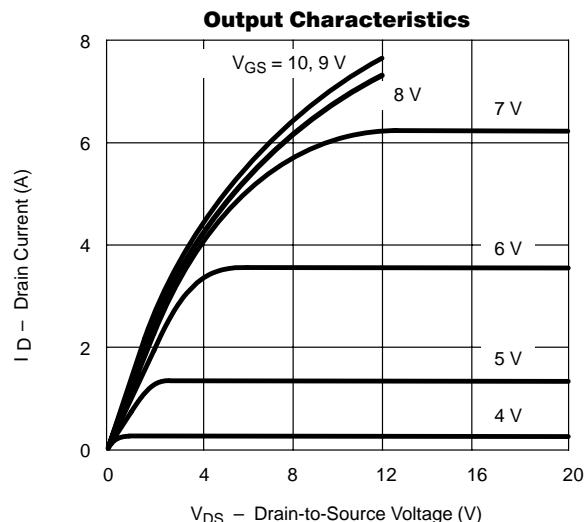
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SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

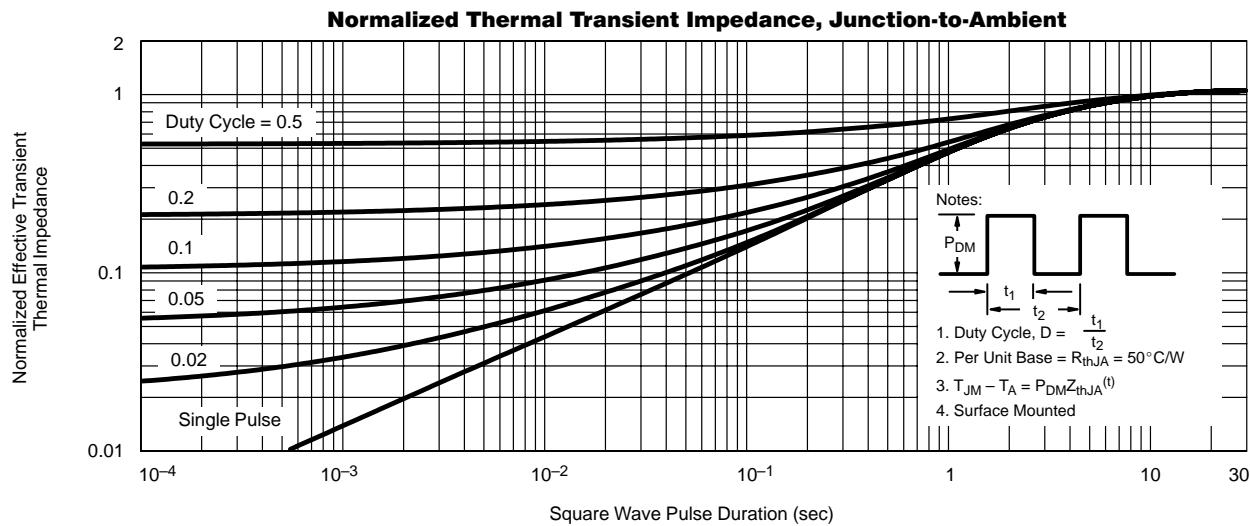
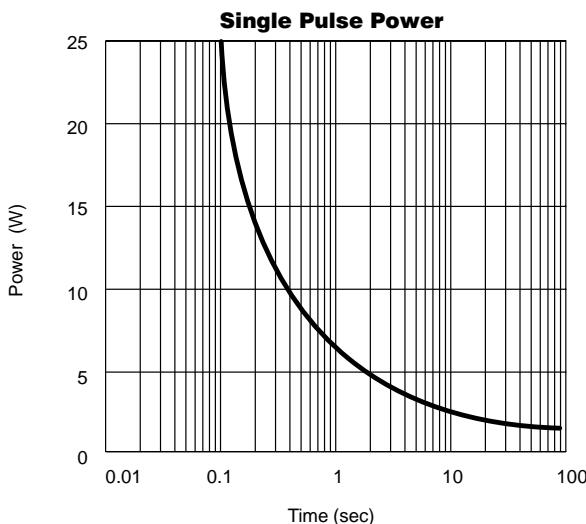
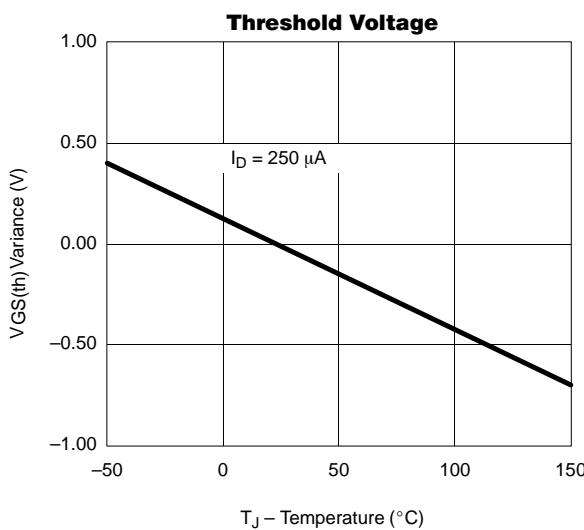
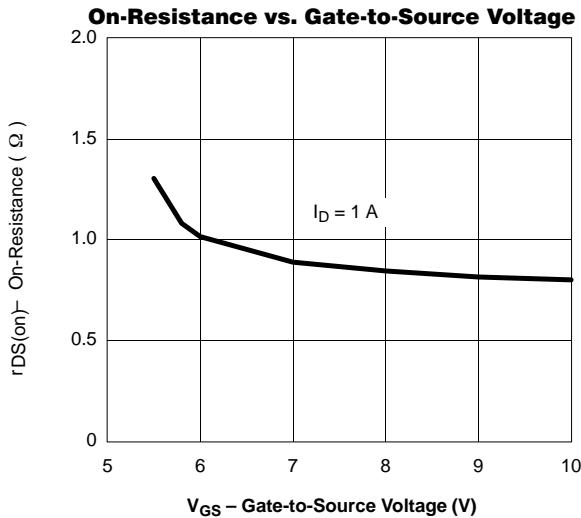
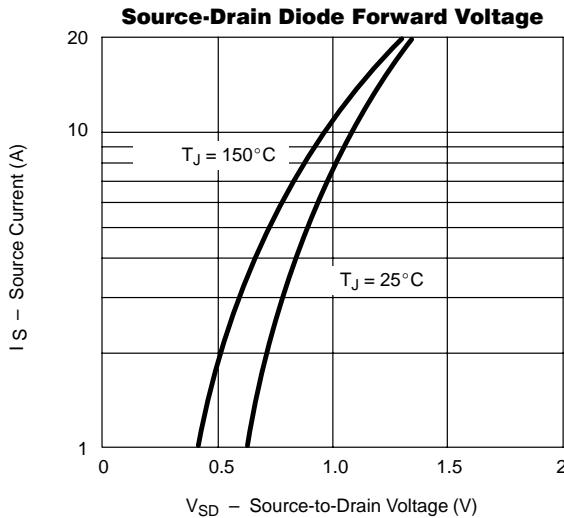
PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP ^A	MAX	UNIT
STATIC						
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$	2			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}$, $V_{GS} = \pm 20 \text{ V}$	2		± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 160 \text{ V}$, $V_{GS} = 0 \text{ V}$		2		μA
		$V_{DS} = 160 \text{ V}$, $V_{GS} = 0 \text{ V}$, $T_J = 55^\circ\text{C}$		25		
On-State Drain Current ^B	$I_{D(\text{on})}$	$V_{DS} \geq 10 \text{ V}$, $V_{GS} = 10 \text{ V}$	5.0			A
Drain-Source On-State Resistance ^B	$r_{DS(\text{on})}$	$V_{GS} = 10 \text{ V}$, $I_D = 1.0 \text{ A}$		0.8	1.0	Ω
Forward Transconductance ^B	g_{fs}	$V_{DS} = 15 \text{ V}$, $I_D = 1.0 \text{ A}$		1.5		S
Diode Forward Voltage ^B	V_{SD}	$I_S = 1.0 \text{ A}$, $V_{GS} = 0 \text{ V}$		0.7	1.2	V
DYNAMIC^A						
Total Gate Charge	Q_g	$V_{DS} = 100 \text{ V}$, $V_{GS} = 10 \text{ V}$, $I_D = 1.0 \text{ A}$		8.6	16	nC
Gate-Source Charge	Q_{gs}			1.5		
Gate-Drain Charge	Q_{gd}			3.2		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 100 \text{ V}$, $R_L = 100 \Omega$ $I_D \cong 1.0 \text{ A}$, $V_{GEN} = 10 \text{ V}$, $R_G = 6 \Omega$		7	14	ns
Rise Time	t_r			12	24	
Turn-Off Delay Time	$t_{d(off)}$			26	50	
Fall Time	t_f			15	30	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 1.0 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$		130		

Notes

- A. Guaranteed by design, not subject to production testing.
 B. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS (25°C UNLESS OTHERWISE NOTED)


TYPICAL CHARACTERISTICS (25°C UNLESS OTHERWISE NOTED)





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