马宇哲

高级研究科学家 ⋄ 华为香港研究所

博士 ⋄ 计算机科学与工程 ⋄ 香港中文大学

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研究方向

- 电路设计自动化的建模和优化
- 超大规模集成电路敏捷设计方法学
- 高能效深度学习及其应用，硬件友好型机器学习范式及算法

教育经历

香港中文大学 2016 年 8 月– 2020 年 7 月

博士学位　计算机科学与工程

导师: Bei Yu

学位论文: “Methodologies for Hardware Design Automation and Hardware-friendly Learning”

中山大学 2011 年 9 月 – 2016 年 7 月

学士学位　微电子学

(学分绩 92/100, 排名 1/64)

工作经历

华为香港研究所 (Huawei Hong Kong Research Center) 2020 年 9 月 – 现在

高级研究科学家

腾讯优图实验室 (Tencent YouTu Lab) 2019 年 7 月 – 2020 年 2 月

研究实习生, X-lab

课题: Model Compression and Domain Adaptation

英伟达研究院 (NVIDIA Research, USA) 2018 年 7 月 – 2018 年 11 月

研究实习生, ASIC &VLSI 研究组

课题: Testability Analysis with Graph Neural Networks

铿腾半导体 (Cadence, USA) 2017 年 5 月 – 2017 年 9 月

研究实习生, 数字设计后端研究组

课题: Deep Learning/Machine Learning in Placement

香港中文大学 (The Chinese University of Hong Kong) 2016 年 3 月 – 2016 年 5 月

研究助理, 计算机科学与工程系

课题: Standard Cell Synthesis

奖项及荣誉

最佳论文奖	ASPDAC	2021
最佳研究奖	ASPDAC SRF, ACM SIGDA	2020

最佳学生论文奖	ICTAI	2019
最佳论文奖提名	ASPDAC	2019
季军	ISPD Contest	2020
国家励志奖学金	中山大学	2013, 2014, 2015
一等学术奖学金	中山大学	2013, 2014, 2015
校级优秀学生	中山大学	2013, 2014, 2015

出版物

期刊论文

[J15] Guojin Chen, Wanli Chen, Qi Sun, **Yuzhe Ma**, Haoyu Yang, Bei Yu, "DAMO: Deep Agile Mask Optimization for Full Chip Scale", accepted by IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**).

[J14] Hao Geng, **Yuzhe Ma**, Qi Xu, Jin Miao, Subhendu Roy, Bei Yu, "High-Speed Adder Design Space Exploration via Graph Neural Processes", accepted by IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**).

[J13] Bentian Jiang, Lixin Liu, **Yuzhe Ma**, Bei Yu, Evangeline F.Y. Young, "Neural-ILT 2.0: Migrating ILT to Domain-specific and Multi-task-enabled Neural Network", accepted by IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**).

[J12] Wei Zhong, Shuxiang Hu, **Yuzhe Ma**, Haoyu Yang, Xiuyuan Ma, Bei Yu, "Deep Learning-Driven Simultaneous Layout Decomposition and Mask Optimization", accepted by IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**).

[J11] Wei Li, **Yuzhe Ma**, Qi Sun, Lu Zhang, Yibo Lin, Iris Hui-Ru Jiang, Bei Yu, David Z. Pan, "OpenMPL: An Open Source Layout Decomposer", accepted by IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**).

[J10] Guyue Huang, Jingbo Hu, Yifan He, Jialong Liu, Mingyuan Ma, Zhaoyang Shen, Juejian Wu, Yuanfan Xu, Hengrui Zhang, Kai Zhong, Xuefei Ning, **Yuzhe Ma**, Haoyu Yang, Bei Yu, Huazhong Yang, Yu Wang, "Machine Learning for Electronic Design Automation: A Survey", accepted by ACM Transactions on Design Automation of Electronic Systems (**TODAES**).

[J9] Haoyu Yang, Wei Zhong, **Yuzhe Ma**, Hao Geng, Ran Chen, Wanli Chen, Bei Yu, "VLSI Mask Optimization: From Shallow To Deep Learning", accepted by Integration, the VLSI Journal.

[J8] Kang Liu, Haoyu Yang, **Yuzhe Ma**, Benjamin Tan, Bei Yu, Evangeline F. Y. Young, Ramesh Karri, Siddharth Garg, "Are Adversarial Perturbations a Showstopper for ML-Based CAD? A Case Study on CNN-Based Lithographic Hotspot Detection", ACM Transactions on Design Automation of Electronic Systems (**TODAES**), vol. 25, no. 5, 2020.

[J7] **Yuzhe Ma**, Wei Zhong, Shuxiang Hu, Jhih-Rong Gao, Jian Kuang, Jin Miao, Bei Yu, "A Unified Framework for Simultaneous Layout Decomposition and Mask Optimization", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 39, no. 12, pp. 5069–5082, 2020.

[J6] Hao Geng, Wei Zhong, Haoyu Yang, **Yuzhe Ma**, Joydeep Mitra, Bei Yu, "SRAF Insertion via Supervised Dictionary Learning", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 39, no. 10, pp. 2849–2859, 2020.

[J5] Haoyu Yang, Shuhe Li, Zihao Deng, **Yuzhe Ma**, Bei Yu, and Evangeline F. Y. Young, "GAN-OPC: Mask Optimization with Lithography-guided Generative Adversarial Nets", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 39, no. 10, pp. 2822–2834, 2020.

[J4] **Yuzhe Ma**, Subhendu Roy, Jin Miao, Jiamin Chen, and Bei Yu, "Cross-layer Optimization for High Speed Adders: A Pareto Driven Machine Learning Approach", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 38, no. 12, pp. 2298–2311, 2019

[J3] Qianru Zhang, Meng Zhang, Tinghuan Chen, Zhifei Sun, **Yuzhe Ma**, and Bei Yu, "Recent Advances in Convolutional Neural Network Acceleration", Neurocomputing, vol. 323, pp. 37-51, Jan., 2019.

[J2] Haoyu Yang, Jing Su, Yi Zou, **Yuzhe Ma**, Bei Yu, and Evangeline F. Y. Young, "Layout Hotspot Detection with Feature Tensor Generation and Deep Biased Learning", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 38, no. 6, pp. 1175–1187, 2019.

[J1] Jin Miao, Meng Li, Subhendu Roy, **Yuzhe Ma**, and Bei Yu, "SD-PUF: Spliced Digital Physical Unclonable Function", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), vol. 37, no. 5, pp. 927–940, 2018.

会议论文

[C24] Chen Bai, Qi Sun, Jianwang Zhai, **Yuzhe Ma**, Bei Yu, Martin D.F. Wong, "BOOM-Explorer: RISC-V BOOM Microarchitecture Design Space Exploration Framework", IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**), Nov. 01-04, 2021.

[C23] Guojin Chen, Ziyang Yu, Hongduo Liu, **Yuzhe Ma**, Bei Yu, "DevelSet: Deep Neural Level Set for Instant Mask optimization", IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**), Nov. 01-04, 2021.

[C22] Ziyang Yu, Guojin Chen, **Yuzhe Ma**, Bei Yu, "A GPU-enabled Level-Set Method for Mask Optimization", IEEE/ACM Proceedings Design, Automation and Test in Europe (**DATE**), Feb. 01-05, 2021.

[C21] Zhuolun He, Peiyu Liao, Siting Liu, **Yuzhe Ma**, Bei Yu, "Physical Synthesis for Advanced Neural Network Processors", IEEE/ACM Asian and South Pacific Design Automation Conference (**ASPDAC**), Jan. 18-21, 2021. (Invited Paper)

[C20] Wei Li, Yuxiao Qu, Gengjie Chen, **Yuzhe Ma**, Bei Yu, "TreeNet: Deep Point Cloud Embedding for Routing Tree Construction", IEEE/ACM Asian and South Pacific Design Automation Conference (**ASPDAC**), Jan. 18-21, 2021. **(Best Paper Award)**

[C19] Zhuolun He, Lu Zhang, Peiyu Liao, **Yuzhe Ma**, Bei Yu, "Reinforcement Learning Driven Physical Synthesis", IEEE International Conference on Solid -State and Integrated Circuit Technology (**ICSICT**), Nov. 3-6, 2020. (Invited Paper)

[C18] Guojin Chen, Wanli Chen, **Yuzhe Ma**, Haoyu Yang, Bei Yu, "DAMO: Deep Agile Mask Optimization for Full Chip Scale", IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**), Nov.

2-5, 2020.

[C17] Bentian Jiang, Lixin Liu, **Yuzhe Ma**, Hang Zhang, Evangeline F. Y. Young, Bei Yu, "Neural-ILT: Migrating ILT to Nerual Networks for Mask Printability and Complexity Co-optimizaton", IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**), Nov. 2-5, 2020.

[C16] Zhuolun He, **Yuzhe Ma**, Lu Zhang, Peiyu Liao, Ngai Wong, Bei Yu, Martin D. F. Wong, "Learn to Floorplan through Acquisition of Effective Local Search Heuristics", IEEE International Conference on Computer Design (**ICCD**), Oct. 18–21, 2020.

[C15] Wei Li, Jialu Xia, **Yuzhe Ma**, Jialu Li, Yibo Lin, Bei Yu, "Adaptive Layout Decomposition with Graph Embedding Neural Networks", ACM/IEEE Design Automation Conference (**DAC**), San Francisco, CA, July 19–23, 2020.

[C14] Wei Zhong, Shuxiang Hu, **Yuzhe Ma**, Haoyu Yang, Xiuyuan Ma, Bei Yu, "Deep Learning-Driven Simultaneous Layout Decomposition and Mask Optimization", ACM/IEEE Design Automation Conference (**DAC**), San Francisco, CA, July 19–23, 2020.

[C13] **Yuzhe Ma**, Zhuolun He, Wei Li, Tinghuan Chen, Lu Zhang, Bei Yu, "Understanding Graphs in EDA: From Shallow to Deep Learning", ACM International Symposium on Physical Design (**ISPD**), Taipei, Mar. 25–Apr. 01, 2020. (Invited Paper)

[C12] Haoyu Yang, Wei Zhong, **Yuzhe Ma**, Hao Geng, Ran Chen, Wanli Chen, Bei Yu, "VLSI Mask Optimization: From Shallow To Deep Learning", IEEE/ACM Asian and South Pacific Design Automation Conference (**ASPDAC**), Beijing, Jan. 13–16, 2020. (Invited Paper)

[C11] Zhonghua Zhou, Ziran Zhu, Jianli Chen, **Yuzhe Ma**, Bei Yu, Tsung-Yi Ho, Guy Lemieux, Andre Ivano, "Congestion-aware Global Routing using Deep Convolutional Generative Adversarial Networks", ACM/IEEE Workshop on Machine Learning for CAD (**MLCAD**), Alberta, Canada, Sep. 3–4, 2019.

[C10] **Yuzhe Ma**, Ziyang Yu, Bei Yu, "CAD Tool Design Space Exploration via Bayesian Optimization", ACM/IEEE Workshop on Machine Learning for CAD (**MLCAD**), Alberta, Canada, Sep. 3–4, 2019.

[C9] **Yuzhe Ma**, Ran Chen, Wei Li, Fanhua Shang, Wenjian Yu, Minsik Cho, Bei Yu, "A Unified Approximation Framework for Compressing and Accelerating Deep Neural Networks", IEEE International Conference on Tools with Artificial Intelligence (**ICTAI**), Portland, OR, Nov. 4–6, 2019. **(Best Student Paper Award)**

[C8] Wei Li, **Yuzhe Ma**, Qi Sun, Yibo Lin, Iris Hui-Ru Jiang, Bei Yu, David Z. Pan, "OpenMPL: An Open Source Layout Decomposer", IEEE International Conference on ASIC (**ASICON**), Chongqing, China, Oct. 29–Nov. 1, 2019.

[C7] **Yuzhe Ma**, Haoxing Ren, Brucek Khailany, Harbinder Sikka, Karthikeyan Natarajan, and Bei Yu, "High Performance Graph Convolutional Networks with Applications in Testability Analysis", ACM/IEEE Design Automation Conference (**DAC**), Las Vegas, NV, June 2–6, 2019.

[C6] Hao Geng, Haoyu Yang, **Yuzhe Ma**, Joydeep Mitra, and Bei Yu, "SRAF Insertion via Supervised Dictionary Learning", IEEE/ACM Asian and South Pacific Design Automation Conference (**ASPDAC**), Tokyo, Jan. 21–24, 2019. **(Best Paper Award Nomination)**

[C5] Haoyu Yang, Shuhe Li, **Yuzhe Ma**, Bei Yu, and Evangeline F. Y. Young, "GAN-OPC: Mask Optimization with Lithography-guided Generative Adversarial Nets", ACM/IEEE Design Automation Conference (**DAC**), San Francisco, CA, June 24–28, 2018.

[C4] **Yuzhe Ma**, Jhih-Rong Gao, Jian Kuang, Jin Miao, and Bei Yu, "A Unified Framework for Simultaneous Layout Decomposition and Mask Optimization", IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**), Irvine, CA, Nov. 13–16, 2017.

[C3] Chak-Wa Pui, Gengjie Chen, **Yuzhe Ma**, Evangeline F. Y. Young, and Bei Yu, "Clock-Aware UltraScale FPGA Placement with Machine Learning Routability Prediction", IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**), Irvine, CA, Nov. 13–16, 2017.

[C2] **Yuzhe Ma**, Xuan Zeng, and Bei Yu, "Methodologies for Layout Decomposition and Mask Optimization: A Systematic Review", IFIP/IEEE International Conference on Very Large Scale Integration (**VLSI-SoC**), Abu Dhabi, UAE, Oct. 23–25, 2017.

[C1] Subhendu Roy, **Yuzhe Ma**, Jin Miao, and Bei Yu, "A Learning Bridge from Architectural Synthesis to Physical Design for Exploring Power Efficient High-Performance Adders", IEEE/ACM International Symposium on Low Power Electronics and Design (**ISLPED**), Taipei, Taiwan, July 24–26, 2017.

专利

[P1] **Yuzhe Ma**, Haoxing Ren, Brucek Khailany, Harbinder Sikka, Lijuan Luo, Karthikeyan Natarajan, "Deep Learning Testability Analysis with Graph Convolutional Networks", US Patent 10657306, May, 2020.

授课经历

2019 年春	Energy Efficient Computing	助教
2018 年春	Practical Computational Geometry Algorithms	助教
2017 年春	Approximation Algorithms	助教
2016 & 2017 年秋	Embedded System Development and Applications	助教

项目

- 参与, 第一贡献人, "芯片可制造性统一优化框架", 香港研究资助局优配项目，RGC 24209017, HK$725,500, 07/2017–06/2020.
- 参与, 第一贡献人, "AI 芯片物理设计", 香港中文大学–华为校企合作研究项目，Reference# TH1914457, 12/2019–08/2020, HK$1,400,000.
- 参与, "模拟芯片可靠性检测框架", 香港中文大学–华为校企合作研究项目，Reference# TH1914161, 10/2019–07/2020, HK$650,000.
- 参与, "集成电路芯片版图验证与优化", 香港中文大学–Cadence 校企合作研究项目, 06/2019–05/2021, HK$156,580.

学术服务

技术程序委员会

- Workshop on Synthesis And System Integration of Mixed Information Technologies (SASIMI), 2021.

期刊邀请审稿人

- ACM Transaction on Design Automation of Electronic Systems (TODAES)
- IEEE Transaction on Computer-Aided Design of Integrated Circuits and Systems (TCAD)
- VLSI Design
- IET Cyber-Physical Systems: Theory & Applications

会议邀请/外部审稿人

- IEEE Conference on Computer Vision and Pattern Recognition (CVPR), 2020, 2021
- ACM/IEEE Design Automation Conference (DAC), 2018, 2019, 2020
- AAAI Conference on Artificial Intellignece (AAAI), 2021
- ACM International Symposium on Physical Design (ISPD), 2018, 2019
- IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC), 2018