

# YUZHE MA

Ph.D. Student ◊ Department of Computer Science & Engineering  
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## RESEARCH INTERESTS

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- Machine learning with applications in VLSI CAD
- Physical design & design for manufacturability in VLSI CAD
- Hardware-friendly learning

## EDUCATION

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<b>The Chinese University of Hong Kong, NT, Hong Kong SAR</b> Ph.D. student, Department of Computer Science & Engineering. Advisor: Prof. Bei Yu	Aug. 2016 – Present
<b>Sun Yat-sen University, Guangzhou, P.R. China</b> B.Eng., Microelectronics. (GPA 92/100, RANK 1/64) Dissertation: “Methodologies for Standard Cell Layout Migration”	Sep. 2011 – Jul. 2016

## EXPERIENCE

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<b>Tencent YouTu Lab, Shenzhen, China</b> Research Intern, X-lab Topic: Model Compression and Domain Adaptation	July 2019 – Feb. 2020
<b>NVIDIA Research, TX, USA</b> Research Intern, ASIC and VLSI research group Topic: Testability Analysis with Graph Neural Networks	July 2018 – Nov. 2018
<b>Cadence Design Systems, Inc., CA, USA</b> Research Intern, Digital Design and Signoff Group Topic: Deep Learning/Machine Learning in Placement	May 2017 – Sep. 2017
<b>The Chinese University of Hong Kong, NT, Hong Kong SAR</b> Research Assistant, Department of Computer Science & Engineering Topic: Standard Cell Synthesis	Mar. 2016 – May 2016

## PUBLICATIONS

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### Journal Papers

- [J7] **Yuzhe Ma**, Wei Zhong, Shuxiang Hu, Jhih-Rong Gao, Jian Kuang, Jin Miao, Bei Yu, “A Unified Framework for Simultaneous Layout Decomposition and Mask Optimization”, accepted by IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**).
- [J6] Hao Geng, Wei Zhong, Haoyu Yang, **Yuzhe Ma**, Joydeep Mitra, Bei Yu, “SRAF Insertion via Supervised Dictionary Learning”, accepted by IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**).
- [J5] Haoyu Yang, Shuhe Li, Zihao Deng, **Yuzhe Ma**, Bei Yu, and Evangeline F. Y. Young, “GAN-OPC: Mask Optimization with Lithography-guided Generative Adversarial Nets”, accepted by IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**).
- [J4] **Yuzhe Ma**, Subhendu Roy, Jin Miao, Jiamin Chen, and Bei Yu, “Cross-layer Optimization for High Speed Adders: A Pareto Driven Machine Learning Approach”, accepted by IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**).

- [J3] Qianru Zhang, Meng Zhang, Tinghuan Chen, Zhifei Sun, **Yuzhe Ma**, and Bei Yu, “Recent Advances in Convolutional Neural Network Acceleration”, *Neurocomputing*, vol. 323, pp. 37-51, Jan., 2019.
- [J2] Haoyu Yang, Jing Su, Yi Zou, **Yuzhe Ma**, Bei Yu, and Evangeline F. Y. Young, “Layout Hotspot Detection with Feature Tensor Generation and Deep Biased Learning”, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 38, no. 6, pp. 1175–1187, 2019.
- [J1] Jin Miao, Meng Li, Subhendu Roy, **Yuzhe Ma**, and Bei Yu, “SD-PUF: Spliced Digital Physical Unclonable Function”, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 37, no. 5, pp. 927–940, 2018.

## Conference Papers

- [C13] Wei Li, Jialu Xia, **Yuzhe Ma**, Jialu Li, Yibo Lin, Bei Yu, “Adaptive Layout Decomposition with Graph Embedding Neural Networks”, *ACM/IEEE Design Automation Conference (DAC)*, San Francisco, CA, July 19–23, 2020.
- [C12] Wei Zhong, Shuxiang Hu, **Yuzhe Ma**, Haoyu Yang, Xiuyuan Ma, Bei Yu, “Deep Learning-Driven Simultaneous Layout Decomposition and Mask Optimization”, *ACM/IEEE Design Automation Conference (DAC)*, San Francisco, CA, July 19–23, 2020.
- [C11] **Yuzhe Ma**, Zhuolun He, Wei Li, Tinghuan Chen, Lu Zhang, Bei Yu, “Understanding Graphs in EDA: From Shallow to Deep Learning”, *ACM International Symposium on Physical Design (ISPD)*, Taipei, Mar. 25–Apr. 01, 2020. (Invited Paper)
- [C10] Haoyu Yang, Wei Zhong, **Yuzhe Ma**, Hao Geng, Ran Chen, Wanli Chen, Bei Yu, “VLSI Mask Optimization: From Shallow To Deep Learning”, *IEEE/ACM Asian and South Pacific Design Automation Conference (ASPDAC)*, Beijing, Jan. 13–16, 2020. (Invited Paper)
- [C9] **Yuzhe Ma**, Ran Chen, Wei Li, Fanhua Shang, Wenjian Yu, Minsik Cho, Bei Yu, “A Unified Approximation Framework for Compressing and Accelerating Deep Neural Networks”, *IEEE International Conference on Tools with Artificial Intelligence (ICTAI)*, Portland, OR, Nov. 4–6, 2019. (**Best Student Paper Award**)
- [C8] Wei Li, **Yuzhe Ma**, Qi Sun, Yibo Lin, Iris Hui-Ru Jiang, Bei Yu, David Z. Pan, “OpenMPL: An Open Source Layout Decomposer”, *IEEE International Conference on ASIC (ASICON)*, Chongqing, China, Oct. 29–Nov. 1, 2019.
- [C7] **Yuzhe Ma**, Haoxing Ren, Brucek Khailany, Harbinder Sikka, Karthikeyan Natarajan, and Bei Yu, “High Performance Graph Convolutional Networks with Applications in Testability Analysis”, *ACM/IEEE Design Automation Conference (DAC)*, Las Vegas, NV, June 2–6, 2019.
- [C6] Hao Geng, Haoyu Yang, **Yuzhe Ma**, Joydeep Mitra, and Bei Yu, “SRAF Insertion via Supervised Dictionary Learning”, *IEEE/ACM Asian and South Pacific Design Automation Conference (ASPDAC)*, Tokyo, Jan. 21–24, 2019. (**Best Paper Award Nomination**)
- [C5] Haoyu Yang, Shuhe Li, **Yuzhe Ma**, Bei Yu, and Evangeline F. Y. Young, “GAN-OPC: Mask Optimization with Lithography-guided Generative Adversarial Nets”, *ACM/IEEE Design Automation Conference (DAC)*, San Francisco, CA, June 24–28, 2018.
- [C4] **Yuzhe Ma**, Jhih-Rong Gao, Jian Kuang, Jin Miao, and Bei Yu, “A Unified Framework for Simultaneous Layout Decomposition and Mask Optimization”, *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Irvine, CA, Nov. 13–16, 2017.
- [C3] Chak-Wa Pui, Gengjie Chen, **Yuzhe Ma**, Evangeline F. Y. Young, and Bei Yu, “Clock-Aware UltraScale FPGA Placement with Machine Learning Routability Prediction”, *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Irvine, CA, Nov. 13–16, 2017.
- [C2] **Yuzhe Ma**, Xuan Zeng, and Bei Yu, “Methodologies for Layout Decomposition and Mask Optimization: A Systematic Review”, *IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC)*, Abu Dhabi, UAE, Oct. 23–25, 2017.
- [C1] Subhendu Roy, **Yuzhe Ma**, Jin Miao, and Bei Yu, “A Learning Bridge from Architectural Synthesis to Physical Design for Exploring Power Efficient High-Performance Adders”, *IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED)*, Taipei, Taiwan, July 24–26, 2017.

## Patents

[P1] **Yuzhe Ma**, Haoxing Ren, Brucek Khailany, Harbinder Sikka, Lijuan Luo, Karthikeyan Natarajan, “Deep Learning Testability Analysis with Graph Convolutional Networks”, US Patent 10657306, May, 2020.

## SELECTED AWARDS AND HONORS

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Best Poster (Research) Award	ASPDAC SRF, ACM SIGDA	2020
Third Place Award	ISPD Contest	2020
Best Student Paper Award	ICTAI	2019
Best Paper Award Nomination	ASPDAC	2019
Full Postgraduate Studentship	The Chinese University of Hong Kong	2016 –
National Encouragement Scholarship	Sun Yat-sen University	2013, 2014, 2015
First Class Outstanding Academic Scholarship	Sun Yat-sen University	2013, 2014, 2015
Merit Student of Sun Yat-sen University	Sun Yat-sen University	2013, 2014, 2015

## GRADUATE-LEVEL COURSES

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ENGG5501: Foundations of Optimization  
ENGG5103: Data Mining  
SEEM5350: Numerical Optimization  
CSCI5580: Online Algorithms for Machine Learning and Optimization  
CENG5270: CAD for Physical Design of VLSI Circuits

## TECHNICAL SKILLS

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<b>Languages</b>	C/C++, Python, MATLAB, $\text{\LaTeX}$
<b>Operating Systems</b>	Linux/UNIX, MacOS
<b>Toolkits</b>	PyTorch, Caffe