

YUZHE MA

Senior Research Scientist ◊ Huawei Hong Kong Research Center
Ph.D. ◊ The Chinese University of Hong Kong
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RESEARCH INTERESTS

- Machine learning with applications in VLSI CAD
- Hardware-friendly learning algorithm
- Agile VLSI design methodology

EDUCATION

The Chinese University of Hong Kong, NT, Hong Kong SAR Aug. 2016 – Jul. 2020
Ph.D. Computer Science & Engineering.
Advisor: Prof. Bei Yu
Dissertation: “Methodologies for Hardware Design Automation and Hardware-friendly Learning”

Sun Yat-sen University, Guangzhou, P.R. China Sep. 2011 – Jul. 2016
B.Eng. Microelectronics
(GPA 92/100, RANK 1/64)

EXPERIENCE

Huawei Hong Kong Research Center, Hong Kong SAR Sep. 2020 – Present
Senior Research Scientist

Tencent YouTu Lab, Shenzhen, China Jul. 2019 – Feb. 2020
Research Intern, X-lab
Topic: Model Compression and Domain Adaptation

NVIDIA Research, TX, USA Jul. 2018 – Nov. 2018
Research Intern, ASIC and VLSI research group
Topic: Testability Analysis with Graph Neural Networks

Cadence Design Systems, Inc., CA, USA May 2017 – Sep. 2017
Research Intern, Digital Design and Signoff Group
Topic: Deep Learning/Machine Learning in Placement

The Chinese University of Hong Kong, NT, Hong Kong SAR Mar. 2016 – May 2016
Research Assistant, Department of Computer Science & Engineering
Topic: Standard Cell Synthesis

PUBLICATIONS

Journal Papers

- [J8] Kang Liu, Haoyu Yang, **Yuzhe Ma**, Benjamin Tan, Bei Yu, Evangeline F. Y. Young, Ramesh Karri, Siddharth Garg, “Are Adversarial Perturbations a Showstopper for ML-Based CAD? A Case Study on CNN-Based Lithographic Hotspot Detection”, accepted by ACM Transactions on Design Automation of Electronic Systems (**TODAES**).
- [J7] **Yuzhe Ma**, Wei Zhong, Shuxiang Hu, Jhih-Rong Gao, Jian Kuang, Jin Miao, Bei Yu, “A Unified Framework for Simultaneous Layout Decomposition and Mask Optimization”, accepted by IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**).
- [J6] Hao Geng, Wei Zhong, Haoyu Yang, **Yuzhe Ma**, Joydeep Mitra, Bei Yu, “SRAF Insertion via Supervised Dictionary Learning”, accepted by IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**).

- [J5] Haoyu Yang, Shuhe Li, Zihao Deng, **Yuzhe Ma**, Bei Yu, and Evangeline F. Y. Young, “GAN-OPC: Mask Optimization with Lithography-guided Generative Adversarial Nets”, accepted by IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**).
- [J4] **Yuzhe Ma**, Subhendu Roy, Jin Miao, Jiamin Chen, and Bei Yu, “Cross-layer Optimization for High Speed Adders: A Pareto Driven Machine Learning Approach”, accepted by IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**).
- [J3] Qianru Zhang, Meng Zhang, Tinghuan Chen, Zhifei Sun, **Yuzhe Ma**, and Bei Yu, “Recent Advances in Convolutional Neural Network Acceleration”, *Neurocomputing*, vol. 323, pp. 37-51, Jan., 2019.
- [J2] Haoyu Yang, Jing Su, Yi Zou, **Yuzhe Ma**, Bei Yu, and Evangeline F. Y. Young, “Layout Hotspot Detection with Feature Tensor Generation and Deep Biased Learning”, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 38, no. 6, pp. 1175–1187, 2019.
- [J1] Jin Miao, Meng Li, Subhendu Roy, **Yuzhe Ma**, and Bei Yu, “SD-PUF: Spliced Digital Physical Unclonable Function”, *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 37, no. 5, pp. 927–940, 2018.

Conference Papers

- [C21] Zhuolun He, Peiyu Liao, Siting Liu, **Yuzhe Ma**, Bei Yu, “Physical Synthesis for Advanced Neural Network Processors”, *IEEE/ACM Asian and South Pacific Design Automation Conference (ASPDAC)*, Jan. 18-21, 2021. (Invited Paper)
- [C20] Wei Li, Yuxiao Qu, Gengjie Chen, **Yuzhe Ma**, Bei Yu, “TreeNet: Deep Point Cloud Embedding for Routing Tree Construction”, *IEEE/ACM Asian and South Pacific Design Automation Conference (ASPDAC)*, Jan. 18-21, 2021.
- [C19] Zhuolun He, Lu Zhang, Peiyu Liao, **Yuzhe Ma**, Bei Yu, “Reinforcement Learning Driven Physical Synthesis”, *IEEE International Conference on Solid -State and Integrated Circuit Technology (ICSICT)*, Nov. 3-6, 2020. (Invited Paper)
- [C18] Guojin Chen, Wanli Chen, **Yuzhe Ma**, Haoyu Yang, Bei Yu, “DAMO: Deep Agile Mask Optimization for Full Chip Scale”, *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Nov. 2-5, 2020.
- [C17] Bentian Jiang, Lixin Liu, **Yuzhe Ma**, Hang Zhang, Evangeline F. Y. Young, Bei Yu, “Neural-ILT: Migrating ILT to Nerual Networks for Mask Printability and Complexity Co-optimizaton”, *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Nov. 2-5, 2020.
- [C16] Zhuolun He, **Yuzhe Ma**, Lu Zhang, Peiyu Liao, Ngai Wong, Bei Yu, Martin D. F. Wong, “Learn to Floorplan through Acquisition of Effective Local Search Heuristics”, *IEEE International Conference on Computer Design (ICCD)*, Oct. 18–21, 2020.
- [C15] Wei Li, Jialu Xia, **Yuzhe Ma**, Jialu Li, Yibo Lin, Bei Yu, “Adaptive Layout Decomposition with Graph Embedding Neural Networks”, *ACM/IEEE Design Automation Conference (DAC)*, San Francisco, CA, July 19–23, 2020.
- [C14] Wei Zhong, Shuxiang Hu, **Yuzhe Ma**, Haoyu Yang, Xiuyuan Ma, Bei Yu, “Deep Learning-Driven Simultaneous Layout Decomposition and Mask Optimization”, *ACM/IEEE Design Automation Conference (DAC)*, San Francisco, CA, July 19–23, 2020.
- [C13] **Yuzhe Ma**, Zhuolun He, Wei Li, Tinghuan Chen, Lu Zhang, Bei Yu, “Understanding Graphs in EDA: From Shallow to Deep Learning”, *ACM International Symposium on Physical Design (ISPD)*, Taipei, Mar. 25–Apr. 01, 2020. (Invited Paper)
- [C12] Haoyu Yang, Wei Zhong, **Yuzhe Ma**, Hao Geng, Ran Chen, Wanli Chen, Bei Yu, “VLSI Mask Optimization: From Shallow To Deep Learning”, *IEEE/ACM Asian and South Pacific Design Automation Conference (ASPDAC)*, Beijing, Jan. 13–16, 2020. (Invited Paper)
- [C11] Zhonghua Zhou, Ziran Zhu, Jianli Chen, **Yuzhe Ma**, Bei Yu, Tsung-Yi Ho, Guy Lemieux, Andre Ivano, “Congestion-aware Global Routing using Deep Convolutional Generative Adversarial Networks”, *ACM/IEEE Workshop on Machine Learning for CAD (MLCAD)*, Alberta, Canada, Sep. 3–4, 2019.

- [C10] **Yuzhe Ma**, Ziyang Yu, Bei Yu, “CAD Tool Design Space Exploration via Bayesian Optimization”, ACM/IEEE Workshop on Machine Learning for CAD (**MLCAD**), Alberta, Canada, Sep. 3–4, 2019.
- [C9] **Yuzhe Ma**, Ran Chen, Wei Li, Fanhua Shang, Wenjian Yu, Minsik Cho, Bei Yu, “A Unified Approximation Framework for Compressing and Accelerating Deep Neural Networks”, IEEE International Conference on Tools with Artificial Intelligence (**ICTAI**), Portland, OR, Nov. 4–6, 2019. (**Best Student Paper Award**)
- [C8] Wei Li, **Yuzhe Ma**, Qi Sun, Yibo Lin, Iris Hui-Ru Jiang, Bei Yu, David Z. Pan, “OpenMPL: An Open Source Layout Decomposer”, IEEE International Conference on ASIC (**ASICON**), Chongqing, China, Oct. 29–Nov. 1, 2019.
- [C7] **Yuzhe Ma**, Haoxing Ren, Brucek Khailany, Harbinder Sikka, Karthikeyan Natarajan, and Bei Yu, “High Performance Graph Convolutional Networks with Applications in Testability Analysis”, ACM/IEEE Design Automation Conference (**DAC**), Las Vegas, NV, June 2–6, 2019.
- [C6] Hao Geng, Haoyu Yang, **Yuzhe Ma**, Joydeep Mitra, and Bei Yu, “SRAF Insertion via Supervised Dictionary Learning”, IEEE/ACM Asian and South Pacific Design Automation Conference (**ASPDAC**), Tokyo, Jan. 21–24, 2019. (**Best Paper Award Nomination**)
- [C5] Haoyu Yang, Shuhe Li, **Yuzhe Ma**, Bei Yu, and Evangeline F. Y. Young, “GAN-OPC: Mask Optimization with Lithography-guided Generative Adversarial Nets”, ACM/IEEE Design Automation Conference (**DAC**), San Francisco, CA, June 24–28, 2018.
- [C4] **Yuzhe Ma**, Jhih-Rong Gao, Jian Kuang, Jin Miao, and Bei Yu, “A Unified Framework for Simultaneous Layout Decomposition and Mask Optimization”, IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**), Irvine, CA, Nov. 13–16, 2017.
- [C3] Chak-Wa Pui, Gengjie Chen, **Yuzhe Ma**, Evangeline F. Y. Young, and Bei Yu, “Clock-Aware UltraScale FPGA Placement with Machine Learning Routability Prediction”, IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**), Irvine, CA, Nov. 13–16, 2017.
- [C2] **Yuzhe Ma**, Xuan Zeng, and Bei Yu, “Methodologies for Layout Decomposition and Mask Optimization: A Systematic Review”, IFIP/IEEE International Conference on Very Large Scale Integration (**VLSI-SoC**), Abu Dhabi, UAE, Oct. 23–25, 2017.
- [C1] Subhendu Roy, **Yuzhe Ma**, Jin Miao, and Bei Yu, “A Learning Bridge from Architectural Synthesis to Physical Design for Exploring Power Efficient High-Performance Adders”, IEEE/ACM International Symposium on Low Power Electronics and Design (**ISLPED**), Taipei, Taiwan, July 24–26, 2017.

Patents

- [P1] **Yuzhe Ma**, Haoxing Ren, Brucek Khailany, Harbinder Sikka, Lijuan Luo, Karthikeyan Natarajan, “Deep Learning Testability Analysis with Graph Convolutional Networks”, US Patent 10657306, May, 2020.

SELECTED AWARDS AND HONORS

Best Poster (Research) Award	ASPDAC SRF, ACM SIGDA	2020
Third Place Award	ISPD Contest	2020
Best Student Paper Award	ICTAI	2019
Best Paper Award Nomination	ASPDAC	2019
Full Postgraduate Studentship	The Chinese University of Hong Kong	2016 –
National Encouragement Scholarship	Sun Yat-sen University	2013, 2014, 2015
First Class Outstanding Academic Scholarship	Sun Yat-sen University	2013, 2014, 2015
Merit Student of Sun Yat-sen University	Sun Yat-sen University	2013, 2014, 2015

TECHNICAL SKILLS

Languages	C/C++, Python, MATLAB, L ^A T _E X
Operating Systems	Linux/UNIX, MacOS
Toolkits	PyTorch, Caffe