

$$\begin{array}{r} -8 \quad +7 \\ 1000 \quad 0111 \end{array}$$

$$\begin{array}{r} -8 \quad -7 \quad -6 \quad \dots \quad -1 \\ 1000 \quad 1111 \quad 1110 \quad \dots \quad 1001 \end{array}$$

$$\begin{array}{r} 0 \quad 1 \quad \dots \quad 7 \\ 0000 \quad 0001 \quad \dots \quad 0111 \end{array}$$

$$(-5) + (-7)$$

$$\begin{array}{r} \cancel{1011} \\ + \cancel{1011} \\ \hline \cancel{1011} \end{array}$$

12

$$5 + 6$$

$$\begin{array}{r} 0101 \\ + 0110 \\ \hline 0101 \end{array}$$

+ 11

$$-7 + 5$$

$$\begin{array}{r} 1001 \\ + 0101 \\ \hline 1001 \end{array}$$

-2

$$\begin{array}{r} 1011 \\ + 1001 \\ \hline 1100 \end{array}$$

$$\begin{array}{r} 10011 \\ + 11001 \\ \hline 101100 \end{array}$$

-12

BIT OVERFLOW

So don't need to consider edge cases in "two's complement."

(-8) two's complement

overflow

$$\begin{array}{r} 1000 \\ 1111 \\ \hline 1000 \end{array}$$

$$\begin{array}{r} 1001000 \quad (6 \text{ bits}) \\ 110111 \\ + 111000 \\ \hline 1000 \end{array}$$

equivalent to

$$\begin{array}{r} 1000 \\ 111000 \end{array}$$



8

1 0 0 0

reg signed [3:0] a

a = 4'1010

reg signed [7:0] b

b = a

// b = 8'11111010

min:  $-8 \times 4 = -32$

1 0 0 0 0 0

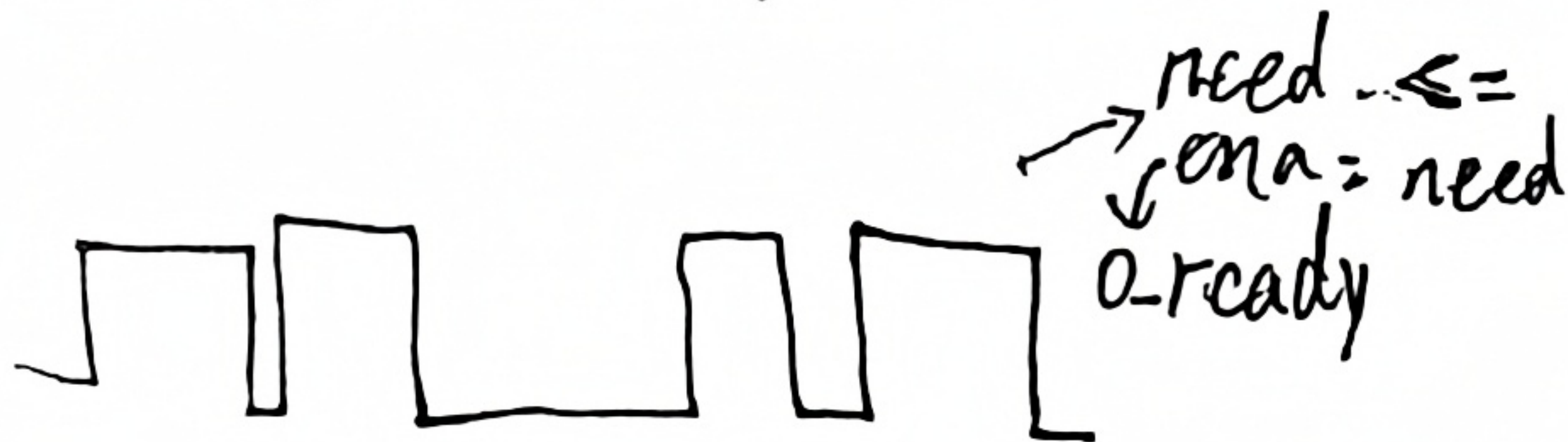
max:  $7 \times 4 = 28$

0 . . . .

[6 bits]

\* signed

next cycle



count = 4

000111

0001

110000

111001

111000

111001

$5 + -7 = -2$

~~000101~~  
~~111111~~  
~~1000100~~

000101  
+ 111001  
-----  
111110

testbench

$1 + 4 + (-7) + (-1)$   
 $= -3$

1 0 0 0

1 1 1 1

~~0 1 1 1~~

~~0 0 0 1~~

~~1 0 0 1~~

1 0 0 1 1

1 1 1 0 0 1

⊖ 1 1 1 1 0 1

1 0 0 0 1 0

1 0 0 0 0 1

1 0 0 0