-8 +7

1000 0111

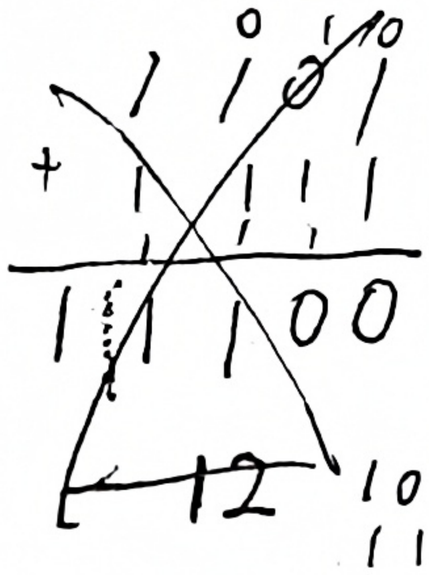
-8 -7 -6 ..... -1

1000 1111 1110 1001

0 1 7

0000 0001 0111

(-5)+(-7)



5+6

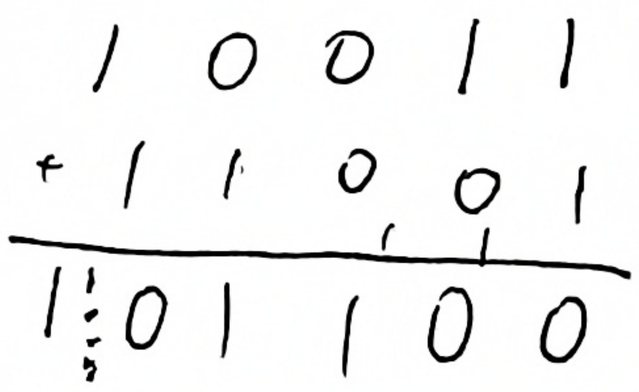
0101
+0110
01011
+11

-7 + 5

1001
+0101
10010
-2

1011
+1001
1100

BIT OVERFLOW



So don't need to consider edge cases in "twos_complement.v"

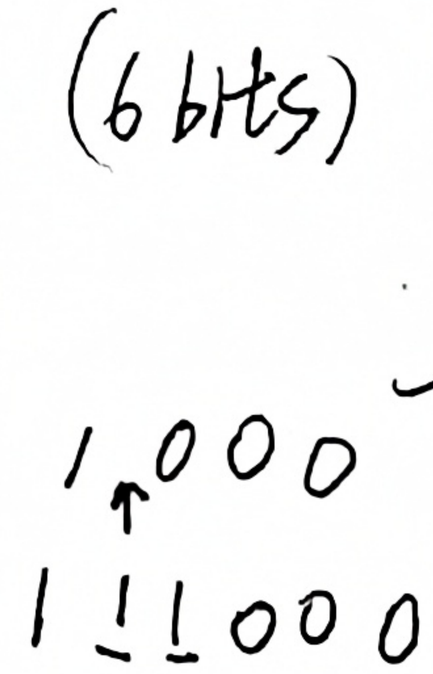
(-8) two's complement

1000 (6 bits)

overflow 1111

11000

equivalent to



-8

1000

reg signed [3:0] a

a = 4'1010

reg signed [7:0] b

b = a

// b = 8'1111 1010

min: -8×4 = -32

1 00000

max: 7×4 = 28

0 - - - -

[6 bits]

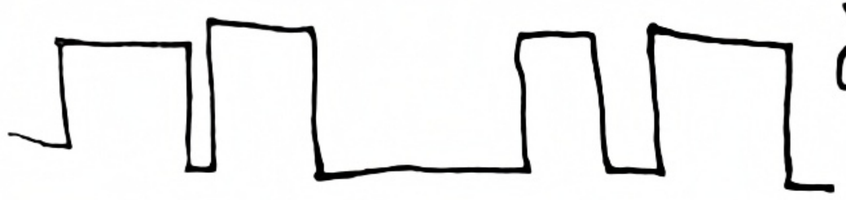
* signed

need <=

ena = need

o_rcady

next cycle



count = 4

0001

000111

+ 11000

11100

10011

111000

111001

testbench

1+4+(-7)+(-1)

= -3 = -3

5 + -7 = -2

00101

+ 111

1000100

000101

+ 111001

111110

1000

-

111101

1111

0+++

0001

+0001

100111

111001

100010

100001

1000