


FACULTY OF **ENGINEERING**

Building a better VHDL testing environment

Joren Guillaume

FEA
Ghent University

Prelimenary Presentation

Outline

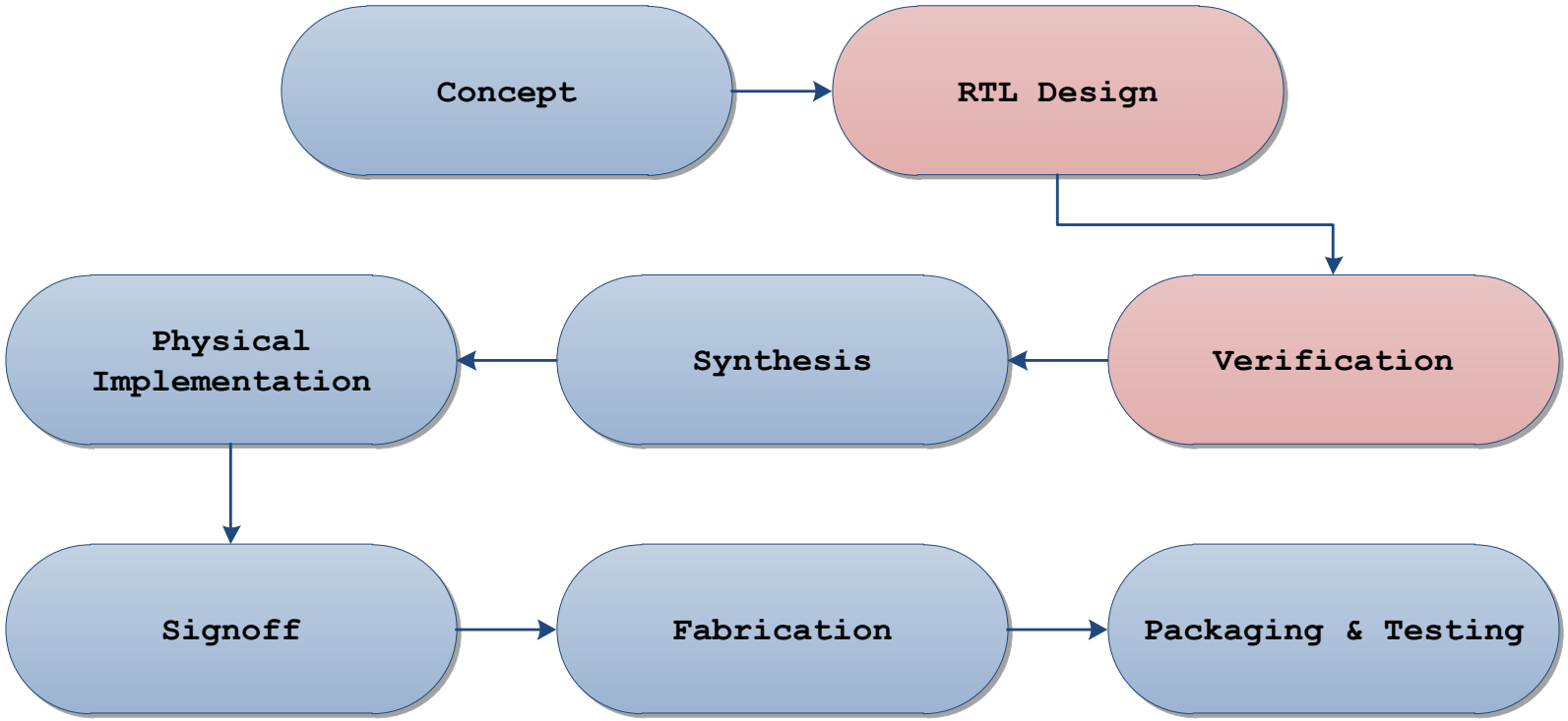
Outline

VHDL

VHDL

- VHSIC Hardware Description Language
- Developed by U.S. Department of Defense
  - Document → Simulate → Synthesize
- Used for describing digital and mixed-signal systems
- Compiled & simulated using special tools (e.g. ModelSim)

VHDL - design flow



Outline

Testing VHDL

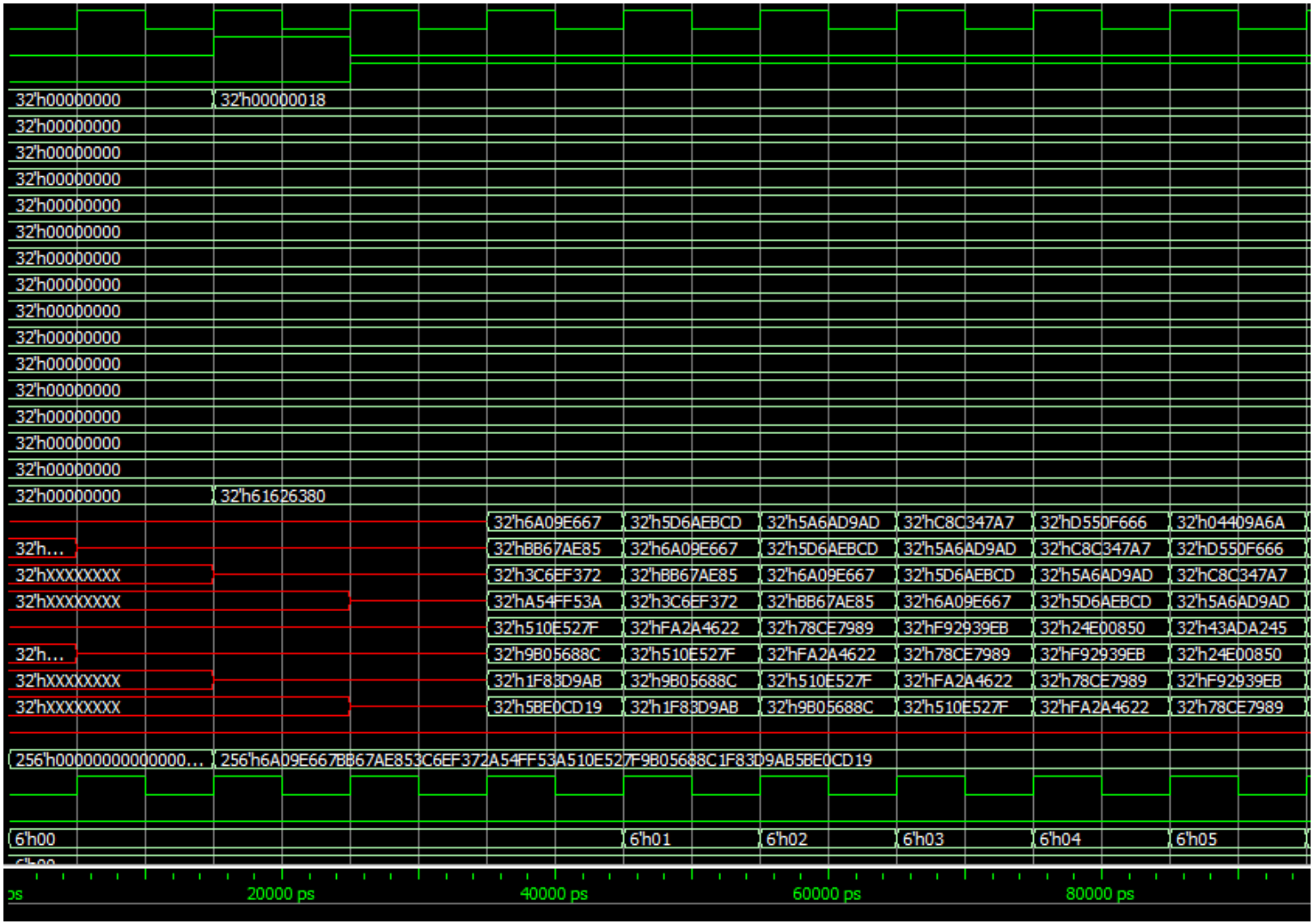
Testbenches

- Entity & architecture selection
- Signal drivers, stimuli & processes
- Assertions and output tracking
  - Comparison to "golden reference"
  - Wave-check
  - Manual check

Problems

- Non-standardized process
- Single point of failure

Modelsim - waves



Outline

VHDL testing framework

Standardized testing framework

- Based on Test Driven Development (TDD)
- Cross platform
- Utility library
  - Standardized testbenches
  - Swift coding
- Script-based processing → Standardized processing & output
- Continuous Integration (CI) system

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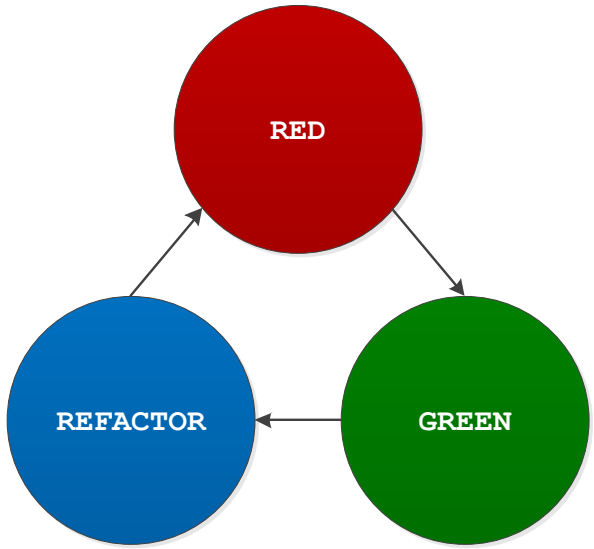
Test Driven Development

Test Driven Development

- Software development technique
- Proven to significantly reduce errors
- All behaviour is tested
- Unit testing & short development cycle
- Red - Green - Refactor



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Specialized library

Bitvis utility library

- Expands VHDL functions
  - Easy value checking
  - Clock & pulse generators
  - String handling & random generation
  - Easy output logging
- Quick & uniform coding
- Compatible with all VHDL versions

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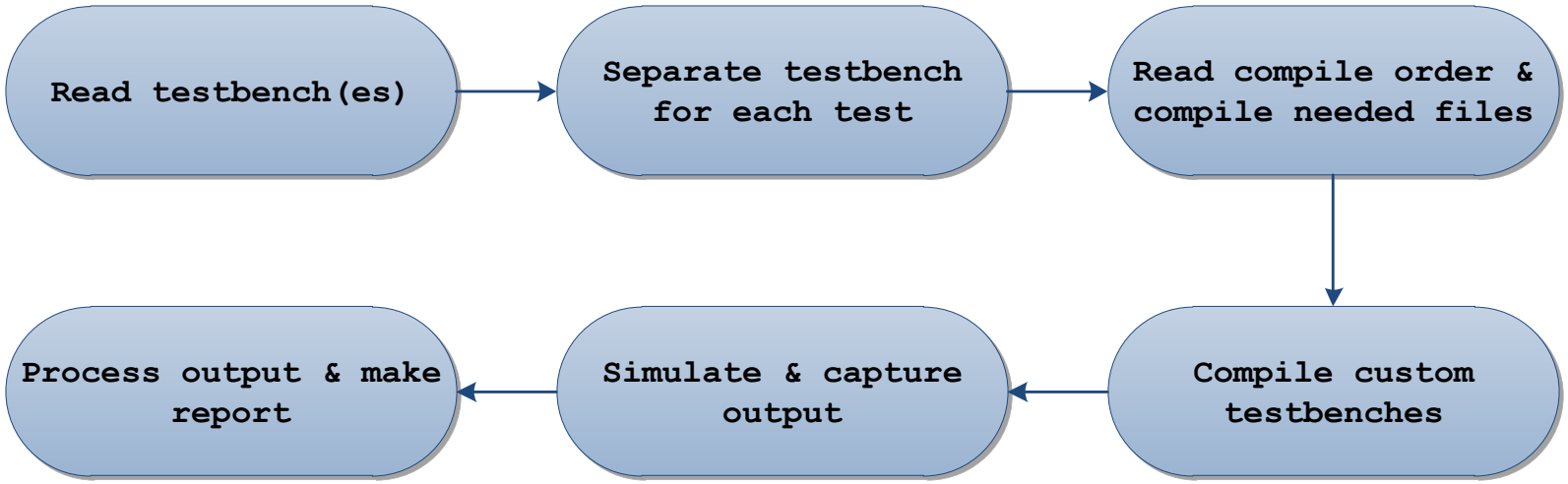
Script-based processing

Specialized python script



Script-based processing

Features

- Standalone functions
- Customizable process
- Different modes of separation
- Text & JUnit format reports
- Automated file cleanup

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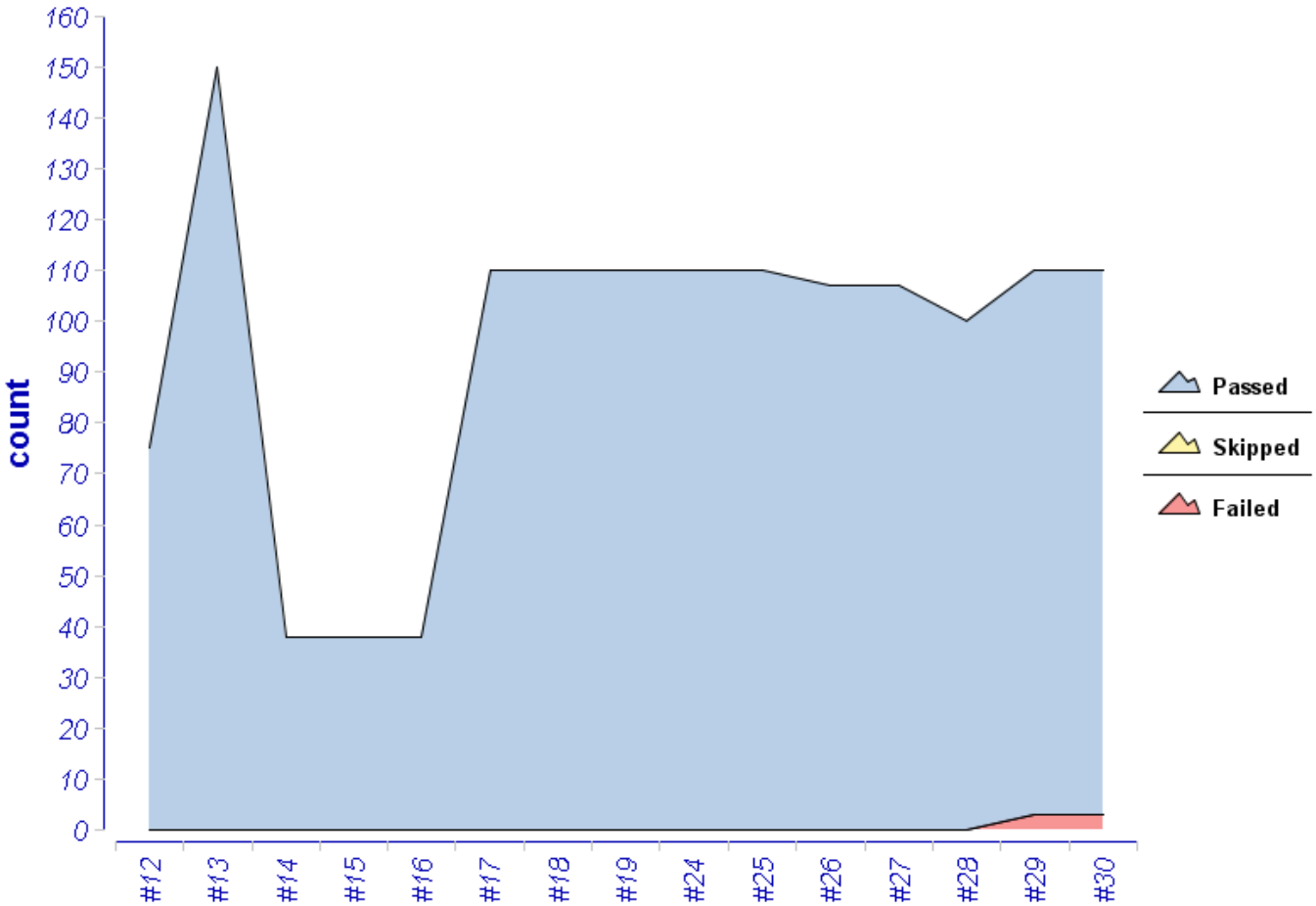
Continuous Integration

Hudson-CI

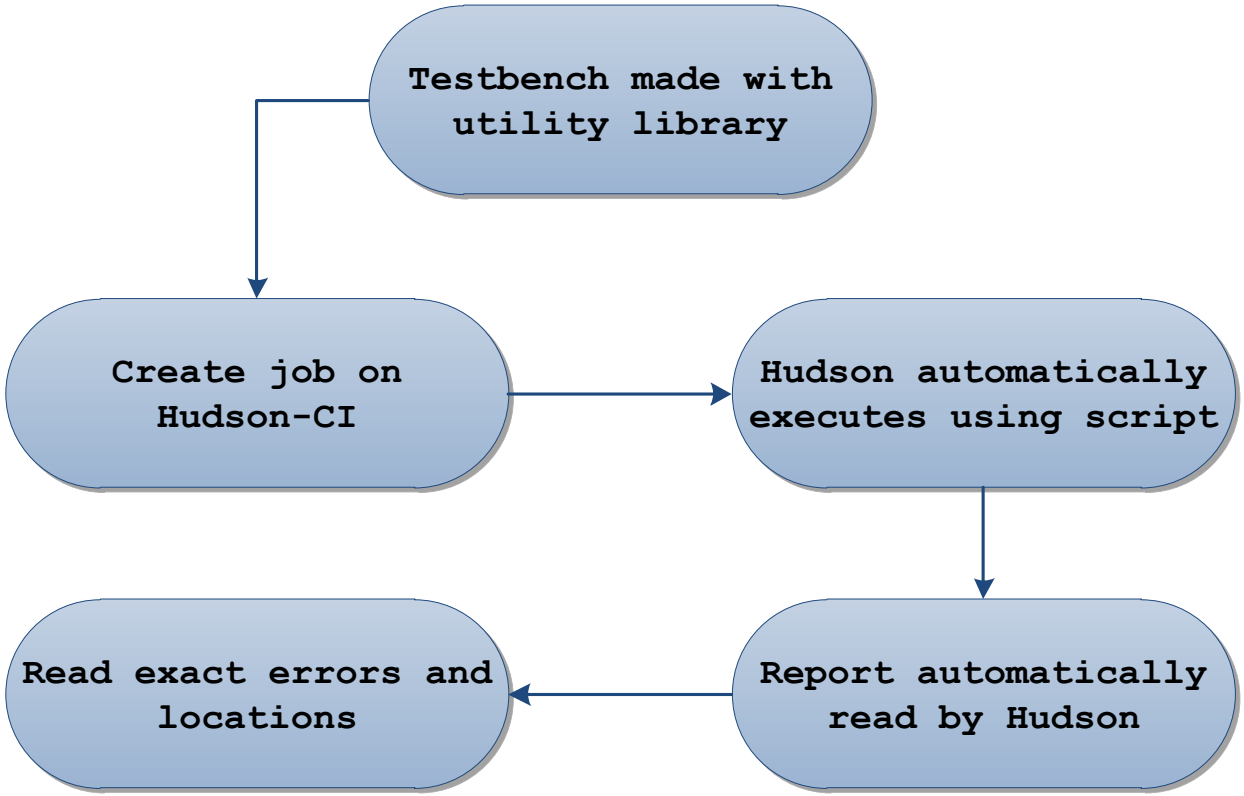
- Centralized, automated testing
- Revision control integration (e.g. Git)
- Statistics on success
- Standardized test reports (JUnit)
- Very customizable

Hudson interface

Hudson statistics



Framework design flow



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Problems

- VHDL has no reflection
  - Circumvent with higher level language
- Simulation is not synthesis
  - Wait statements, wrong sensitivity list ...
- Code duplication increases compile & simulation time
  - Implement regression testing
- Relatively few options
  - Further development

Outline

Future work

- Improving base script
  - Better integration utility library
  - More options
- Regression testing
- Proper documentation & examples

Outline

Demo