Building a better VHDL testing environment

Joren Guillaume

FEA
Ghent University

Prelimenary Presentation

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VHDL

VHDL

- VHSIC Hardware Description Language
- Used for describing digital and mixed-signal systems
- Simulated & compiled using special tools (e.g. ModelSim)

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Test Driven Development

Test Driven Development

- Software development process
- Write test first, write code second
- Unit testing with very short development cycle

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How is VHDL tested?

VHDL is tested using testbenches

- Architecture selection
- Signal drivers, stimuli & processes
- Assertions and output tracking

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Script-based processing

Python script

- Read pre-edited VHDL testbenches
- Divide into smaller tests
- Check faults after division
- Captures & processes output

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Continuous Integration

Hudson-CI

- Centralized, automated testing
- Revision control integration (e.g. Git)
- Statistics on success

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Specialized library

Bitvis Utility Library

- Expands VHDL functions
- Quick & uniform coding
- Compatible with all VHDL versions

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Problems

- Top-level blindness
  - No inner signal monitoring
  - Lack of inner testing & reporting
- TDD not fully implementable
  - No testing before code
  - Unit-testing impractical

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Future Work

- Improving base script
- Multi-level testbench integration