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================================================================
== Synthesis Summary Report of 'moller_hls'
================================================================
+ General Information:
    * Date:           Fri Jul 14 12:53:03 2023
    * Version:        2023.1 (Build 3854077 on May  4 2023)
    * Project:        LargeData
    * Solution:       wPragmas (Vivado IP Flow Target)
    * Product family: kintex7
    * Target device:  xc7k160t-fbg484-1


+ Performance & Resource Estimates:

    PS: '+' for module; 'o' for loop; '*' for dataflow
```

Modules & Loops	Issue Type	Slack	Latency (cycles)	Latency (ns)	Iteration Latency	Interval	Trip Count	Pipelined	BRAM	DSP	FF	LUT	URAM
+ moller_hls	-	0.18	354	3.540e+03	-	355	-	no	4 (~0%)	-	4230 (2%)	11221 (11%)	-
+ make_event	-	6.45	0	0.000	-	0	-	no	-	-	-	31 (~0%)	-
+ make_event	-	6.45	0	0.000	-	0	-	no	-	-	-	31 (~0%)	-
+ moller_hls_Pipeline_VITIS_LOOP_71_4	-	0.18	227	2.270e+03	-	227	-	no	2 (~0%)	-	500 (~0%)	1269 (1%)	-
o VITIS_LOOP_71_4	-	7.30	225	2.250e+03	3	1	224	yes	-	-	-	-	-
+ moller_hls_Pipeline_VITIS_LOOP_133_1	-	4.06	10	100.000	-	10	-	no	-	-	14 (~0%)	115 (~0%)	-
o VITIS_LOOP_133_1	-	7.30	8	80.000	1	1	8	yes	-	-	-	-	-

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== HW Interfaces
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* AP_FIFO
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Interface	Direction	Data Width
s_fadc_hits	out	3584
s_ring_all_t	out	512
s_ring_trigger	out	8
s_trigger	out	64

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* Other Ports
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Port	Mode	Direction	Bitwidth
energy_threshold	ap_none	in	13
ring_threshold	ap_none	in	16

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* TOP LEVEL CONTROL
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Interface	Type	Ports
ap_clk	clock	ap_clk

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| ap_rst     | reset      | ap_rst                           |
| ap_ctrl    | ap_ctrl_hs | ap_done ap_idle ap_ready ap_start |
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================================================================
== SW I/O Information
================================================================
* Top Function Arguments
+------------------+-----------+----------------------------+
| Argument         | Direction | Datatype                   |
+------------------+-----------+----------------------------+
| energy_threshold | in        | ap_uint<13>                |
| ring_threshold   | in        | ap_uint<16>                |
| s_fadc_hits      | in        | stream<fadc_hits_t, 0>&    |
| s_trigger        | out       | stream<trigger_t, 0>&      |
| s_ring_trigger   | out       | stream<ring_trigger_t, 0>& |
| s_ring_all_t     | out       | stream<ring_all_t, 0>&     |
+------------------+-----------+----------------------------+
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* SW-to-HW Mapping
+------------------+------------------+-----------+
| Argument         | HW Interface     | HW Type   |
+------------------+------------------+-----------+
| energy_threshold | energy_threshold | port      |
| ring_threshold   | ring_threshold   | port      |
| s_fadc_hits      | s_fadc_hits      | interface |
| s_trigger        | s_trigger        | interface |
| s_ring_trigger   | s_ring_trigger   | interface |
| s_ring_all_t     | s_ring_all_t     | interface |
+------------------+------------------+-----------+
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================================================================
== Bind Op Report
================================================================
+---------------------------------------+-----+--------+-------------+-----+--------+---------+
| Name                                  | DSP | Pragma | Variable    | Op  | Impl   | Latency |
+---------------------------------------+-----+--------+-------------+-----+--------+---------+
| + moller_hls                          | 0   |        |             |     |        |         |
|   + moller_hls_Pipeline_VITIS_LOOP_71_4 | 0 |        |             |     |        |         |
|     add_ln71_fu_755_p2                | -   |        | add_ln71    | add | fabric | 0       |
|     allr_e_8_fu_960_p2                | -   |        | allr_e_8    | add | fabric | 0       |
|     allr_nhits_8_fu_998_p2            | -   |        | allr_nhits_8 | add | fabric | 0       |
|   + moller_hls_Pipeline_VITIS_LOOP_133_1 | 0 |       |             |     |        |         |
|     add_ln133_fu_137_p2               | -   |        | add_ln133   | add | fabric | 0       |
+---------------------------------------+-----+--------+-------------+-----+--------+---------+
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================================================================
== Bind Storage Report
================================================================
+---------------------------------------+------+------+--------+-------------------------+---------+------+---------+
| Name                                  | BRAM | URAM | Pragma | Variable                | Storage | Impl | Latency |
+---------------------------------------+------+------+--------+-------------------------+---------+------+---------+
| + moller_hls                          | 4    | 0    |        |                         |         |      |         |
|   arr_event_e_U                       | 1    | -    |        | arr_event_e             | ram_t2p | auto | 1       |
|   arr_event_t_U                       | -    | -    |        | arr_event_t             | ram_t2p | auto | 1       |
|   fadc_hits_pre_e_U                   | 1    | -    |        | fadc_hits_pre_e         | ram_t2p | auto | 1       |
|   fadc_hits_pre_t_U                   | -    | -    |        | fadc_hits_pre_t         | ram_t2p | auto | 1       |
|   + moller_hls_Pipeline_VITIS_LOOP_71_4 | 2  | 0    |        |                         |         |      |         |
|     arr_chan_map_DET_ID_U             | -    | -    |        | arr_chan_map_DET_ID     | rom_1p  | auto | 1       |
|     arr_chan_map_SEG_NUM_U            | 1    | -    |        | arr_chan_map_SEG_NUM    | rom_1p  | auto | 1       |
```

Firefox

file:///C:/Users/mrcco/AppData/Roaming/Xilinx/Vitis/LargeData/wPra...

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|
|      arr_chan_map_SUB_ELEMENT_U          | 1    | -    |        | arr_chan_map_SUB_ELEMENT | rom_1p  | auto | 1
|
+-------------------------------------+------+------+--------+--------------------------+---------+------+-------
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================================================================
== Pragma Report
================================================================
* Valid Pragma Syntax
+----------------+--------------------------------------------+---------------------------------------------------
-------------------------------------------+
| Type           | Options                                    | Location
|
+----------------+--------------------------------------------+---------------------------------------------------
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| array_partition | dim=1 type=complete variable=time_bitmap.trig | ../../../../Documents/Vitis/LargerDataSet
/moller_hls.cpp:52 in moller_hls, time_bitmap.trig |
| array_partition | dim=1 type=complete variable=allr.r          | ../../../../Documents/Vitis/LargerDataSet
/moller_hls.cpp:54 in moller_hls, allr.r            |
| unroll          |                                              | ../../../../Documents/Vitis/LargerDataSet
/moller_hls.cpp:65 in moller_hls                    |
+----------------+--------------------------------------------+---------------------------------------------------
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