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================================================================
== Vivado RTL Synthesis Results
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+ General Information:
    * Date:            Fri Jul 14 11:35:18 -0400 2023
    * Version:         2023.1 (Build 3854077 on May  4 2023)
    * Project:         LargeData
    * Solution:        wPragmas (Vivado IP Flow Target)
    * Product family:  kintex7
    * Target device:   xc7k160t-fbg484-1


================================================================
== Run Constraints & Options
================================================================
+ Design Constraints & Options:
    * RTL Synthesis target clock:  10 ns
    * C-Synthesis target clock:    10 ns
    * C-Synthesis uncertainty:     27%

+ RTL Synthesis Options:
    * config_export -vivado_synth_strategy:     default
    * config_export -vivado_synth_design_args:  -directive sdx_optimization_effort_high

+ Reporting Options:
    * config_export -vivado_report_level:      2
    * config_export -vivado_max_timing_paths:  10


================================================================
== RTL Synthesis Resource Summary
================================================================
LUT:              4556
FF:               4215
DSP:              0
BRAM:             5
URAM:             0
SRL:              0


================================================================
== RTL Synthesis Timing Summary
================================================================
* Timing was met
+----------------+-------------+
| Timing         | Period (ns) |
+----------------+-------------+
| Target         | 10.000      |
| Post-Synthesis | 5.047       |
+----------------+-------------+


================================================================
== RTL Synthesis Resources
================================================================
+-------------------------------------------------------+------+------+-----+------+------+-----+---------+------+--
-------+-------------------------+-----------------------------------------------------------------------+
| Name                                                  | LUT  | FF   | DSP | BRAM | URAM | SRL | Pragma | Impl |
Latency | Variable                | Source                                                                |
+-------------------------------------------------------+------+------+-----+------+------+-----+---------+------+--
-------+-------------------------+-----------------------------------------------------------------------+
| inst                                                  | 4556 | 4215 |     | 5    |      |     |         |      |
|                         |                                                                       |
|   (inst)                                              | 23   | 3704 |     |      |      |     |         |      |
|                         |                                                                       |
|   arr_event_e_U                                       | 1581 |      |     | 1    |      |     |         |      |
|                         |                                                                       |
|     bind_storage ram_t2p                              |      |      |     |      |      |     |         | auto | 1
| arr_event_e             | ../../../../Documents/Vitis/LargerDataSet/moller_hls.cpp:55           |
|   arr_event_t_U                                       | 521  |      |     | 1    |      |     |         |      |
|                         |                                                                       |
|     bind_storage ram_t2p                              |      |      |     |      |      |     |         | auto | 1
```

arr_event_t	../../../../Documents/Vitis/LargerDataSet/moller_hls.cpp:55								
fadc_hits_pre_e_U		1494			1				
bind_storage ram_t2p								auto	1
fadc_hits_pre_e									
fadc_hits_pre_t_U		643			1				
bind_storage ram_t2p								auto	1
fadc_hits_pre_t									
grp_moller_hls_Pipeline_VITIS_LOOP_133_1_fu_7515		20	14						
(grp_moller_hls_Pipeline_VITIS_LOOP_133_1_fu_7515)			12						
grp_moller_hls_Pipeline_VITIS_LOOP_71_4_fu_7469		274	497		1				
(grp_moller_hls_Pipeline_VITIS_LOOP_71_4_fu_7469)		248	489		1				
arr_chan_map_DET_ID_U		3	3						
bind_storage rom_1p								auto	1
arr_chan_map_DET_ID									
arr_chan_map_SUB_ELEMENT_U		3	3						
bind_storage rom_1p								auto	1
arr_chan_map_SUB_ELEMENT									
flow_control_loop_pipe_sequential_init_U		20	2						

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== RTL Synthesis Fail Fast
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Criteria	Guideline	Actual	Status
LUT	70%	4.49%	OK
FD	50%	2.08%	OK
LUTRAM+SRL	25%	0.00%	OK
MUXF7	15%	0.10%	OK
DSP	80%	0.00%	OK
RAMB/FIFO	80%	0.77%	OK
DSP+RAMB+URAM (Avg)	70%	0.77%	OK
BUFGCE* + BUFGCTRL	24	0	OK
DONT_TOUCH (cells/nets)	0	0	OK
MARK_DEBUG (nets)	0	0	OK
Control Sets	1901	14	OK
Average Fanout for modules > 100k cells	4	0	OK
Non-FD high fanout nets > 10k loads	0	0	OK
TIMING-6 (No common primary clock between related clocks)	0	0	OK
TIMING-7 (No common node between related clocks)	0	0	OK
TIMING-8 (No common period between related clocks)	0	0	OK
TIMING-14 (LUT on the clock tree)	0	0	OK
TIMING-35 (No common node in paths with the same clock)	0	0	OK
Number of paths above max LUT budgeting (0.575ns)	0	0	OK
Number of paths above max Net budgeting (0.403ns)	0	0	OK

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== RTL Synthesis Timing Paths
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* Timing was met

Path	SLACK	STARTPOINT PIN	ENDPOINT PIN	LOGIC LEVELS	MAX FANOUT	DATAPATH DELAY	DATAPATH LOGIC DELAY	DATAPATH NET DELAY

Path1	4.953	fadc_hits_t_207_reg_14918_reg[2]/C	arr_event_e_U/ram_reg/DIBDI[0]	6	15	4.354	0.699	3.655
Path2	4.953	fadc_hits_t_207_reg_14918_reg[2]/C	arr_event_e_U/ram_reg/DIBDI[10]	6	15	4.354	0.699	3.655
Path3	4.953	fadc_hits_t_207_reg_14918_reg[2]/C	arr_event_e_U/ram_reg/DIBDI[11]	6	15	4.354	0.699	3.655
Path4	4.953	fadc_hits_t_207_reg_14918_reg[2]/C	arr_event_e_U/ram_reg/DIBDI[12]	6	15	4.354	0.699	3.655
Path5	4.953	fadc_hits_t_207_reg_14918_reg[2]/C	arr_event_e_U/ram_reg/DIBDI[1]	6	15	4.354	0.699	3.655

Path1 Cells	Primitive Type
fadc_hits_t_207_reg_14918_reg[2]	FLOP_LATCH.flop.FDRE
arr_event_e_U/ram_reg_i_1914	LUT.others.LUT6
arr_event_e_U/ram_reg_i_1473	LUT.others.LUT5
arr_event_e_U/ram_reg_i_727	LUT.others.LUT6
arr_event_e_U/ram_reg_i_353	LUT.others.LUT5
arr_event_e_U/ram_reg_i_144	LUT.others.LUT6
fadc_hits_pre_e_U/ram_reg_i_43	LUT.others.LUT6
arr_event_e_U/ram_reg	BMEM.bram.RAMB18E1

Path2 Cells	Primitive Type
fadc_hits_t_207_reg_14918_reg[2]	FLOP_LATCH.flop.FDRE
arr_event_e_U/ram_reg_i_1914	LUT.others.LUT6
arr_event_e_U/ram_reg_i_1473	LUT.others.LUT5
arr_event_e_U/ram_reg_i_727	LUT.others.LUT6
arr_event_e_U/ram_reg_i_353	LUT.others.LUT5
arr_event_e_U/ram_reg_i_144	LUT.others.LUT6
fadc_hits_pre_e_U/ram_reg_i_33	LUT.others.LUT6
arr_event_e_U/ram_reg	BMEM.bram.RAMB18E1

Path3 Cells	Primitive Type
fadc_hits_t_207_reg_14918_reg[2]	FLOP_LATCH.flop.FDRE
arr_event_e_U/ram_reg_i_1914	LUT.others.LUT6
arr_event_e_U/ram_reg_i_1473	LUT.others.LUT5
arr_event_e_U/ram_reg_i_727	LUT.others.LUT6
arr_event_e_U/ram_reg_i_353	LUT.others.LUT5
arr_event_e_U/ram_reg_i_144	LUT.others.LUT6
fadc_hits_pre_e_U/ram_reg_i_32	LUT.others.LUT6
arr_event_e_U/ram_reg	BMEM.bram.RAMB18E1

Path4 Cells	Primitive Type
fadc_hits_t_207_reg_14918_reg[2]	FLOP_LATCH.flop.FDRE
arr_event_e_U/ram_reg_i_1914	LUT.others.LUT6
arr_event_e_U/ram_reg_i_1473	LUT.others.LUT5
arr_event_e_U/ram_reg_i_727	LUT.others.LUT6
arr_event_e_U/ram_reg_i_353	LUT.others.LUT5
arr_event_e_U/ram_reg_i_144	LUT.others.LUT6
fadc_hits_pre_e_U/ram_reg_i_31	LUT.others.LUT6
arr_event_e_U/ram_reg	BMEM.bram.RAMB18E1

Path5 Cells	Primitive Type
fadc_hits_t_207_reg_14918_reg[2]	FLOP_LATCH.flop.FDRE
arr_event_e_U/ram_reg_i_1914	LUT.others.LUT6
arr_event_e_U/ram_reg_i_1473	LUT.others.LUT5
arr_event_e_U/ram_reg_i_727	LUT.others.LUT6

arr_event_e_U/ram_reg_i_353	LUT.others.LUT5
arr_event_e_U/ram_reg_i_144	LUT.others.LUT6
fadc_hits_pre_e_U/ram_reg_i_42	LUT.others.LUT6
arr_event_e_U/ram_reg	BMEM.bram.RAMB18E1

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== RTL Synthesis Vivado Reports
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Report Type	Report Location
design_analysis	impl/verilog/report/moller_hls_design_analysis_synth.rpt
failfast	impl/verilog/report/moller_hls_failfast_synth.rpt
timing	impl/verilog/report/moller_hls_timing_synth.rpt
timing_paths	impl/verilog/report/moller_hls_timing_paths_synth.rpt
utilization	impl/verilog/report/moller_hls_utilization_synth.rpt
utilization_hierarchical	impl/verilog/report/moller_hls_utilization_hierarchical_synth.rpt