Lecture 4: Op amp Circuits

EE 103

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Problems of BJT based Amplifiers

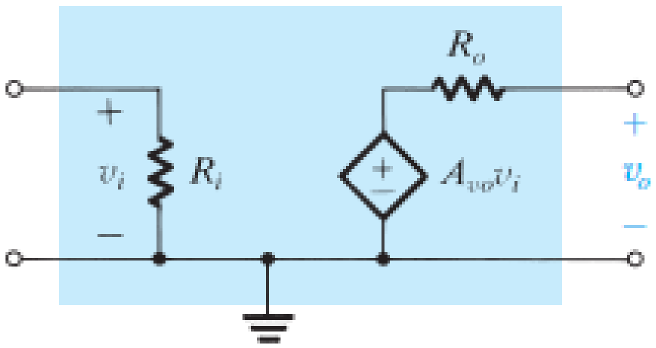
- Voltage gain depends on the device parameters

  (which in turn depends on temperature and also vary from device to device)

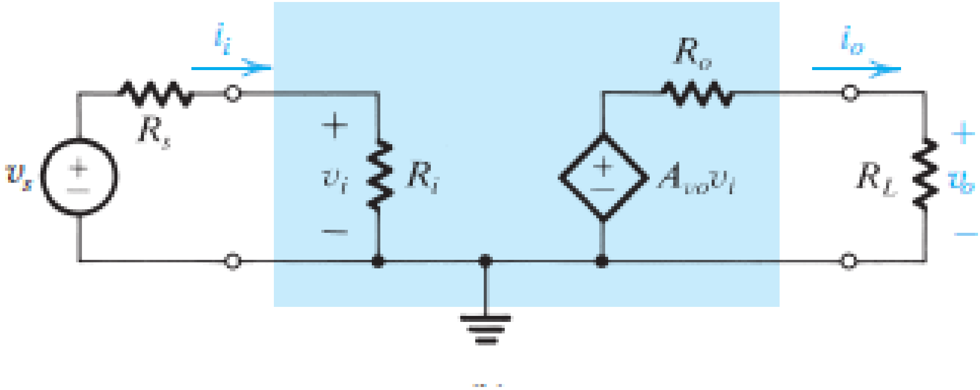
- For example, the gain of a BJT Common-Emitter amplifier is:

  $-g_m R_C \| R_L$
- Solution:
  - Cascaded amplifiers

Amplifier Requirements



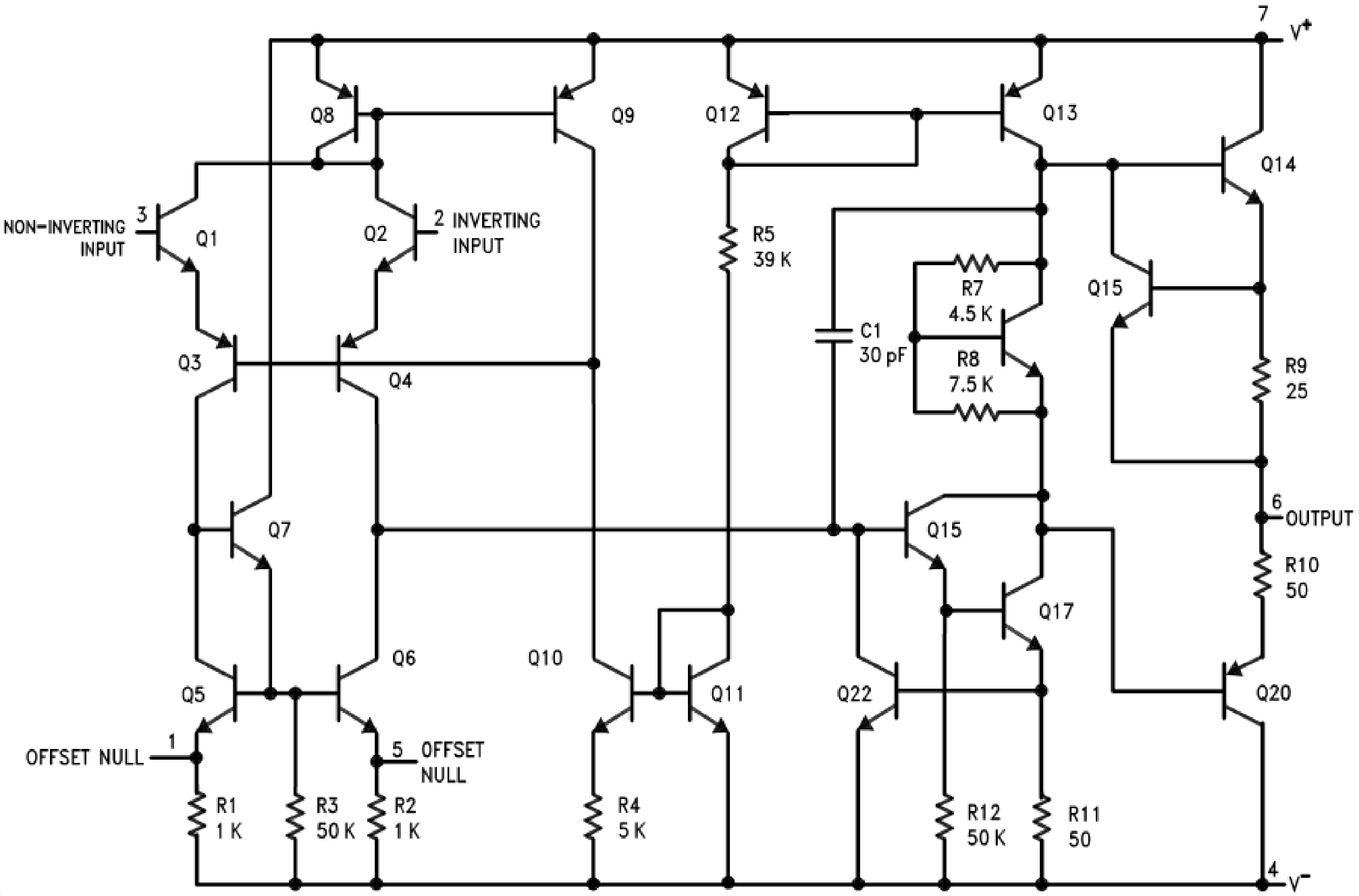
(a)



- Input side requirements
  - Input resistance (R_i) of the amplifier should be ideally infinite.

- Load requirements
  - Output resistance (R_o) of the amplifier should be ideally 0.

LM 741 Op amp



- **Three major blocks:**
  - Input block: gives very high input resistance and also a voltage gain of about 1000.
- A gain clock:
  - gives a voltage gain of about 1000.
- Output stage:
  - Unity voltage gain but very high current gain; also provides short-circuit protection to the output

3. Operational Amplifier

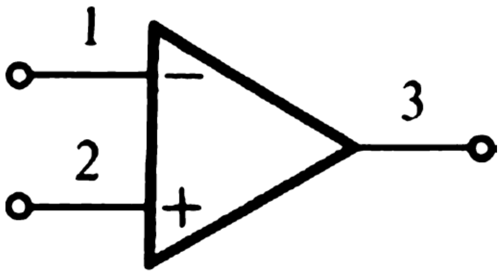
Operational amplifier (op amp)

Direct-coupled (dc) high-gain amplifier with differential voltage input & single-ended voltage output.

• Developed for mathematical operations on signal waveforms. It is an electronic circuit with several internal passive & active devices, available as a single-chip device, several op amps on a single chip, or op amps with other circuits on the same chip.

• Main objective: Circuit performance parameters decided by passive components & nearly independent of electronic device parameters.

Op amp circuit symbol (simplified)



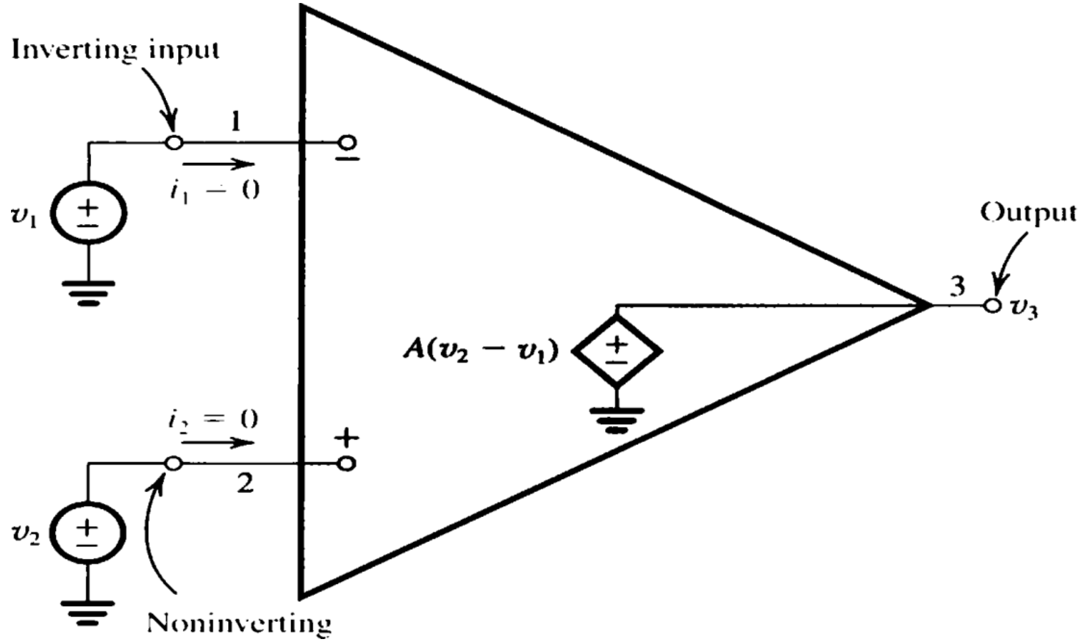
• Input terminals: 1, 2. Output terminal: 3.

• 3 single-ended ports with the circuit ground (Gnd) as the common terminal (implied, not shown in the symbol).

• Inverting input v_{i-}: 1-Gnd. Non-inverting input v_{i+}: 2-Gnd. Output v_o: 3-Gnd.

Input-output relation

- Terminal voltage: voltage between the terminal & Gnd.
- Difference-mode (DM) input $v_{id} = v_2 - v_1$.
- Common-mode (CM) input $v_{ic} = (v_2 + v_1)/2$.
- Output voltage $v_3 = A_d v_{\mathrm{id}} + A_c v_{\mathrm{ic}}$.
- DM gain: A_d. CM gain: A_c.
- Common-mode rejection ratio (CMRR) $= A_d/A_c$.



Ideal op amp

- $A_d \to \infty$. $A_c \to 0$. $v_3 = A_d(v_2 - v_1)$

DM input amplification with no effect of CM input. Finite output voltage obtained with zero DM input.

CMRR $= A_d/A_c \to \infty$.

- Infinite input resistances for the two inputs (zero input currents) .
- Zero output resistance (output voltage independent of the load current).

Op amp in linear operation

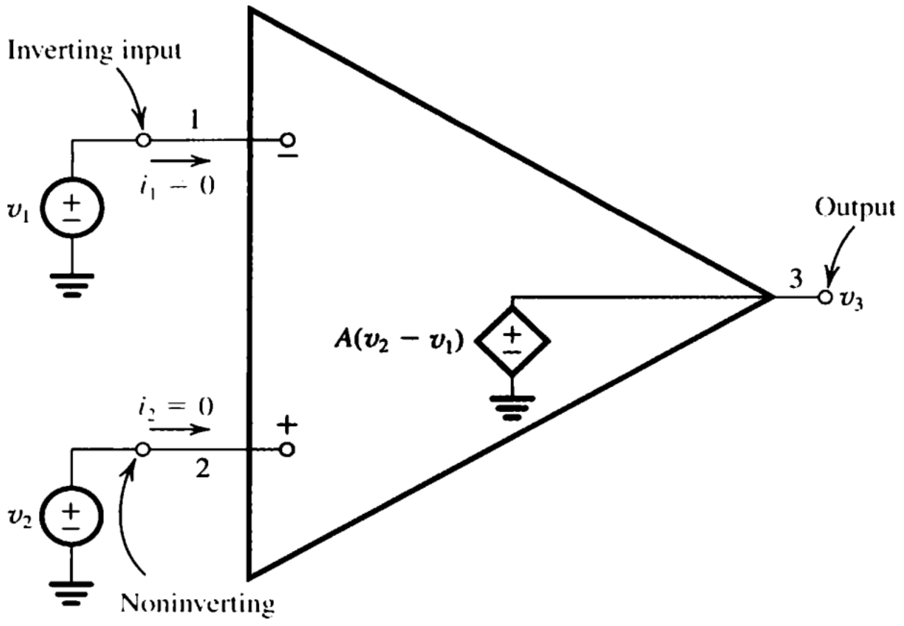
• $v_3 = A_d v_{\mathrm{id}}$

For finite output v_3 and $A_d \to \infty$, DM input $v_{\mathrm{id}} = v_3/A_d \to 0$.

• Input resistances R_{i1}, $R_{i2} \to \infty \Rightarrow$ zero input currents.

• Zero voltage across the input terminals with zero input currents is known as "virtual short" across the input terminals.

• Virtual short condition is very useful in analyzing linear op amp circuits.

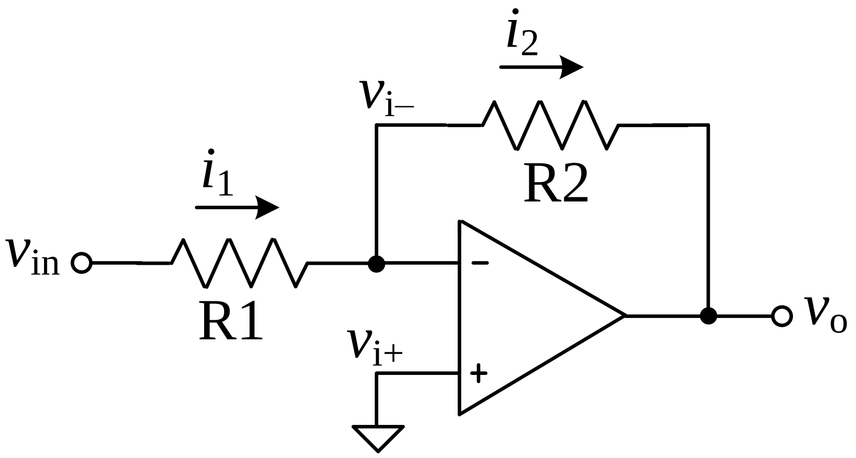


• Virtual short is applicable only during linear operation, & the conditions for it have to be satisfied by external circuit & input voltages. Input currents may increase and output may be distorted during nonlinear operation. Input and output voltage limits for linear operation:

CM input: $V_{CC+} > V_{ICH} > [v_1, v_2] > V_{ICL} > V_{CC-}$.
Output: $V_{CC+} > V_{OH} > v_3 > V_{OL} > V_{CC-}$.

4. Linear Circuits

4.1. Inverting Amplifier Circuit



$v_{i+} = 0.$
Virtual short: $v_{i-} = v_{i+} = 0.$ $i_1 = i_2.$
$i_2 = i_1 = (v_{in} - v_{i-})/R_1 = v_{in}/R_1$
$v_o = v_{i-} - R_2\, i_2 = -\,(R_2/R_1)\, v_{in}$
Voltage gain: $A_v = v_o/\, v_{in} = -\,R_2/R_1$.
Input resistance: $R_{in} = v_{in}\,/i_1 = R_1$.

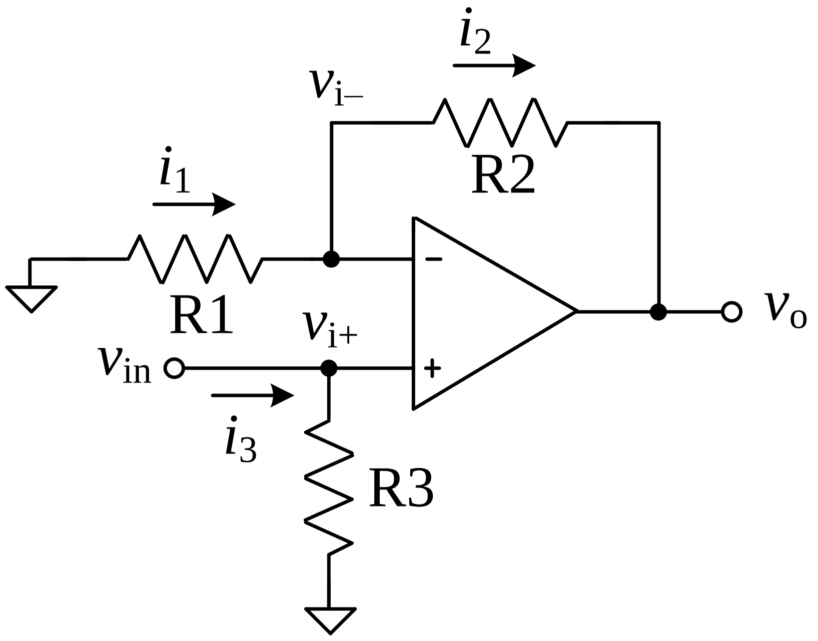
Circuit operation basis: Negative feedback (visited later), which opposes disturbance. Check the circuit operation with virtual short assumption and a disturbance at the −ve input. If v_{i-} increases, v_o decreases, i_2 increases, v_{i-} decreases, leading to virtual short restoration. If the op-amp input terminals are interchanged, an increase in v_{i+} will cause further increase leading to virtual short violation.

Current & power gains depend on load resistance (not shown). R_{in} can be decreased by connecting a resistor between input and ground.

Application: Precise inverting gain with low to moderate R_{in}.

Example: $R_1 = 10$ kΩ, $R_2 = 100$ kΩ. $R_L = 1$ kΩ. $A_v = -10$, $R_{in} = 10$ kΩ .

4.2. Non-inverting Amplifier Circuit



$v_{i+} = v_{in}$

Virtual short assumption: $v_{i-} = v_{i+}$ & $i_1 = i_2$

$i_1 = (0 - v_{i-})/R_1 = -v_{in}/R_1$

$v_o = v_{i+} - R_2\, i_2 = (1 + R_2/R_1)\, v_{in}$

Voltage gain: $A_v = v_o/\, v_{in} = 1 + R_2/R_1$

Input resistance: $R_{in} = v_{in}/i_3 = R_3$

R3 is optional & can be selected for the desired R_{in}.

Basis for circuit operation: Negative feedback. Check the circuit operation, with virtual short assumption & a disturbance at the –ve input. If v_{i-} increases, v_o decreases, i_2 increases, v_{i-} decreases, leading to virtual short restoration. Next check with the op-amp input terminals interchanged.

Application: Precise non-inverting gain with high, moderate, or low R_{in}.

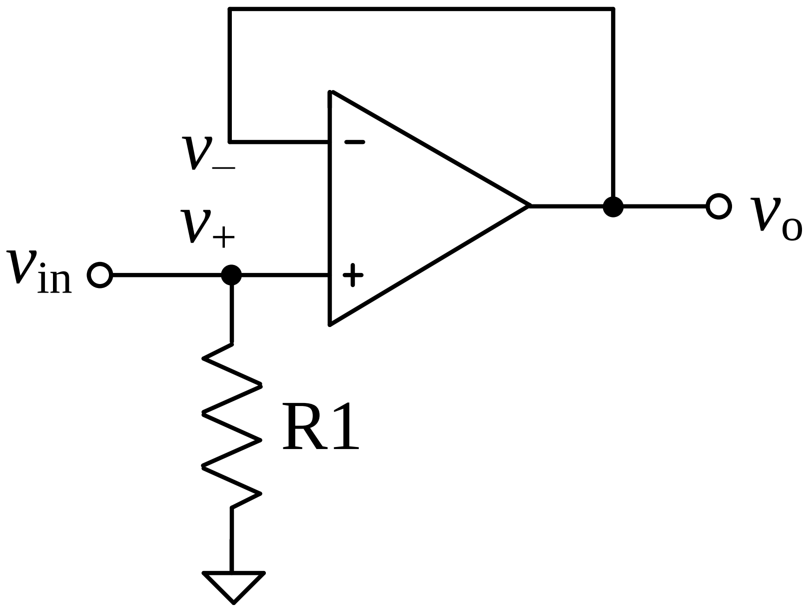
Example: $R_1 = 10\ \text{k}\Omega$, $R_2 = 100\ \text{k}\Omega$, $R_3 = 1\ \text{M}\Omega$, $A_v = 11$, $R_{in} = 1\ \text{M}\Omega$.

4.3. Non-inverting Unity Follower Circuit (Unity Buffer)

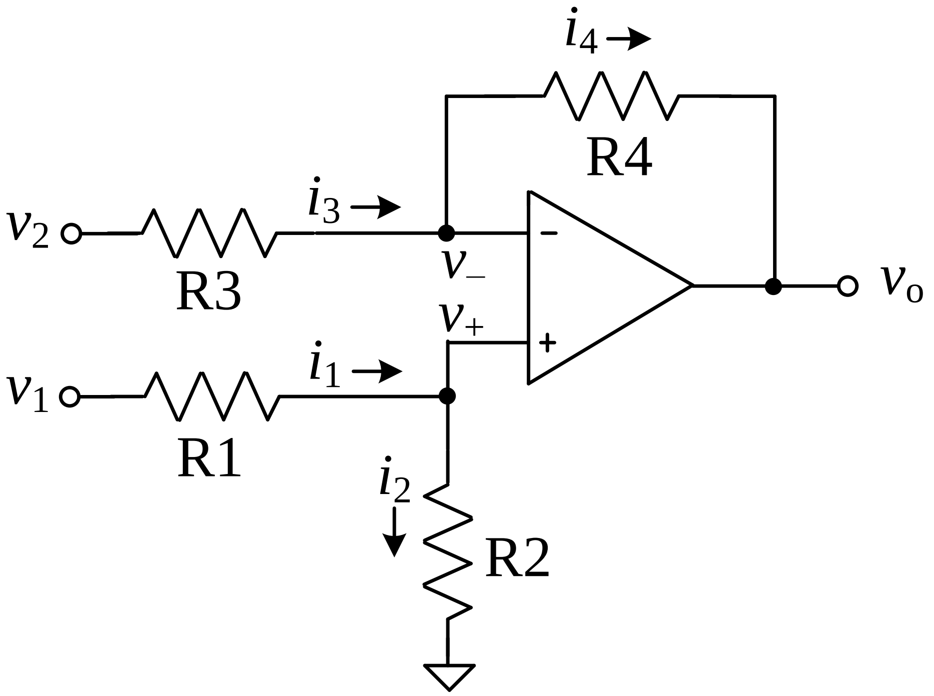
It is a special case of non-inverting amplifier with unity voltage gain.

Voltage gain: $A_v = 1$
Input resistance: $R_{in} = R_1$

Application: Buffer amplifier with very high R_{in} and very low R_o. It is used for connecting a source with high source resistance to a relatively low value load resistance without causing voltage attenuation. It provides unity voltage gain and large current gain.



4.4. Difference Amplifier Circuit



Select $R_2/R_1 = R_4/R_3 = \alpha$.

Virtual short assumption: $i_1 = i_2$ & $i_3 = i_4$.

Circuit function: (i) inverting amplifier for v_2, (ii) attenuator & non-inverting amplifier for v_1.

$$v_o = v_1 [R_2/(R_1+R_2] [1+R_4/R_3] - v_2 [R_4/R_3]$$

$$= v_1 [\alpha/(1+\alpha)][1+\alpha] - v_2 [\alpha] = \alpha (v_1 - v_2)$$

DM gain $A_d = \alpha$.

CM gain $A_c = 0$

$R_{in1} = R_1 + R_2$, $R_{in2} = R_3$.

- Precise differential gain. Resistance matching needed. Difficult gain control. Unequal input resistances.
- A voltage (DC bias) v_3 can be added to the output by connecting R2 to this voltage in place of ground.

$$v_o = \alpha (v_1 - v_2) + v_3[1/(1+\alpha)] /(1+\alpha)] = \alpha (v_1 - v_2) + v_3$$

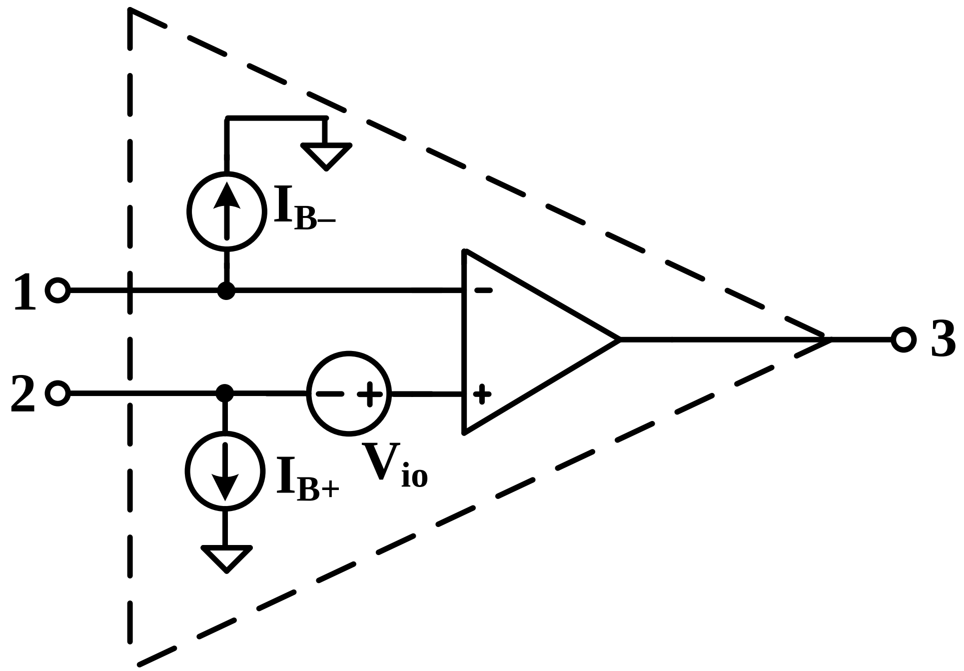
4.9. Practical Op Amp

• Op-amp linear operation has limits for CM input voltage, output voltage, & output current (due to DC supplies & internal circuit)

• DC imperfections

- Input offset voltage (internal error voltage: 1–5 mV) causing output saturation in high-gain circuits.
- Input bias currents: Small DC input currents (10 pA to 100 nA). These must be permitted by external circuit for proper operation.

• Finite input & output resistances.



Op-amp DC error model

• Finite diff. gain (typically > 10^5 at dc, decreasing with frequency), finite CMRR. Another limitation for large amplitude AC signals is “slew rate”, the maximum rate of change of output voltage (typically 1 V/μs).

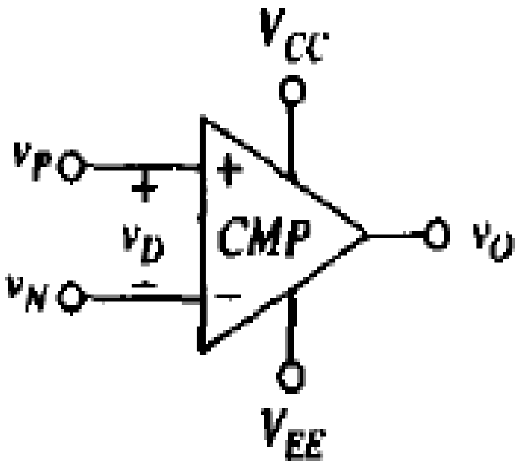
6. Nonlinear Circuits

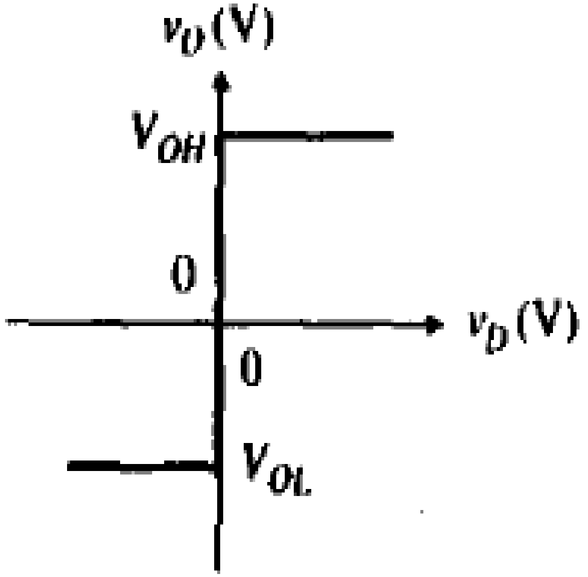
Voltage Comparator

Op-amp like device for open-loop operation & precise binary output levels.

$v_p > v_n$: $v_o = V_{OH}$ (high-level voltage)

$v_p < v_n$: $v_o = V_{OL}$ (low-level voltage)





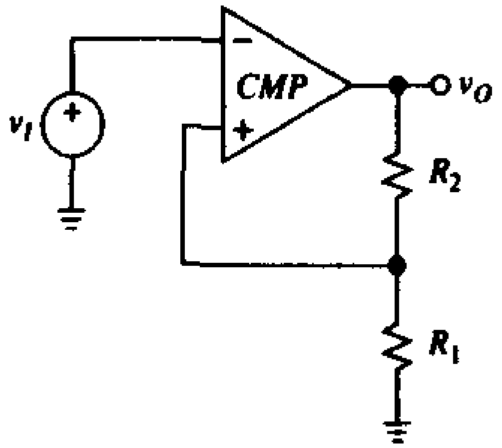
- Circuit symbol: same as op amp, with analog inputs, binary output. Transfer characteristic: Very high gain at $v_p = v_n$ with sharp transition between the two output levels.
- Input swing and output levels generally dependent on V_{CC+} and V_{EE-}.
- A comparator is designed for very low input currents despite large differential input voltage. It has buffers at each input before the differential high-gain. An op amp can also be used as a comparator with due consideration for finite differential input voltage.

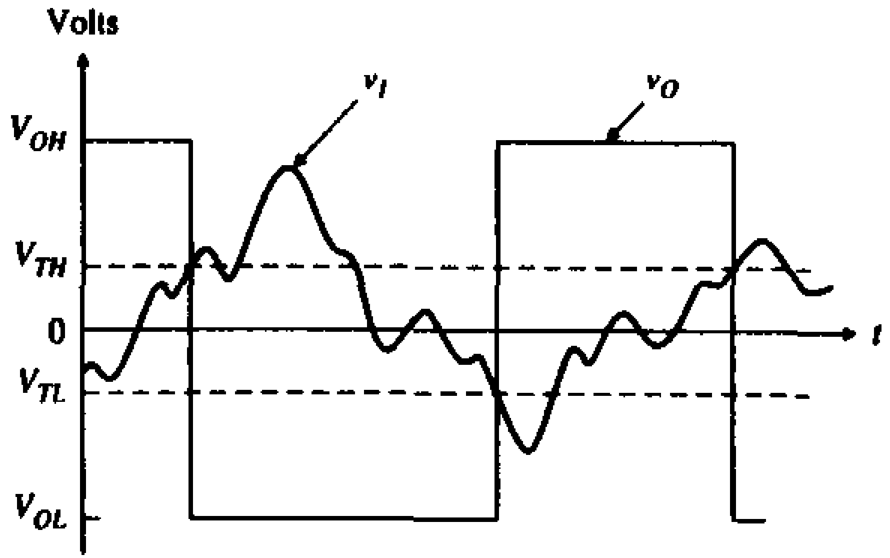
Schmitt Trigger

Comparator with hysteresis: high-gain differential amplifier with +ve feedback. Bistable circuit.

- Inverting Schmitt trigger: clockwise hysteresis.

- Non-inverting Schmitt trigger: counterclockwise hysteresis.





Applications: **Chatter elimination, waveform generation, signal processing.**