Name: _____ **Roll No.:** _____

Signature: _____ **EE103: 2022-2023/I (Autumn)**

Quiz-2 Digital Electronics SOLUTION

December 05. 2022. (Monday) **Marks: 10** **Time: 5:30 PM- 6:00 PM**

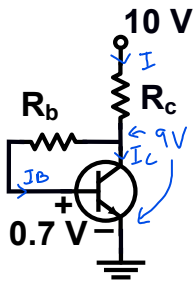
1. The output expression for the K map shown in figure is _____. **(1 Mark)**

RS \ PQ	00	01	11	10
00		1	1	
01	1	1	1	1
11	1	1	1	1
10			1	1

0.5

$F = S + Q\bar{R} + PR$ 0.5

2. In the circuit shown below β = 99 and V_{CE} = 9 V. Determine the ratio $\frac{R_b}{R_c}$. **(1 Mark)**



$I_c = I - I_B = \beta I_B$

$I = (\beta+1) I_B$ — (5)

substitute (3) & (4) in (5)

$\frac{1}{R_c} = \frac{(99+1)\times 8.3}{R_B}$

$\frac{R_b}{R_c} = 830$ ← 0.5

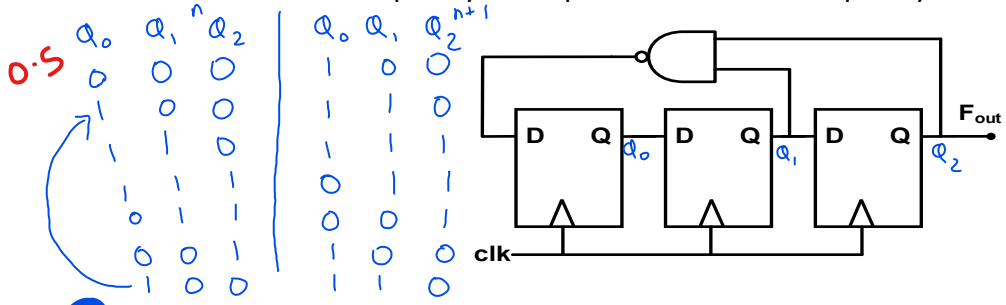
$I = I_c + I_B$ — (1)

$I_c = \beta I_B$ — (2) 0.5

$10 - R_c I = 9 \Rightarrow I = \frac{1}{R_c}$ — (3)

$9 - R_b I_B - 0.7 = 0 \Rightarrow I_B = \frac{8.3}{R_B}$ — (4)

3. Assume that all the outputs are cleared prior to occurrence of first rising edge of the clock determine the ratio of F_{out}/F_{Clk}.
Where F_{out} is the frequency of output and F_{Clk} is the frequency of the clock. **(1 Mark)**



Q_0	Q_1	Q_2	Q_2^{n+1}
0	0	0	1
1	0	0	0
0	1	0	1
1	1	0	1
0	1	1	1
1	1	1	0
0	0	1	1
1	0	1	0
0	0	0	1
1	0	0	0

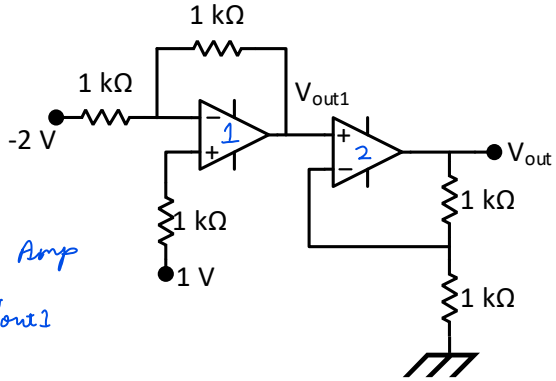
0.5

This is a MOD 5 counter

$\therefore \frac{F_{out}}{F_{clk}} = \frac{1}{5}$ ← 0.5

4. The OPAMP shown in the figure are ideal and they are suitably biased. Determine the following

A. V_{out1}. B. V_{out}. **(2 Marks)**



$V_{1+} = 1V \Rightarrow V_{1-} = 1V$

(1) $\therefore \frac{V_{out1} - 1}{1k} = \frac{1-(-2)}{1k}$

$V_{out1} = 4V$

OPAMP 2 is non inverting Amp

$\therefore V_{out} = \left(1 + \frac{1k}{1k}\right) V_{out1}$

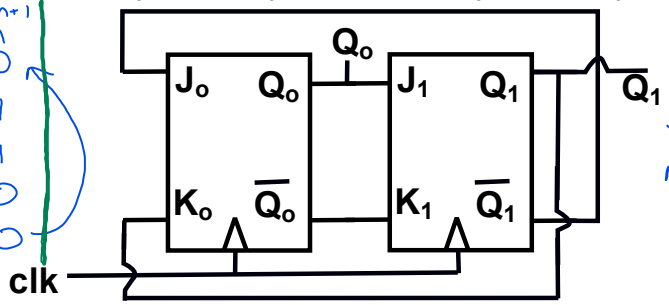
(1) $= 2 \times 4V$

$V_{out} = 8V$

5. In a sequential circuit, the initial state (before the 1st clock pulse) of the circuit is $Q_1Q_0 = 00$. Write down the truth table for the first five clock pulses and therefore what would be the state (Q_1Q_0) at the end of 33rd clock pulse. Note that $J_0 = \overline{Q_1},\ K_0 = Q_1,\ J_1 = Q_0,\ K_1 = \overline{Q_0}$. **(3.5 Marks)**

J_0^n	K_0^n	Q_0^n	J_1^n	K_1^n	Q_1^n	Q_0^{n+1}	Q_1^{n+1}
1	0	0	0	1	0	1	0
1	0	1	1	0	0	1	1
0	1	1	1	0	1	0	1
0	1	0	0	1	1	0	0
1	0	0	0	1	0	1	0

MOD 4 counter

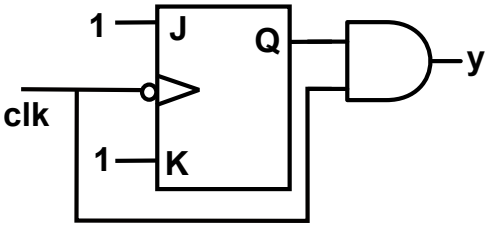


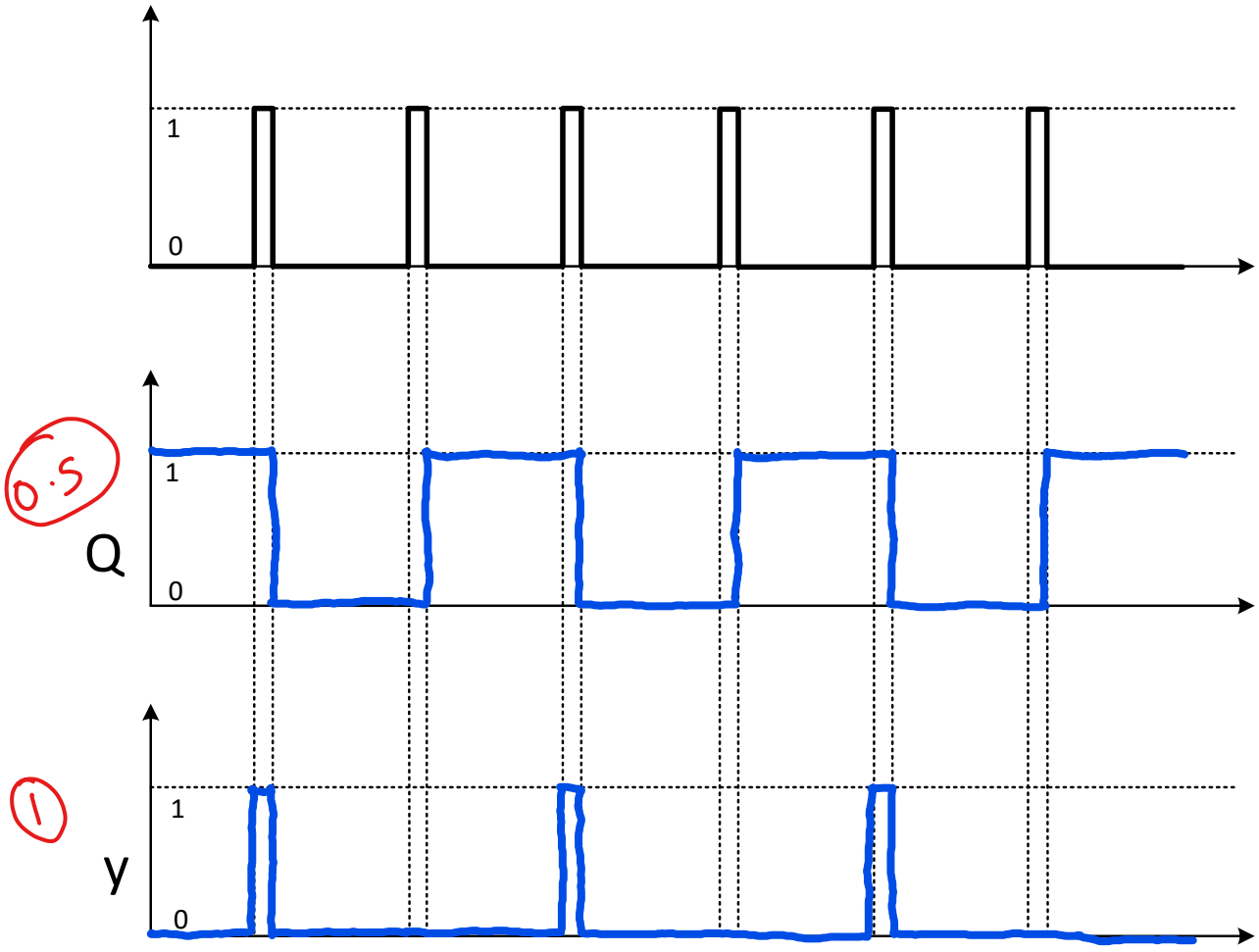
at the end of 33rd clock pulse it would be at MOD$\left(\frac{33}{4}\right)$ = 1st state 0.5

$\therefore Q_1 Q_0 = 01$

3

6. The digital circuit shown in figure generates a modified clock pulse at the output 'y'. Draw the output waveform on the graph provided to you below. Assume initial Q=1. **(1.5 Marks)**





0.5

1