

# EEI 03 Lecture 3 Notes

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# Lecture 3A: Diode Circuits

EE 103

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# Summary of Topics for Lect 3

- **Lect 3A – Rectifier and Regulator Circuits**

- Part1: Rectifier circuits: Half-wave rectifier, Full-wave rectifier (Bridge rectifier)
- Part 2: Unregulated DC Power Supply
- Part 3: Regulator DC Power Supply (Voltage Regulator: IC based regulated DC Power Supply)

# Part 1: Rectifier Circuits

# Part 1: Rectifier Circuits

- Half-Wave Rectifier
- Full-wave Rectifier
  - Bridge rectifier circuit

# Step Down Transformer (230 V - 12 V RMS)

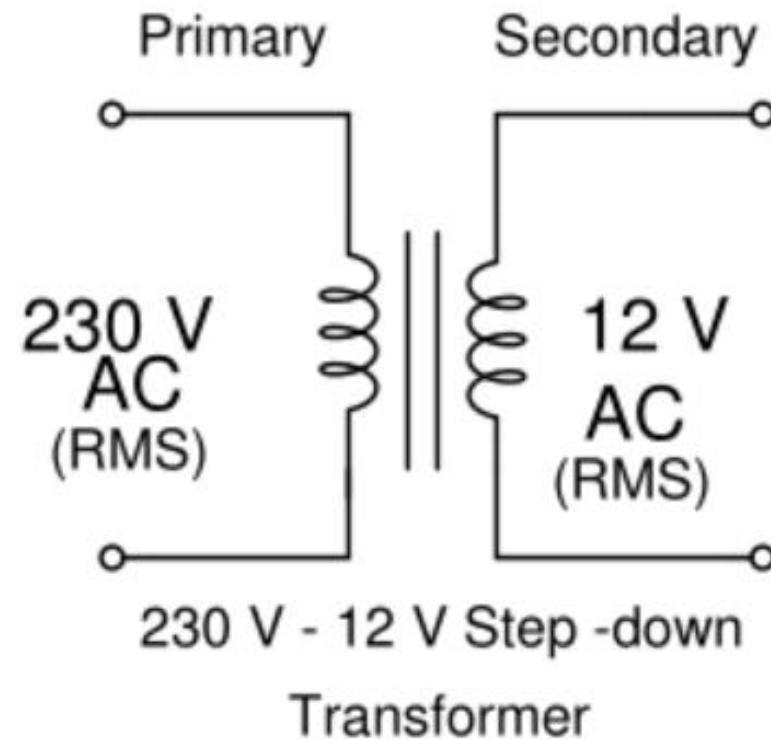


Fig. 1 Step-down Transformer

# A) Half-wave Rectifier

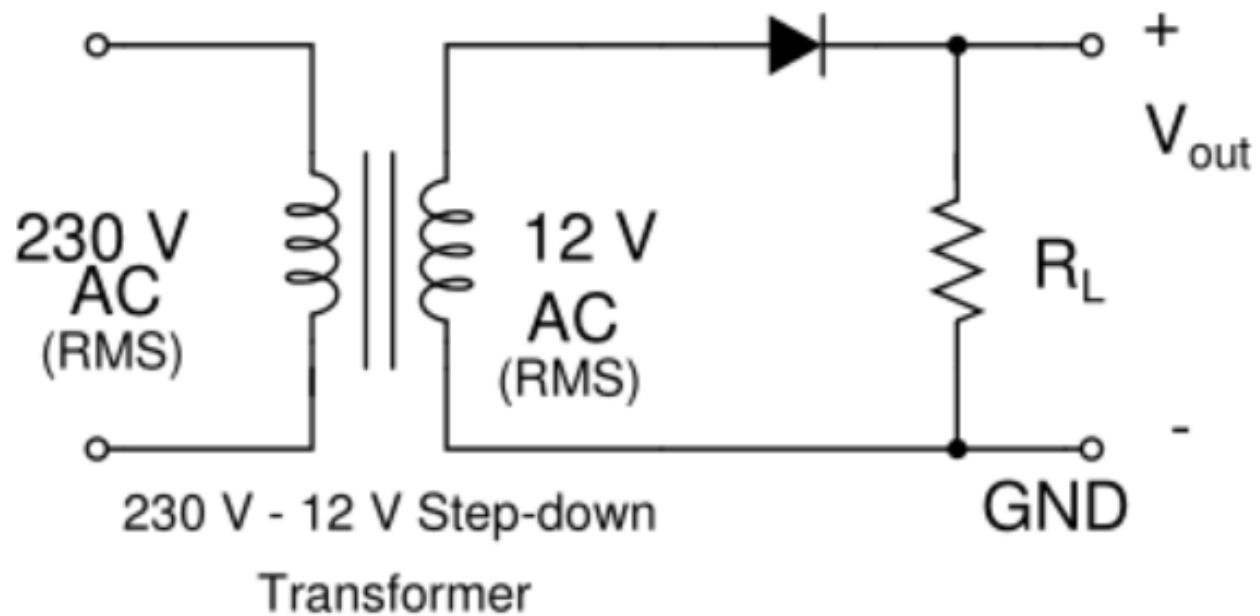
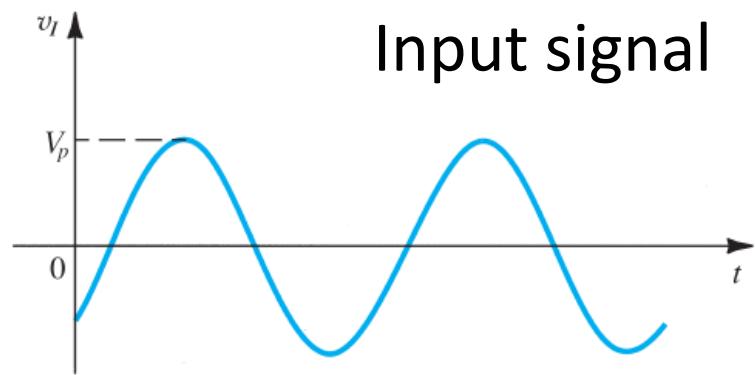


Fig. 2



Half-wave Rectifier Output

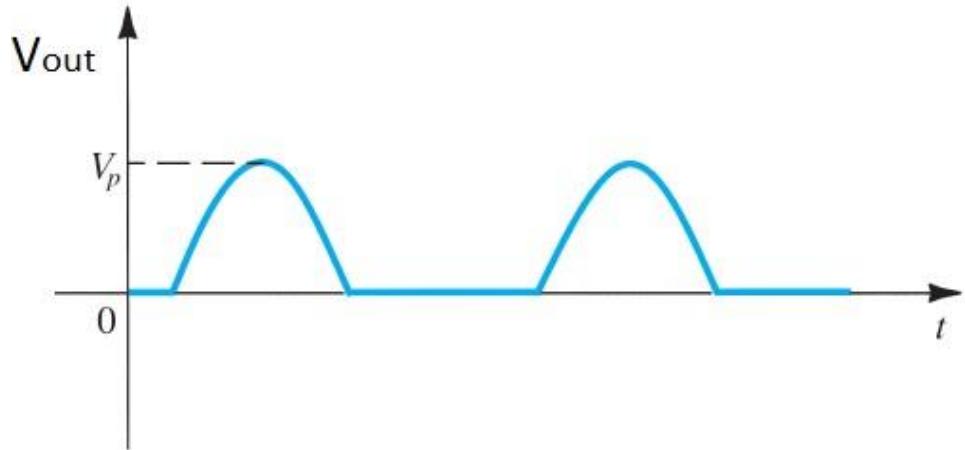


Fig. 3

## B) Full-wave (Bridge) Rectifier

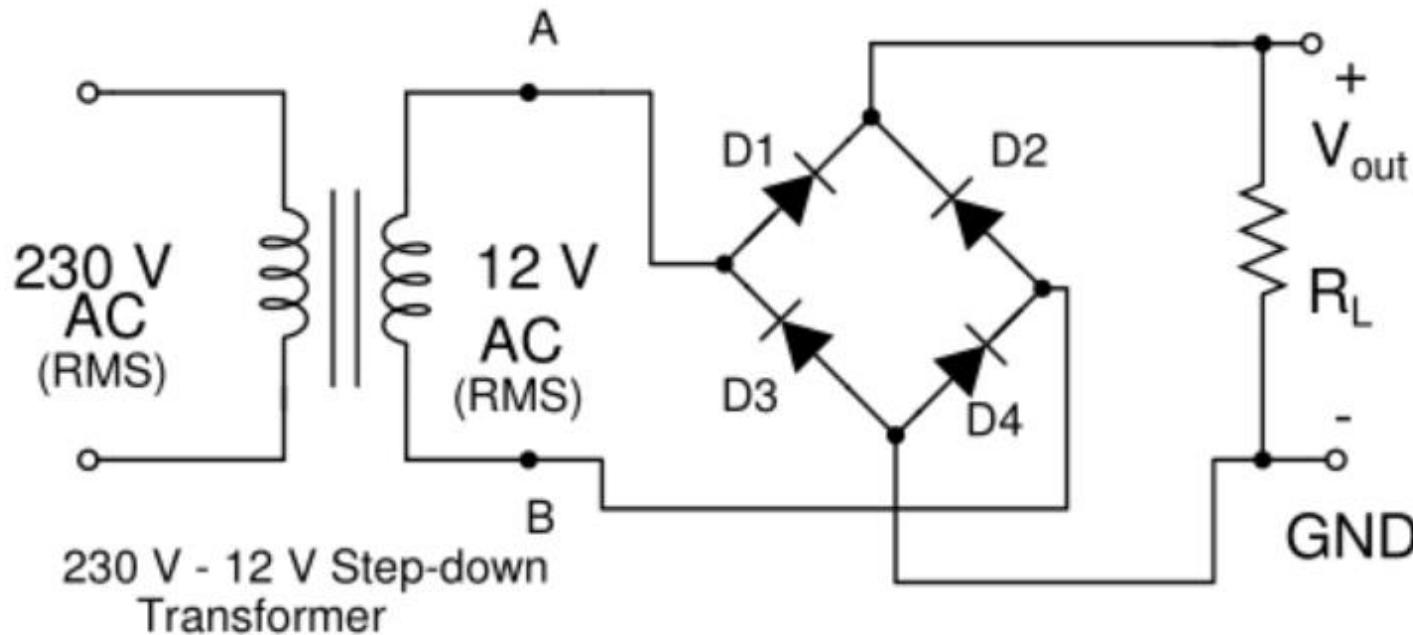
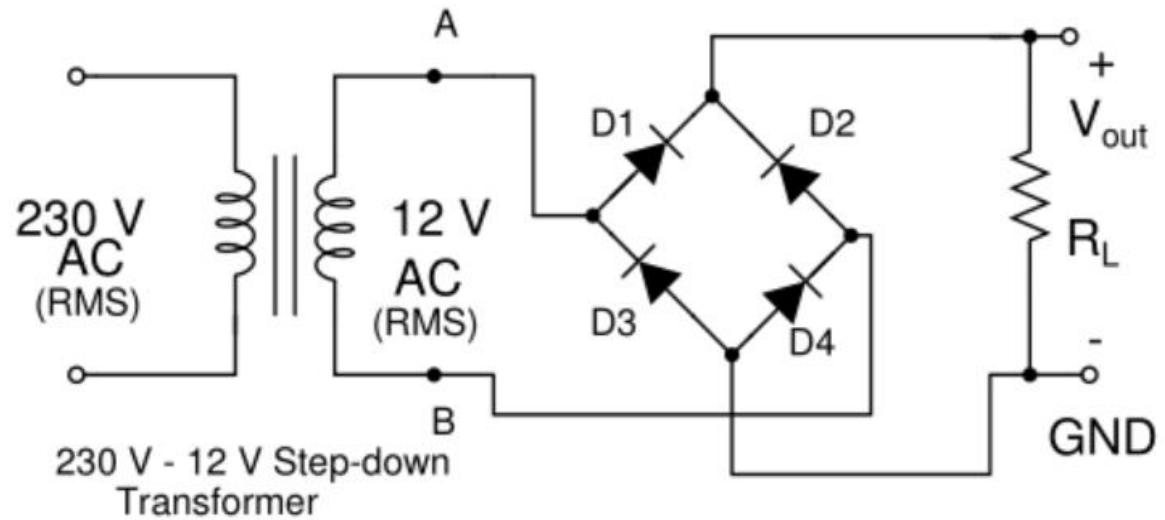
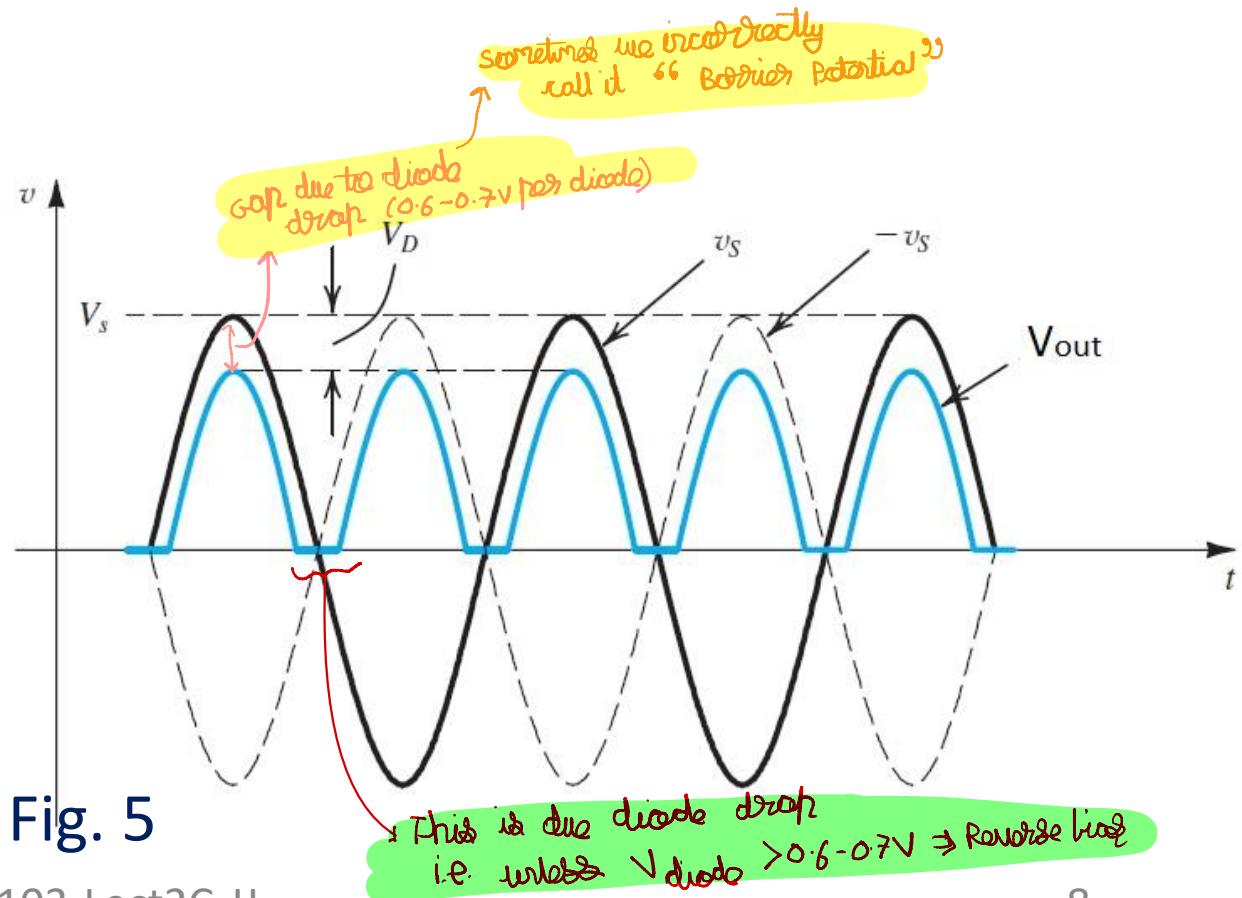


Fig. 4

- Bridge Rectifier: in every half cycle, two diodes will be in the current path



- 1<sup>st</sup> half cycle (output A is +ve w.r.t. Output B): current path – from output A  $\rightarrow$  D1  $\rightarrow$   $R_L$   $\rightarrow$  D4  $\rightarrow$  B; D2 and D3 will not conduct.
- 2<sup>nd</sup> half cycle (Output B is +ve w.r.t. output A): current path – from B  $\rightarrow$  D2  $\rightarrow$   $R_L$   $\rightarrow$  D3  $\rightarrow$  A; D1 and D4 will not conduct.



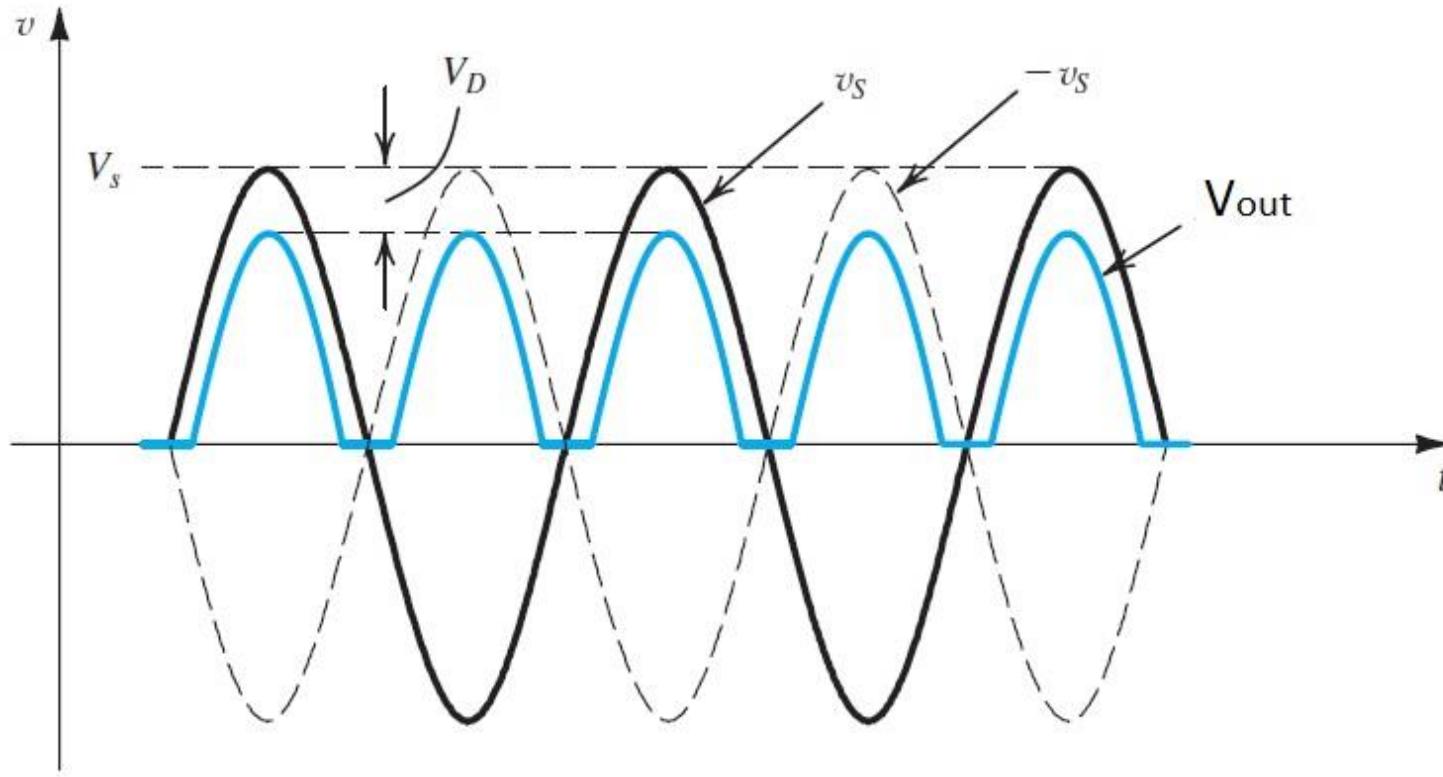


Fig. 6

- Full-wave Rectifier: Input and Output waveforms (considering diode drops)
- Output voltage will have the *two diode drops* lower than the input voltage. Typ. diode drop = 0.6 V

# Part 2: Unregulated Power Supply (Capacitive filter)

- There are two types of regulation:

- a) Load Regulation  $\Rightarrow$  Irrespective of  $R_{load}$  (i.e. load current  $I_{load} = V_{out} / R_{load}$ )  $V_{out}$  should remain constant we choose
- b) Line regulation  $\Rightarrow$  irrespective of  $V_{in}$ ,  $V_{out}$  is constant

# Unregulated Power Supply (Using Half-wave Rectifier and a Capacitive filter)

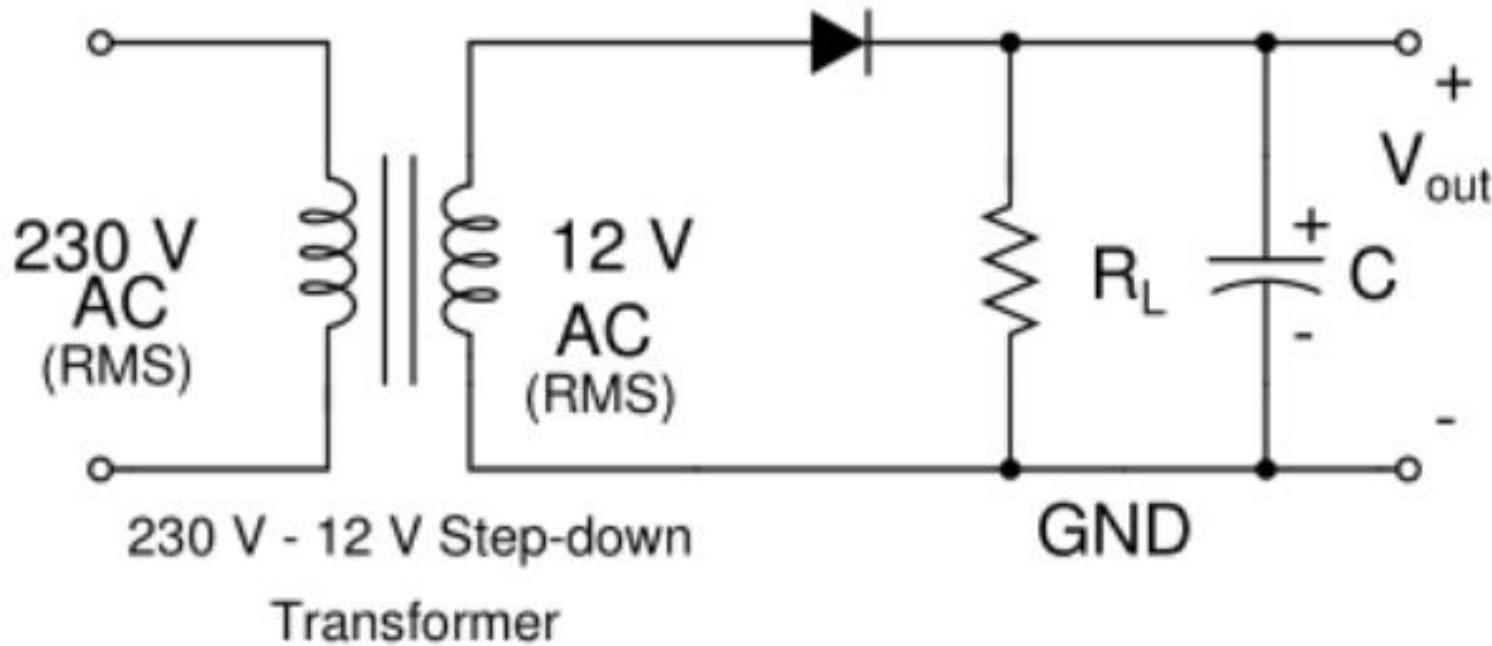
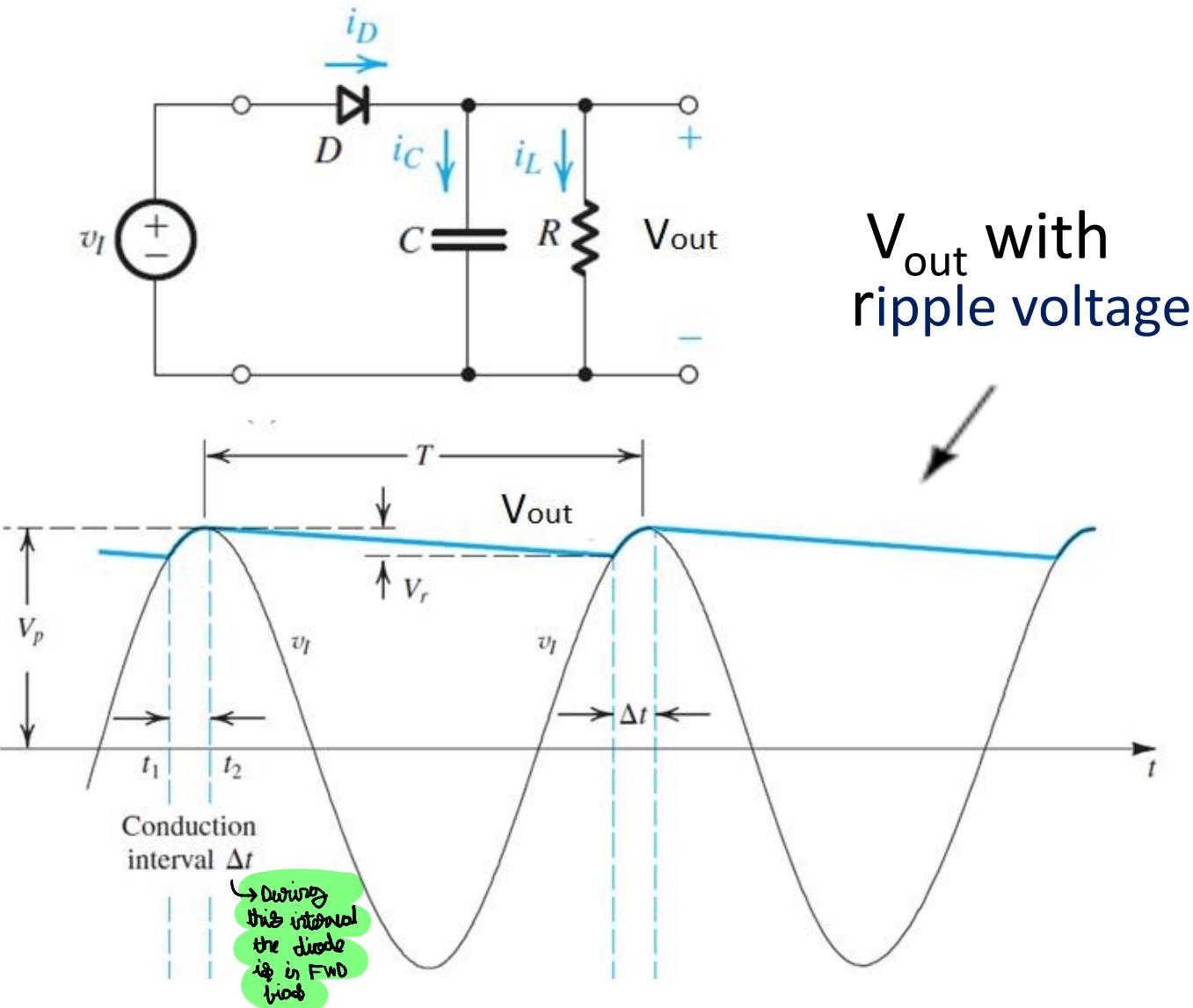


Fig. 7



- The half-wave rectifier with C is very seldom used due to its higher ripple voltage

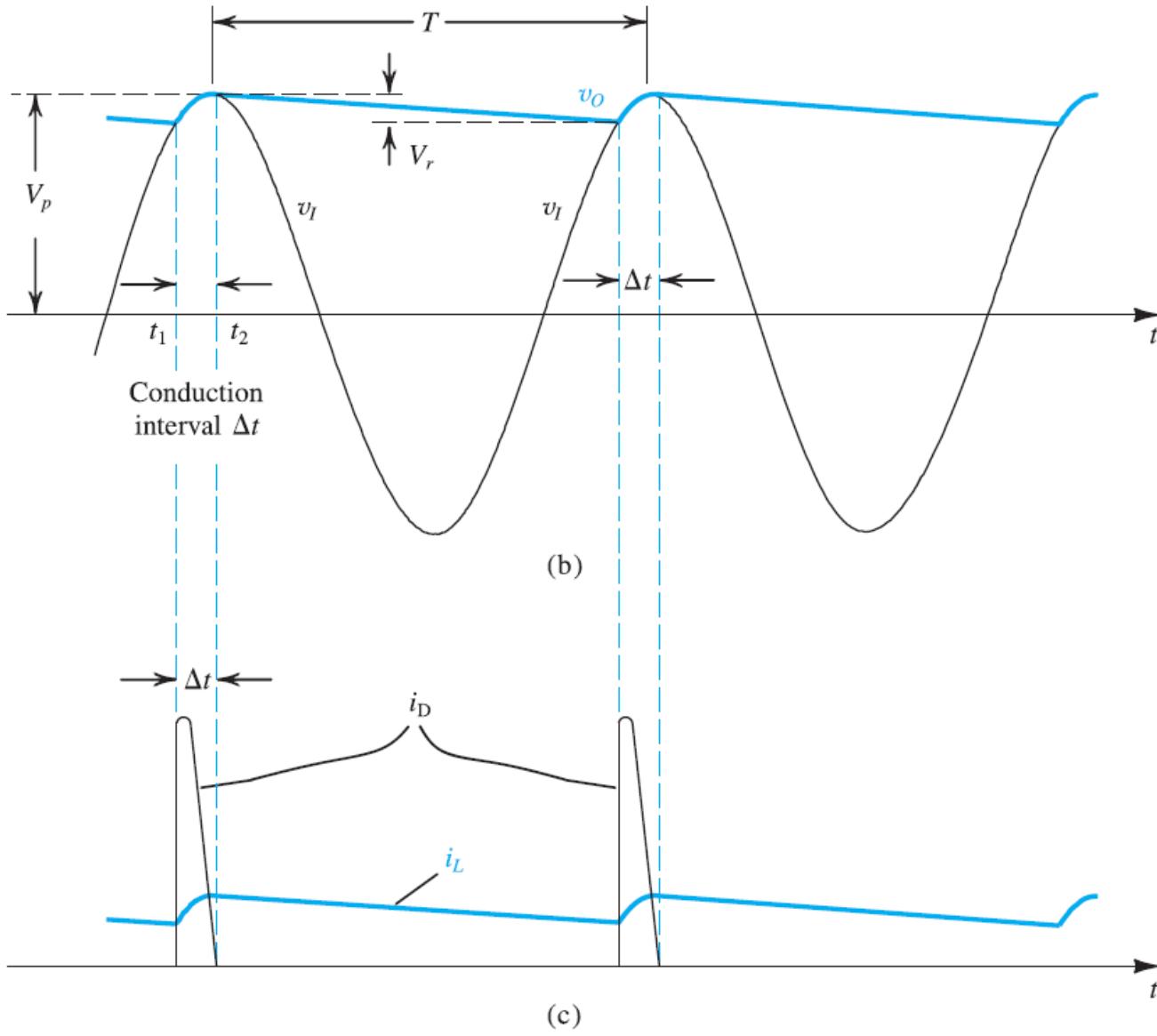
## Operation with C across $R_L$

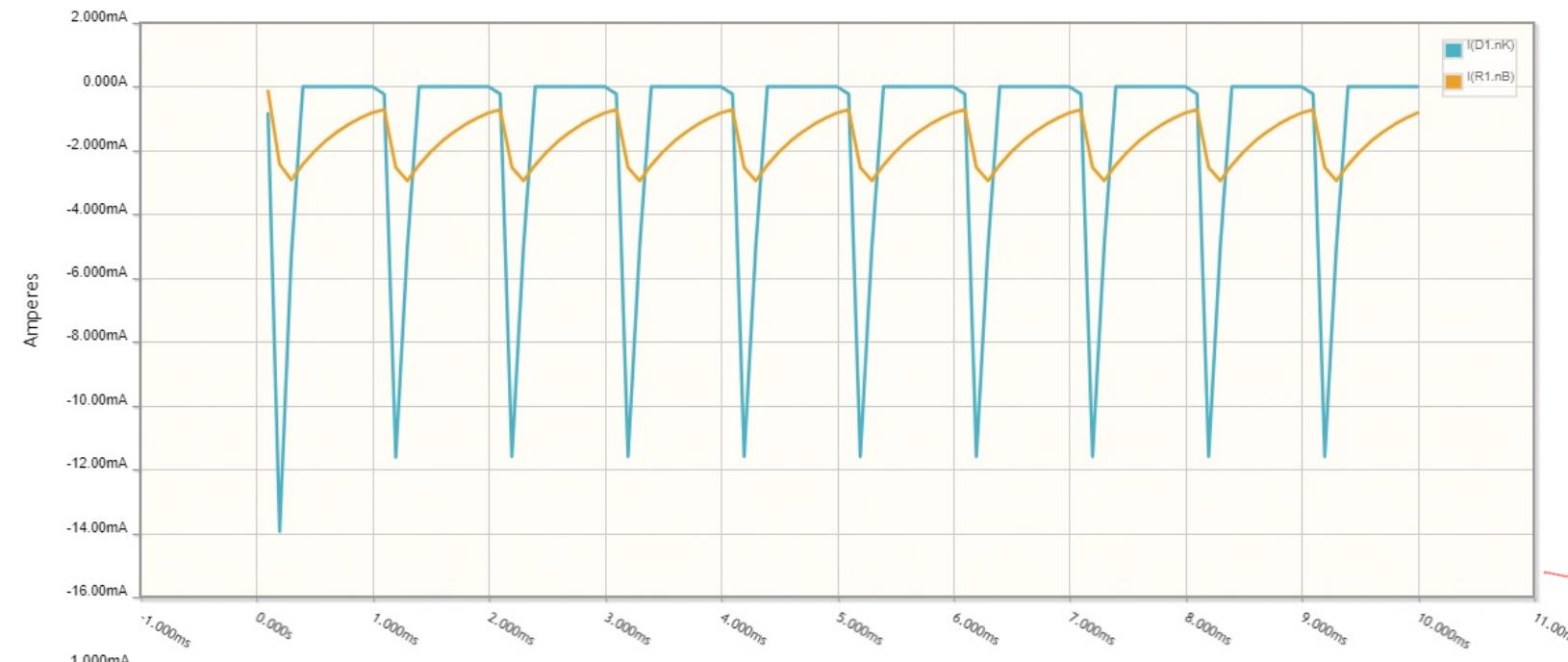
- $C$  charges during  $\Delta_t$ , and discharges during  $(T - \Delta_t)$ .
- Ripple voltage,  $V_r$ , increases with  $i_L$  (load current).
- Ripple voltage can be decreased by increasing  $C$  (not a good solution).
- For a given  $i_L$ , as  $C \uparrow$ ,  $\Delta_t \downarrow$  (which will make  $i_D \uparrow\uparrow$ )

Fig. 9

## Operation with C across $R_L$

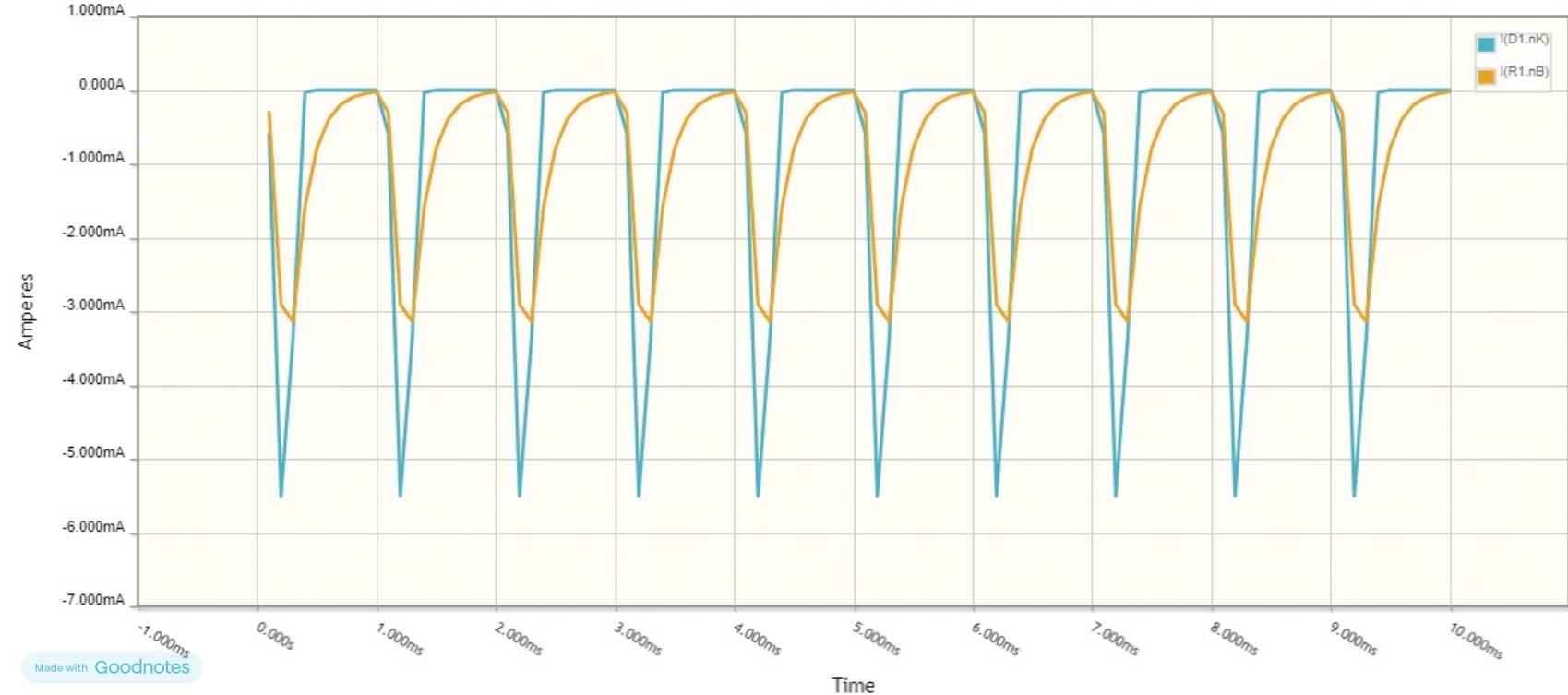
- C charges during  $\Delta_t$ , and discharges during  $(T - \Delta_t)$ .
- Ripple voltage,  $V_r$ , increases with  $i_L$  (load current).
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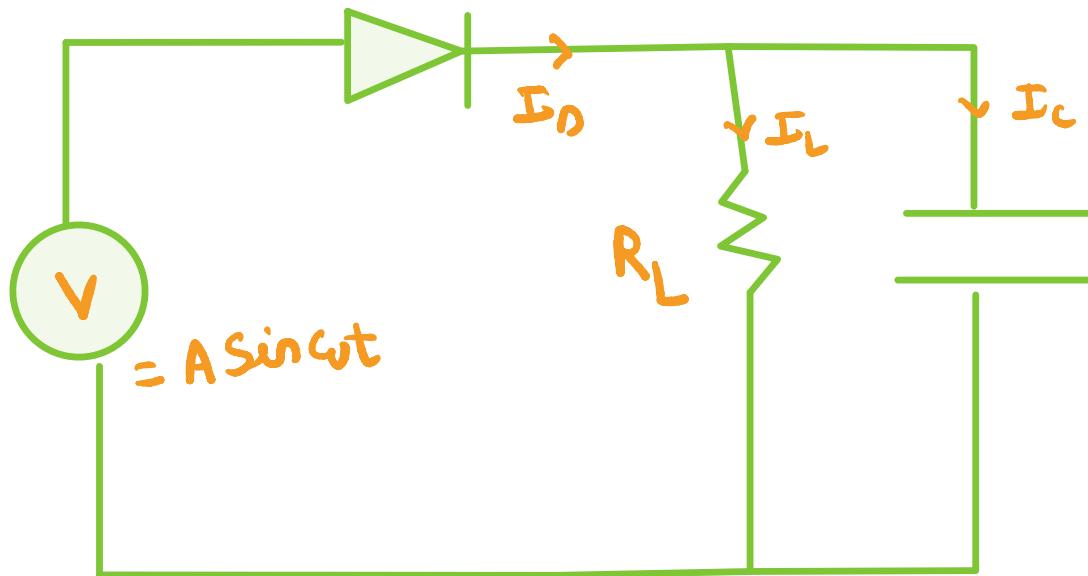
capacitor =  $5 \mu F$

- ↑ A & C ↑  $I_{diode} = \uparrow$
- $P_{diode} = \uparrow$
- diode burns out  
or increasing  
capacitance



capacitor =  $1 \mu F$

But why?



Assuming ideal diode,

$$V_R = A \sin \omega t$$

$$\therefore I_L = \frac{A \sin \omega t}{R}$$

$$V_C = A \sin \omega t$$

$$Q = CA \sin \omega t$$

$$I_C = CA\omega \cos \omega t$$

Till +ve Half Cycle

After  $t = \frac{\pi}{2}$  i.e.  $V_{IN} = \text{max}$  :  $V_{cap} > V_{IN}$   
 $\therefore$  Diode in reverse bias

$$\therefore V_R = V_C = V_0 e^{-\frac{t}{\tau}}$$

This will continue till  $V_0 e^{-t/\tau} > A \sin \omega t \Rightarrow$  After this Again capacitor will charge.

During discharging  
During charging

$$I_D = 0$$

$$I_D = CA\omega \cos \omega t + \frac{A \sin \omega t}{R}$$

$\therefore I_D$  increases with increase in  $C$

# Unregulated Power Supply

(Using Full-wave Bridge Rectifier and a Capacitive filter)

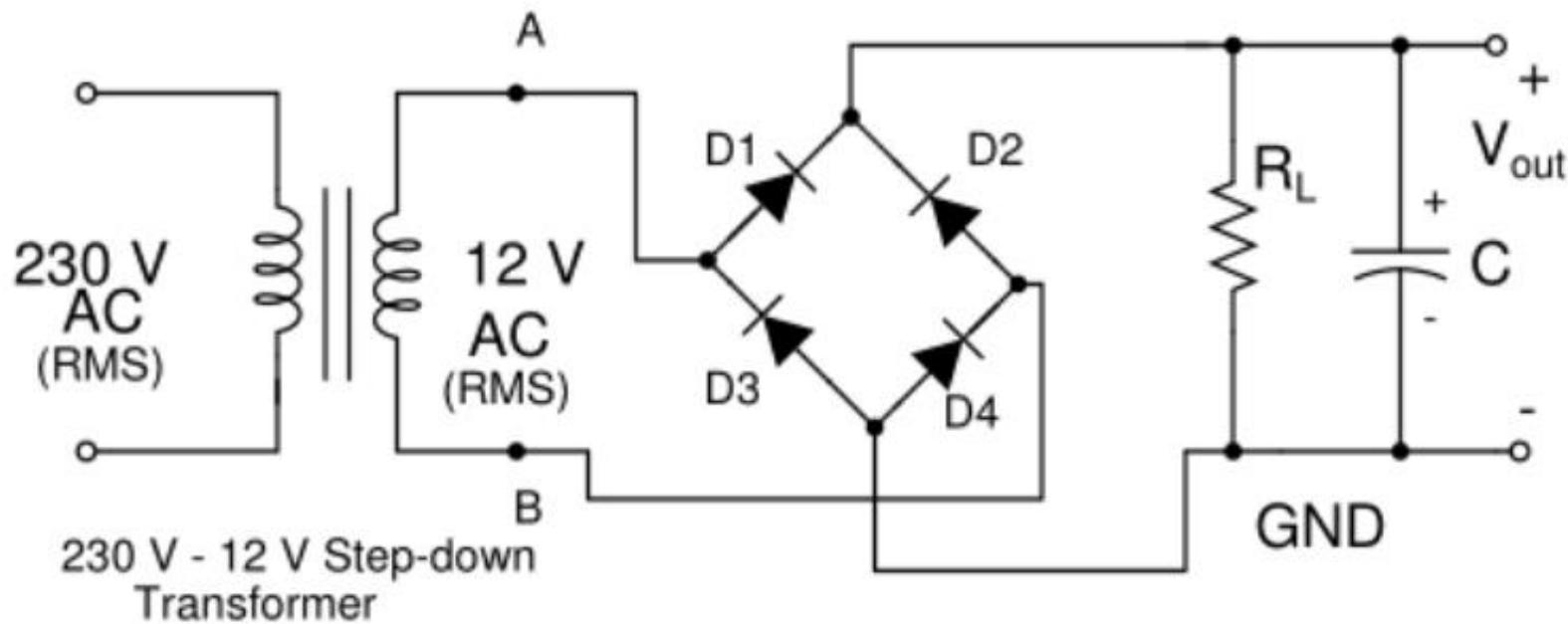


Fig. 10

- Much better than the half-wave (HW) rectifier
  - For the same  $C$  and  $R_L$ , peak-to-peak ripple voltage gets reduced to half that of HW

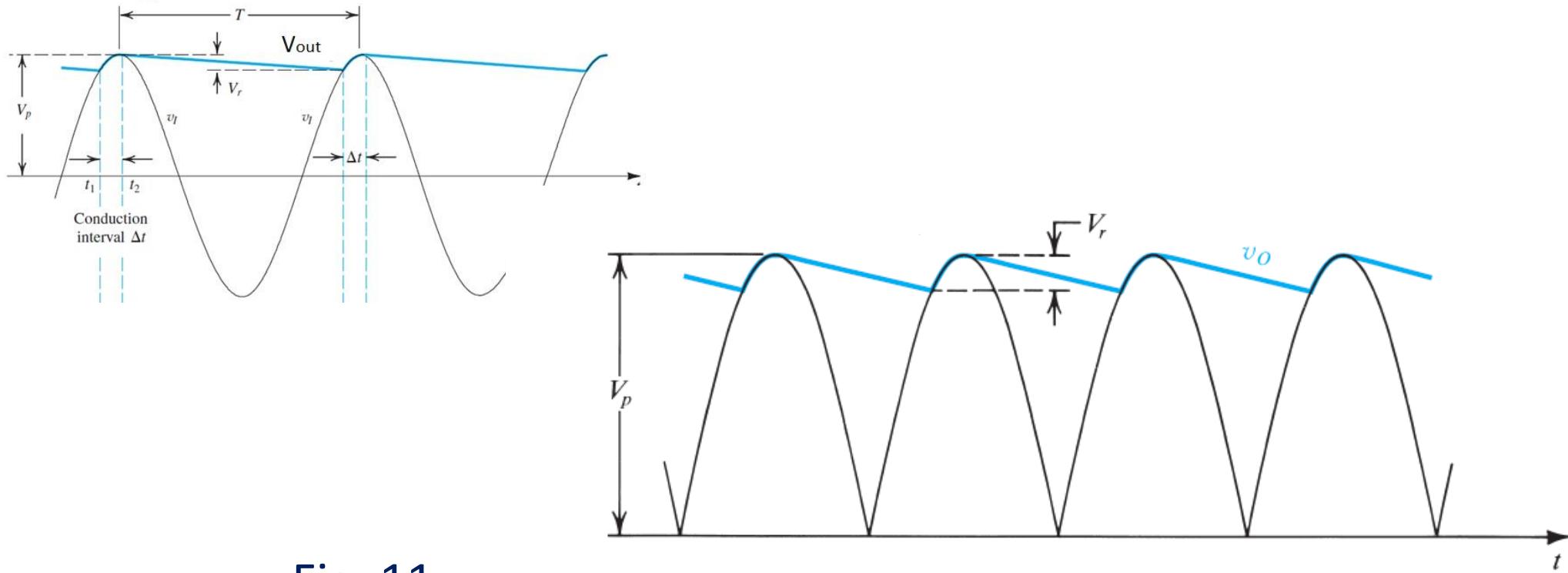


Fig. 11

- Full-wave rectifier output waveform (blue)
- Less Ripple voltage, compared to the Half-wave rectifier circuit
  - Discharge interval for C almost half that of HW case)

# Problems of Unregulated Power Supply

- Output voltage fluctuates
  - When ac input voltage fluctuates
  - When load current fluctuates
- Ripple voltage increases with load current
  - Ripple voltage for a given load current ( $i_L$ ) can be reduced only by increasing  $C$
  - Increasing  $C$  beyond a certain value can cause diode damages (as the peak diode current will always be many times the average load current)

# Part 3: Regulated DC Power Supply

# Regulated Power Supply

- **Problems of the unregulated power supply**
  - Output voltage fluctuates with the input voltage (for a given load current) - Line regulation
  - Output voltage fluctuates for load current (for a given input voltage) - Load regulation
- **Regulated Power Supply**
  - Output voltage stays constant (reasonably well):
    - For varying input voltages
    - For varying load currents

# Two solutions

- Solution 1
  - Zener diode regulator circuit
- Solution 2
  - Voltage Regulator IC

# Solution 1: Zener Regulator Circuit

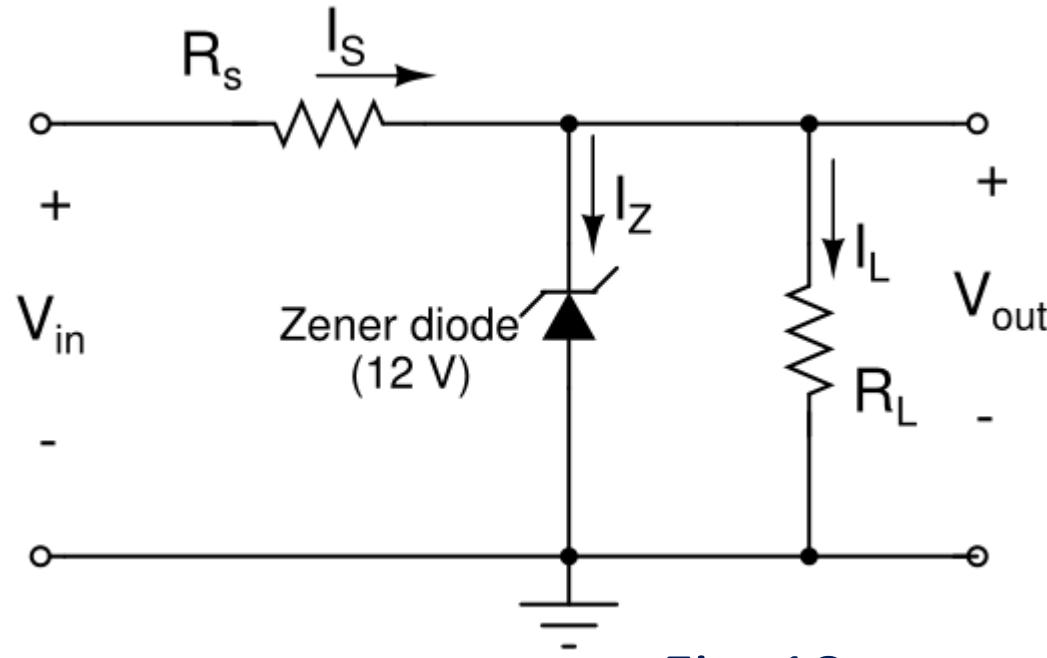
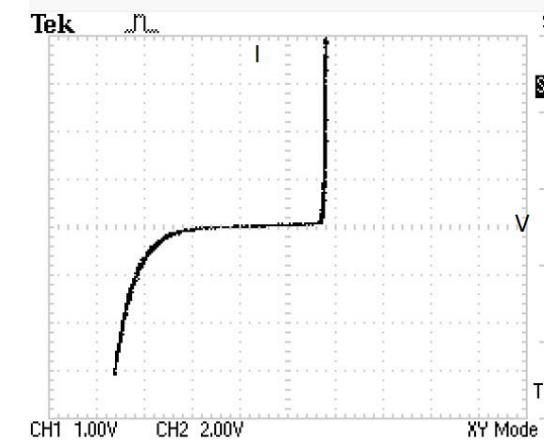
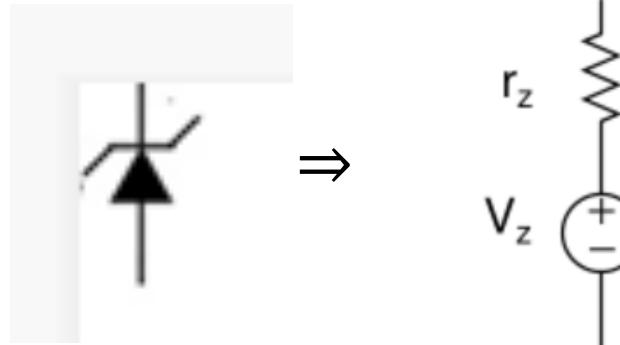


Fig. 18

## Problem statement:

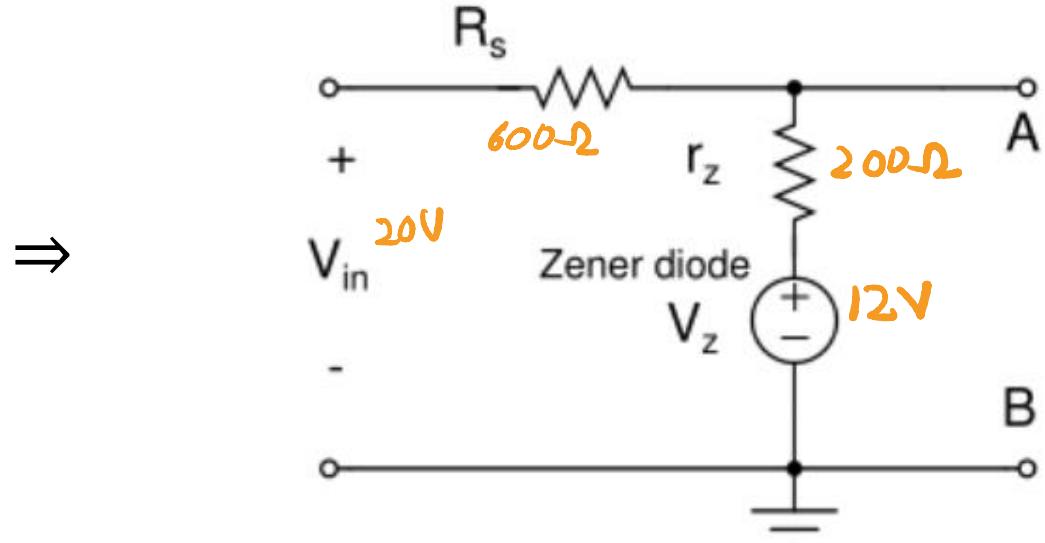
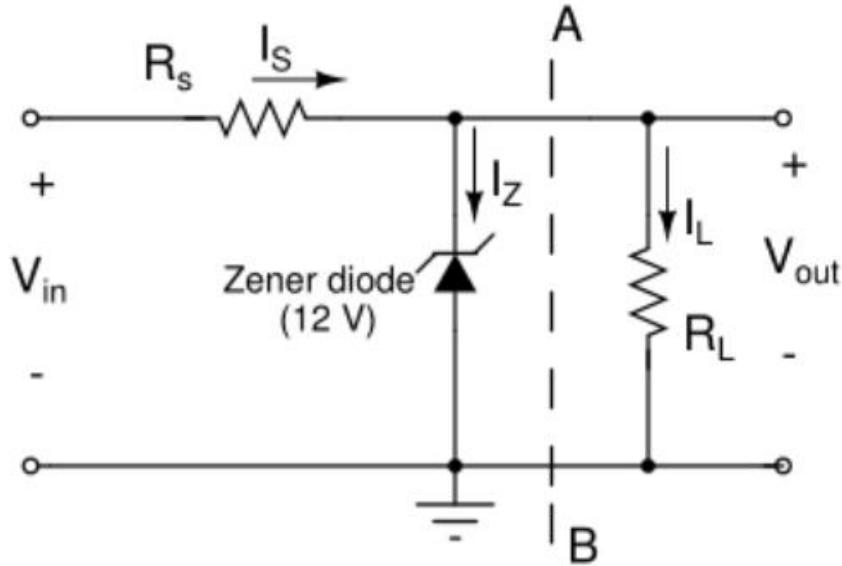
In the Zener regulator circuit shown,  $V_{in} = 20 \text{ V}$ ,  $R_s = 600 \Omega$ ,  $R_L = 1 \text{ k}\Omega$ . Find out the regulator output voltage  $V_{out}$  and the load current  $I_L$ .

Zener parameters:  $V_z = 12 \text{ V}$ ,  $r_z = 200 \Omega$



## Solution:

- In the circuit, the zener diode is reverse biased and operating as a zener.
- We will use a simple model for the zener diode (zener diode voltage ( $V_z$ ) and a series resistor  $r_z$ ).
- Replace the zener with the equivalent circuit.
- Apply Thevenin's theorem.



Find  $V_{Th}$  and  $R_{Th}$  of this circuit across AB

Putting  $V_{in} = 20 \text{ V}$ ,  $R_s = 600 \Omega$ ,

$V_z = 12 \text{ V}$ ,  $r_z = 200 \Omega$ , we get

$$V_{Th}(V_{AB}) = 14 \text{ V}; R_{Th} (= R_s || r_z) = 150 \Omega$$

$$R_L = 1 \text{ k}\Omega$$

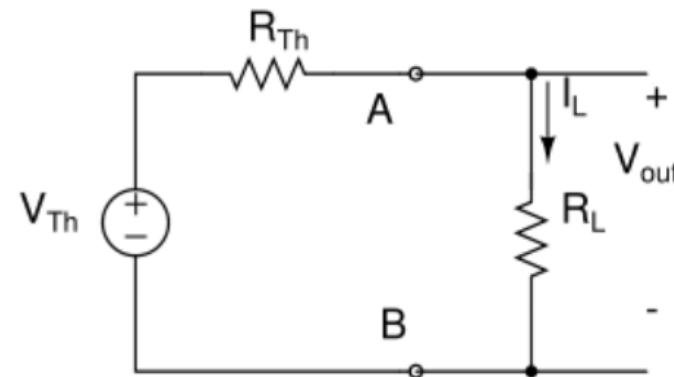
Now?

Substituting  
and evaluating,

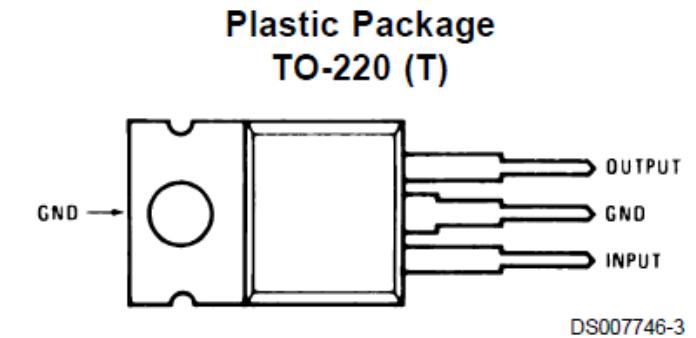
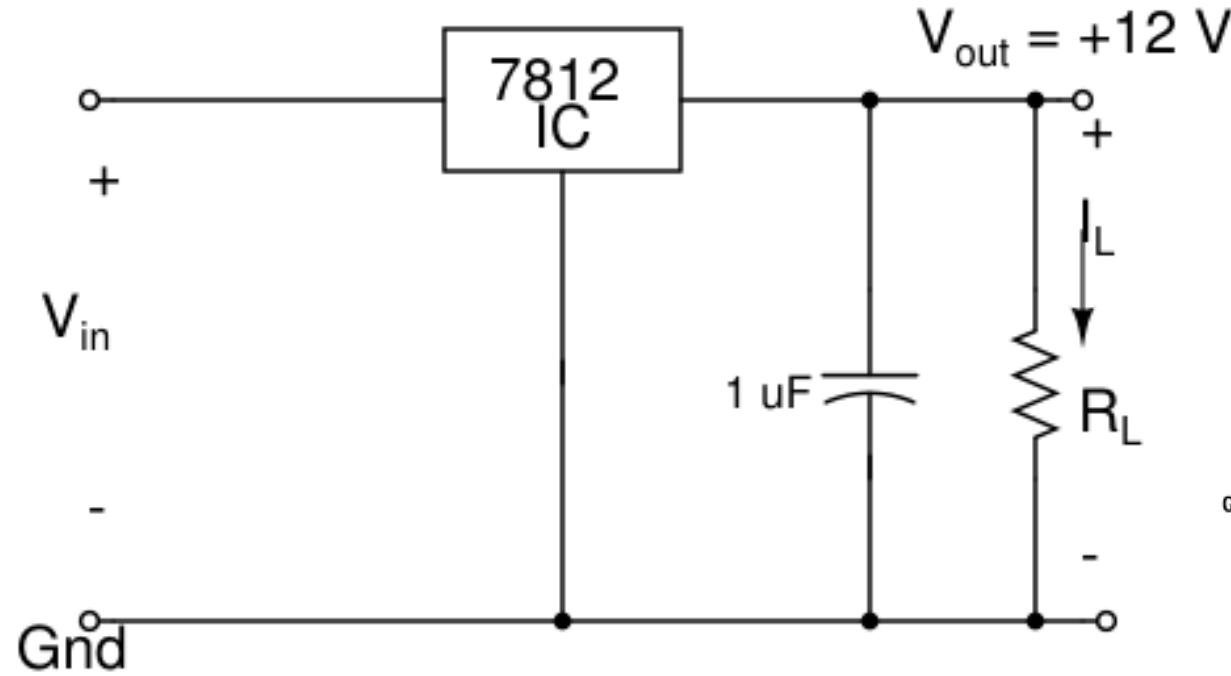
$$V_{out} = 12.17 \text{ V}$$

$$I_L = 12.17 \text{ mA}$$

$\therefore$  For 20V input  
caused only 0.17V change



# 3B: 7812 Three-terminal Voltage Regulator



DS007746-3

Fig. 12

$V_{in} : +14.5 \text{ to } 30 \text{ V}$ ,  $V_{out} : 11.5 \text{ to } 12.5 \text{ V}$

$I_L = \text{up to } 1 \text{ A}$

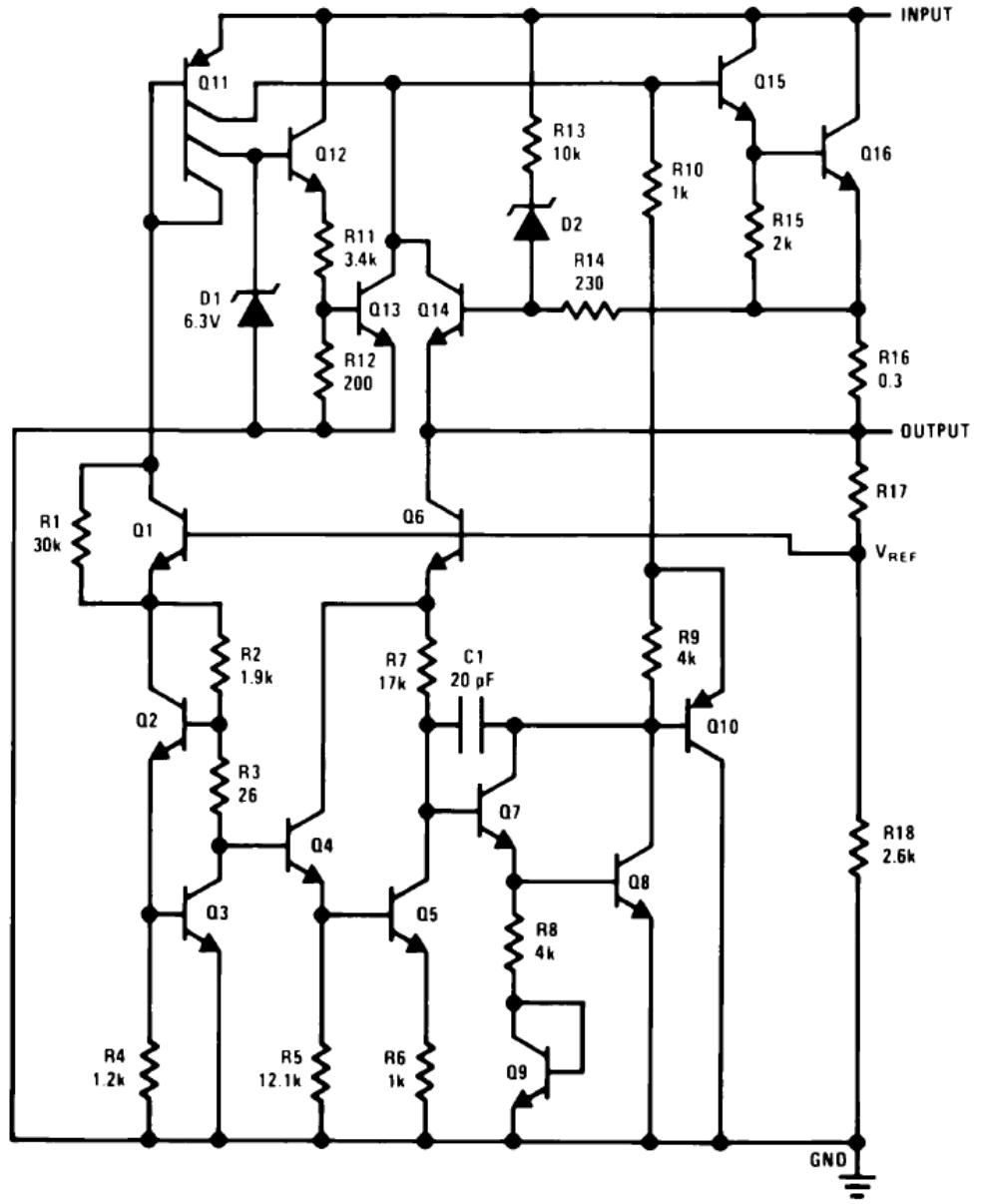


Fig. 13

## Major blocks of the 7812 Voltage Regulator IC:

- Series-pass transistor (Q16)
- Stable Zener reference voltage
- Error amplifier
- Short-circuit protection

Source: 7812 Data sheet, National Semiconductor Corp., 2000

DS007746-1

# Features of an IC Regulator

- $V_{out}$  will be steady for a large range of  $V_{in}$  and  $I_L$  values
- Minimum  $V_{in}$  to the IC regulator:  $V_{out} + 2$  or  $3$  V (typical)
- A small value of capacitor, typically  $1 \mu\text{F}$  is put at the output for stability (i.e. to prevent oscillations)
  - The regulator IC uses a negative feedback error amplifier circuit, which could result in instability.

# Other Popular Three-terminal Voltage Regulator ICs

- Positive Voltage Regulator ICs

1. 7805 :  $V_{out} = 5 \text{ V}$
2. 7806 :  $V_{out} = 6 \text{ V}$
3. 7809 :  $V_{out} = 9 \text{ V}$

- Negative Voltage Regulator ICs

1. 7905 :  $V_{out} = -5 \text{ V}$
2. 7906 :  $V_{out} = -6 \text{ V}$
3. 7909 :  $V_{out} = -9 \text{ V}$
4. 7912 :  $V_{out} = -12 \text{ V}$

is to connect a zener diode with a positive temperature coefficient of about  $2 \text{ mV}/^\circ\text{C}$  in series with a forward-conducting diode. Since the forward-conducting diode has a voltage drop of  $\approx 0.7 \text{ V}$  and a TC of about  $-2 \text{ mV}/^\circ\text{C}$ , the series combination will provide a voltage of  $(V_Z + 0.7)$  with a TC of about zero.

### EXERCISES

- 4.16** A zener diode whose nominal voltage is 10 V at 10 mA has an incremental resistance of  $50 \Omega$ . What voltage do you expect if the diode current is halved? Doubled? What is the value of  $V_{Z_0}$  in the zener model?

**Ans.** 9.75 V; 10.5 V; 9.5 V

$$\begin{aligned} & \left. \begin{aligned} & \frac{10\text{mA}}{50\Omega} \\ & 10\Omega = V_{Z,T} \end{aligned} \right\} V_Z = V_{Z_0} + I_D R \\ & \frac{10\text{mA}}{100\Omega} = 9.5\text{mV} \quad \boxed{V_Z = V_{Z_0} + I_D R} \end{aligned}$$

- 4.17** A zener diode exhibits a constant voltage of 5.6 V for currents greater than five times the knee current.  $I_{ZK}$  is specified to be 1 mA. The zener is to be used in the design of a shunt regulator fed from a 15-V supply. The load current varies over the range of 0 mA to 15 mA. Find a suitable value for the resistor  $R$ . What is the maximum power dissipation of the zener diode?

**Ans.**  $470 \Omega$ ; 112 mW

- 4.18** A shunt regulator utilizes a zener diode whose voltage is 5.1 V at a current of 50 mA and whose incremental resistance is  $7 \Omega$ . The diode is fed from a supply of 15-V nominal voltage through a  $200\Omega$  resistor. What is the output voltage at no load? Find the line regulation and the load regulation.

**Ans.** 5.1 V; 33.8 mV/V;  $-7 \text{ mV/mA}$

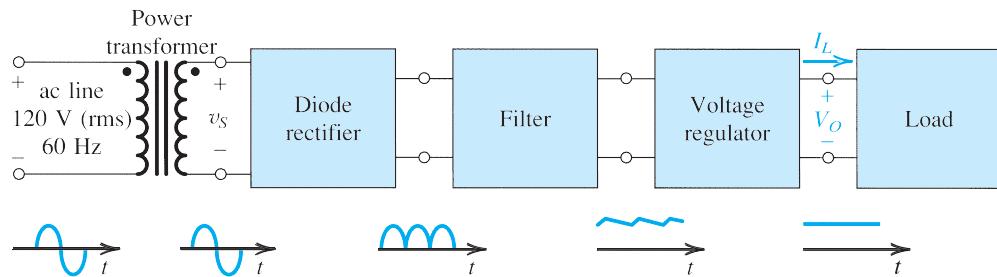
### 4.4.4 A Final Remark

Though simple and useful, zener diodes have lost a great deal of their popularity in recent years. They have been virtually replaced in voltage-regulator design by specially designed integrated circuits (ICs) that perform the voltage-regulation function much more effectively and with greater flexibility than zener diodes.

## 4.5 Rectifier Circuits

One of the most important applications of diodes is in the design of rectifier circuits. A diode rectifier forms an essential building block of the dc power supplies required to power electronic equipment. A block diagram of such a power supply is shown in Fig. 4.22. As indicated, the power supply is fed from the 120-V (rms) 60-Hz ac line, and it delivers a dc voltage  $V_O$  (usually in the range of 4 V to 20 V) to an electronic circuit represented by the *load* block. The dc voltage  $V_O$  is required to be as constant as possible in spite of variations in the ac line voltage and in the current drawn by the load.

The first block in a dc power supply is the **power transformer**. It consists of two separate coils wound around an iron core that magnetically couples the two windings. The **primary winding**, having  $N_1$  turns, is connected to the 120-V ac supply, and the **secondary winding**, having  $N_2$  turns, is connected to the circuit of the dc power supply. Thus an ac voltage  $v_s$  of  $120(N_2/N_1)$  V (rms) develops between the two terminals of the secondary winding. By



**Figure 4.22** Block diagram of a dc power supply.

selecting an appropriate turns ratio ( $N_1/N_2$ ) for the transformer, the designer can step the line voltage down to the value required to yield the particular dc voltage output of the supply. For instance, a secondary voltage of 8-V rms may be appropriate for a dc output of 5 V. This can be achieved with a 15:1 turns ratio.

In addition to providing the appropriate sinusoidal amplitude for the dc power supply, the power transformer provides electrical isolation between the electronic equipment and the power-line circuit. This isolation minimizes the risk of electric shock to the equipment user.

The diode rectifier converts the input sinusoid  $v_S$  to a unipolar output, which can have the pulsating waveform indicated in Fig. 4.22. Although this waveform has a nonzero average or a dc component, its pulsating nature makes it unsuitable as a dc source for electronic circuits, hence the need for a filter. The variations in the magnitude of the rectifier output are considerably reduced by the filter block in Fig. 4.22. In this section we shall study a number of rectifier circuits and a simple implementation of the output filter.

The output of the rectifier filter, though much more constant than without the filter, still contains a time-dependent component, known as **ripple**. To reduce the ripple and to stabilize the magnitude of the dc output voltage against variations caused by changes in load current, a voltage regulator is employed. Such a regulator can be implemented using the zener shunt regulator configuration studied in Section 4.4. Alternatively, and much more commonly at present, an integrated-circuit regulator can be used.

#### 4.5.1 The Half-Wave Rectifier

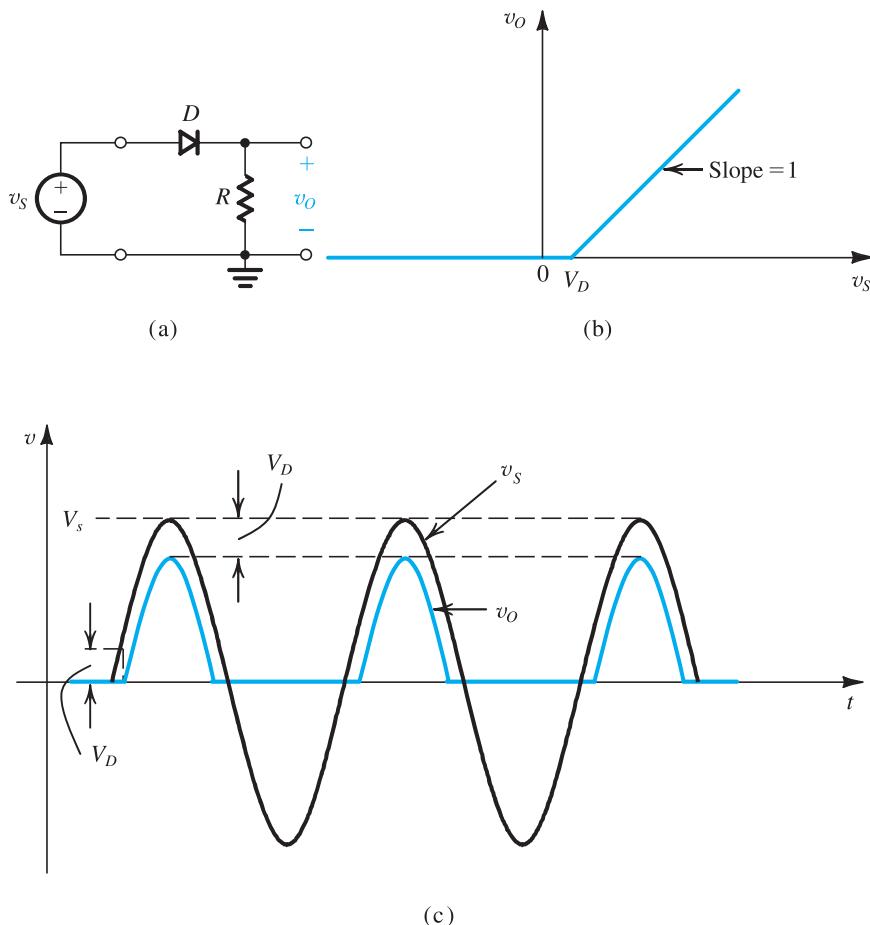
The half-wave rectifier utilizes alternate half-cycles of the input sinusoid. Figure 4.23(a) shows the circuit of a half-wave rectifier. This circuit was analyzed in Section 4.1 (see Fig. 4.3) assuming an ideal diode. Using the more realistic constant-voltage-drop diode model, we obtain

$$v_O = 0, \quad v_S < V_D \quad (4.21a)$$

$$v_O = v_S - V_D, \quad v_S \geq V_D \quad (4.21b)$$

The transfer characteristic represented by these equations is sketched in Fig. 4.23(b), where  $V_D = 0.7$  V or 0.8 V. Figure 4.23(c) shows the output voltage obtained when the input  $v_S$  is a sinusoid.

In selecting diodes for rectifier design, two important parameters must be specified: the current-handling capability required of the diode, determined by the largest current the diode is expected to conduct, and the **peak inverse voltage** (PIV) that the diode must be able to



**Figure 4.23** (a) Half-wave rectifier. (b) Transfer characteristic of the rectifier circuit. (c) Input and output waveforms.

withstand without breakdown, determined by the largest reverse voltage that is expected to appear across the diode. In the rectifier circuit of Fig. 4.23(a), we observe that when  $v_s$  is negative the diode will be cut off and  $v_o$  will be zero. It follows that the PIV is equal to the peak of  $v_s$ ,

$$\text{PIV} = V_s \quad (4.22)$$

It is usually prudent, however, to select a diode that has a reverse breakdown voltage at least 50% greater than the expected PIV.

Before leaving the half-wave rectifier, the reader should note two points. First, it is possible to use the diode exponential characteristic to determine the exact transfer characteristic of the rectifier (see Problem 4.68). However, the amount of work involved is usually too great to be justified in practice. Of course, such an analysis can be easily done using a computer circuit-analysis program such as SPICE.

Second, whether we analyze the circuit accurately or not, it should be obvious that this circuit does not function properly when the input signal is small. For instance, this circuit cannot be used to rectify an input sinusoid of 100-mV amplitude. For such an application one

resorts to a so-called precision rectifier, a circuit utilizing diodes in conjunction with op amps. One such circuit is presented in Section 4.5.5.

### EXERCISE

- 4.19** For the half-wave rectifier circuit in Fig. 4.23(a), show the following: (a) For the half-cycles during which the diode conducts, conduction begins at an angle  $\theta = \sin^{-1}(V_D/V_s)$  and terminates at  $(\pi - \theta)$ , for a total conduction angle of  $(\pi - 2\theta)$ . (b) The average value (dc component) of  $v_o$  is  $V_o \simeq (1/\pi)V_s - V_D/2$ . (c) The peak diode current is  $(V_s - V_D)/R$ .

Find numerical values for these quantities for the case of 12-V (rms) sinusoidal input,  $V_D \simeq 0.7$  V, and  $R = 100 \Omega$ . Also, give the value for PIV.

**Ans.** (a)  $\theta = 2.4^\circ$ , conduction angle =  $175^\circ$ ; (b) 5.05 V; (c) 163 mA; 17 V

### 4.5.2 The Full-Wave Rectifier

The full-wave rectifier utilizes both halves of the input sinusoid. To provide a unipolar output, it inverts the negative halves of the sine wave. One possible implementation is shown in Fig. 4.24(a). Here the transformer secondary winding is **center-tapped** to provide two equal voltages  $v_s$  across the two halves of the secondary winding with the polarities indicated. Note that when the input line voltage (feeding the primary) is positive, both of the signals labeled  $v_s$  will be positive. In this case  $D_1$  will conduct and  $D_2$  will be reverse biased. The current through  $D_1$  will flow through  $R$  and back to the center tap of the secondary. The circuit then behaves like a half-wave rectifier, and the output during the positive half-cycles when  $D_1$  conducts will be identical to that produced by the half-wave rectifier.

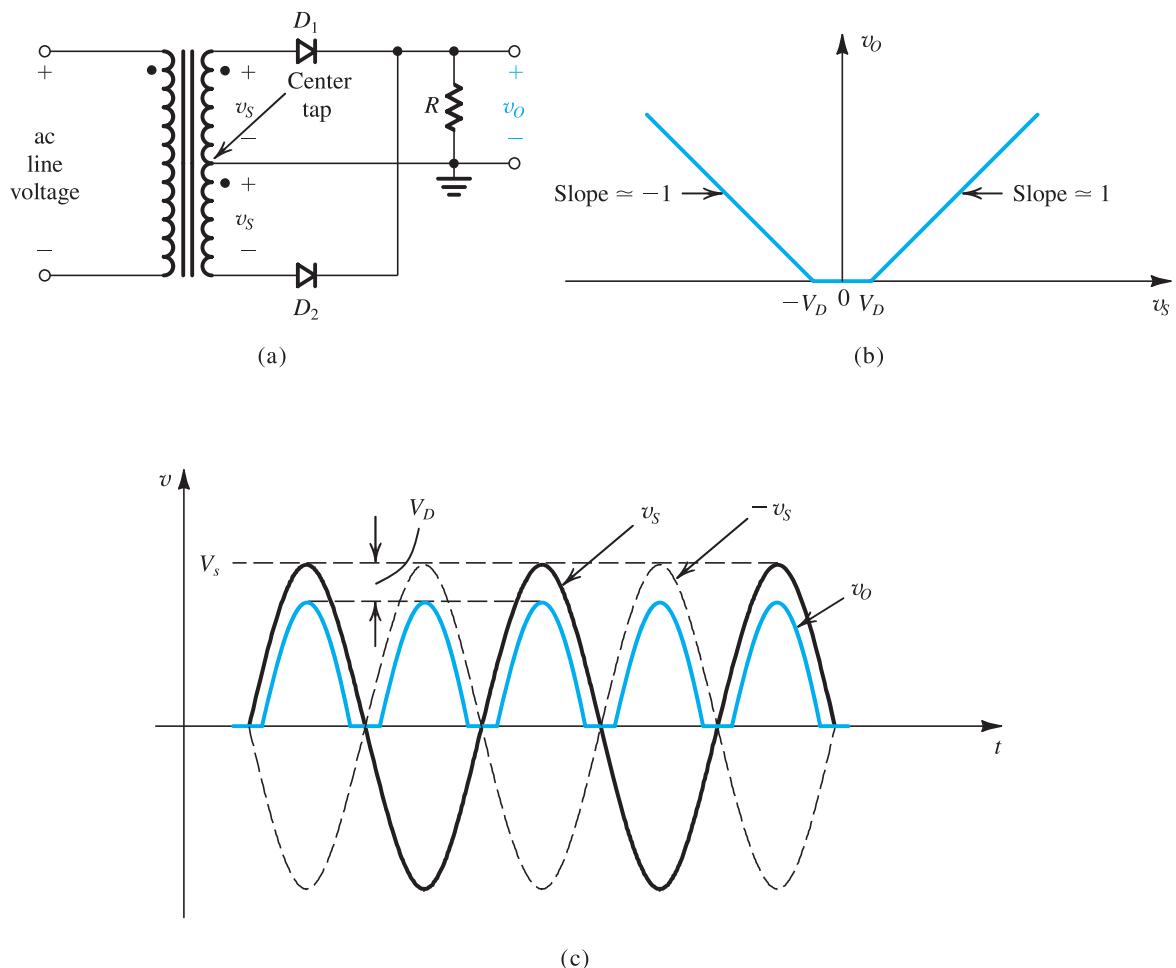
Now, during the negative half-cycle of the ac line voltage, both of the voltages labeled  $v_s$  will be negative. Thus  $D_1$  will be cut off while  $D_2$  will conduct. The current conducted by  $D_2$  will flow through  $R$  and back to the center tap. It follows that during the negative half-cycles while  $D_2$  conducts, the circuit behaves again as a half-wave rectifier. The important point, however, is that the current through  $R$  always flows in the same direction, and thus  $v_o$  will be unipolar, as indicated in Fig. 4.24(c). The output waveform shown is obtained by assuming that a conducting diode has a constant voltage drop  $V_D$ . Thus the transfer characteristic of the full-wave rectifier takes the shape shown in Fig. 4.24(b).

The full-wave rectifier obviously produces a more “energetic” waveform than that provided by the half-wave rectifier. In almost all rectifier applications, one opts for a full-wave type of some kind.

To find the PIV of the diodes in the full-wave rectifier circuit, consider the situation during the positive half-cycles. Diode  $D_1$  is conducting, and  $D_2$  is cut off. The voltage at the cathode of  $D_2$  is  $v_o$ , and that at its anode is  $-v_s$ . Thus the reverse voltage across  $D_2$  will be  $(v_o + v_s)$ , which will reach its maximum when  $v_o$  is at its peak value of  $(V_s - V_D)$ , and  $v_s$  is at its peak value of  $V_s$ ; thus,

$$\text{PIV} = 2V_s - V_D$$

which is approximately twice that for the case of the half-wave rectifier.



**Figure 4.24** Full-wave rectifier utilizing a transformer with a center-tapped secondary winding: (a) circuit; (b) transfer characteristic assuming a constant-voltage-drop model for the diodes; (c) input and output waveforms.

### EXERCISE

- 4.20** For the full-wave rectifier circuit in Fig. 4.24(a), show the following: (a) The output is zero for an angle of  $2 \sin^{-1}(V_D/V_s)$  centered around the zero-crossing points of the sine-wave input. (b) The average value (dc component) of  $v_o$  is  $V_o \simeq (2/\pi)V_s - V_D$ . (c) The peak current through each diode is  $(V_s - V_D)/R$ . Find the fraction (percentage) of each cycle during which  $v_o > 0$ , the value of  $V_o$ , the peak diode current, and the value of PIV, all for the case in which  $v_s$  is a 12-V (rms) sinusoid,  $V_D \simeq 0.7$  V, and  $R = 100 \Omega$ .

**Ans.** 97.4%; 10.1 V; 163 mA; 33.2 V

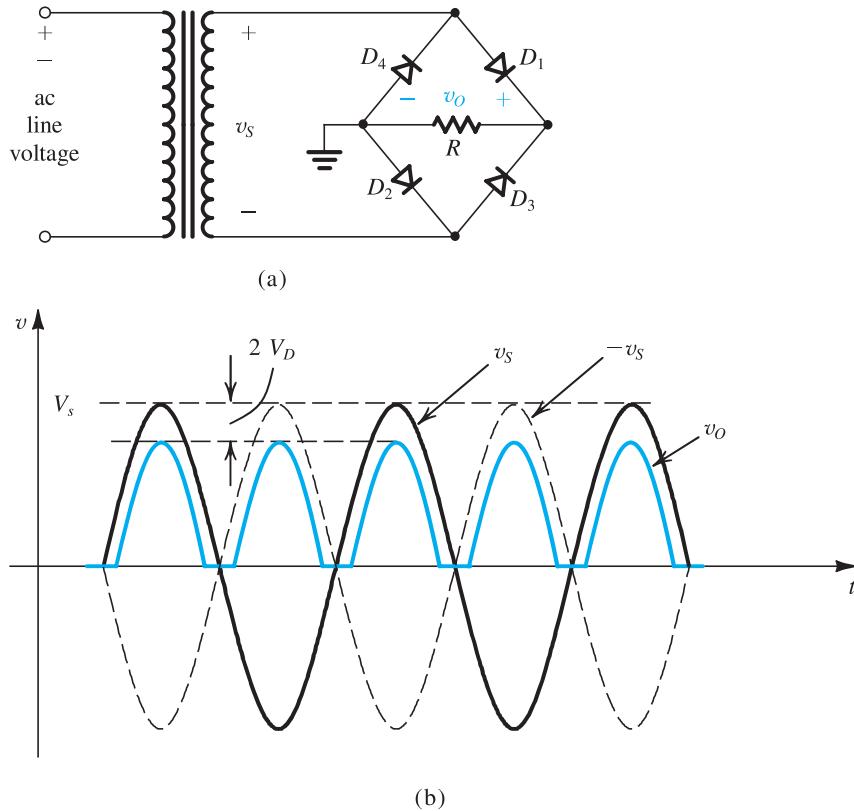
### 4.5.3 The Bridge Rectifier

An alternative implementation of the full-wave rectifier is shown in Fig. 4.25(a). This circuit, known as the bridge rectifier because of the similarity of its configuration to that of the Wheatstone bridge, does not require a center-tapped transformer, a distinct advantage over the full-wave rectifier circuit of Fig. 4.24. The bridge rectifier, however, requires four diodes as compared to two in the previous circuit. This is not much of a disadvantage, because diodes are inexpensive and one can buy a diode bridge in one package.

The bridge-rectifier circuit operates as follows: During the positive half-cycles of the input voltage,  $v_s$  is positive, and thus current is conducted through diode  $D_1$ , resistor  $R$ , and diode  $D_2$ . Meanwhile, diodes  $D_3$  and  $D_4$  will be reverse biased. Observe that there are two diodes in series in the conduction path, and thus  $v_o$  will be lower than  $v_s$  by two diode drops (compared to one drop in the circuit previously discussed). This is somewhat of a disadvantage of the bridge rectifier.

Next, consider the situation during the negative half-cycles of the input voltage. The secondary voltage  $v_s$  will be negative, and thus  $-v_s$  will be positive, forcing current through  $D_3$ ,  $R$ , and  $D_4$ . Meanwhile, diodes  $D_1$  and  $D_2$  will be reverse biased. The important point to note, though, is that during both half-cycles, current flows through  $R$  in the same direction (from right to left), and thus  $v_o$  will always be positive, as indicated in Fig. 4.25(b).

To determine the peak inverse voltage (PIV) of each diode, consider the circuit during the positive half-cycles. The reverse voltage across  $D_3$  can be determined from the loop formed



**Figure 4.25** The bridge rectifier: (a) circuit; (b) input and output waveforms.

by  $D_3$ ,  $R$ , and  $D_2$  as

$$v_{D3}(\text{reverse}) = v_o + v_{D2}(\text{forward})$$

Thus the maximum value of  $v_{D3}$  occurs at the peak of  $v_o$  and is given by

$$\text{PIV} = V_s - 2V_D + V_D = V_s - V_D$$

Observe that here the PIV is about half the value for the full-wave rectifier with a center-tapped transformer. This is another advantage of the bridge rectifier.

Yet one more advantage of the bridge-rectifier circuit over that utilizing a center-tapped transformer is that only about half as many turns are required for the secondary winding of the transformer. Another way of looking at this point can be obtained by observing that each half of the secondary winding of the center-tapped transformer is utilized for only half the time. These advantages have made the bridge rectifier the most popular rectifier circuit configuration.

### EXERCISE

- 4.21** For the bridge-rectifier circuit of Fig. 4.25(a), use the constant-voltage-drop diode model to show that  
 (a) the average (or dc component) of the output voltage is  $V_o \simeq (2/\pi)V_s - 2V_D$  and (b) the peak diode current is  $(V_s - 2V_D)/R$ . Find numerical values for the quantities in (a) and (b) and the PIV for the case in which  $v_s$  is a 12-V (rms) sinusoid,  $V_D \simeq 0.7$  V, and  $R = 100 \Omega$ .

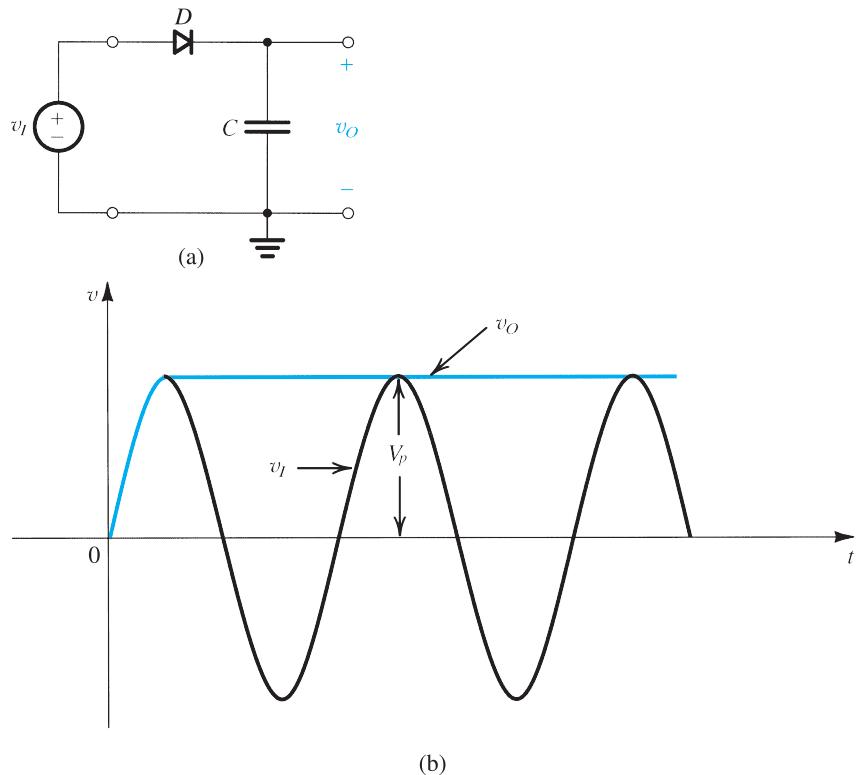
**Ans.** 9.4 V; 156 mA; 16.3 V

### 4.5.4 The Rectifier with a Filter Capacitor—The Peak Rectifier

The pulsating nature of the output voltage produced by the rectifier circuits discussed above makes it unsuitable as a dc supply for electronic circuits. A simple way to reduce the variation of the output voltage is to place a capacitor across the load resistor. It will be shown that this **filter capacitor** serves to reduce substantially the variations in the rectifier output voltage.

To see how the rectifier circuit with a filter capacitor works, consider first the simple circuit shown in Fig. 4.26. Let the input  $v_i$  be a sinusoid with a peak value  $V_p$ , and assume the diode to be ideal. As  $v_i$  goes positive, the diode conducts and the capacitor is charged so that  $v_o = v_i$ . This situation continues until  $v_i$  reaches its peak value  $V_p$ . Beyond the peak, as  $v_i$  decreases, the diode becomes reverse biased and the output voltage remains constant at the value  $V_p$ . In fact, theoretically speaking, the capacitor will retain its charge and hence its voltage indefinitely, because there is no way for the capacitor to discharge. Thus the circuit provides a dc voltage output equal to the peak of the input sine wave. This is a very encouraging result in view of our desire to produce a dc output.

Next, we consider the more practical situation where a load resistance  $R$  is connected across the capacitor  $C$ , as depicted in Fig. 4.27(a). However, we will continue to assume the diode to be ideal. As before, for a sinusoidal input, the capacitor charges to the peak of the input  $V_p$ . Then the diode cuts off, and the capacitor discharges through the load resistance  $R$ . The capacitor discharge will continue for almost the entire cycle, until the time at which  $v_i$



**Figure 4.26** (a) A simple circuit used to illustrate the effect of a filter capacitor. (b) Input and output waveforms assuming an ideal diode. Note that the circuit provides a dc voltage equal to the peak of the input sine wave. The circuit is therefore known as a *peak rectifier* or a *peak detector*.

exceeds the capacitor voltage. Then the diode turns on again and charges the capacitor up to the peak of  $v_I$ , and the process repeats itself. Observe that to keep the output voltage from decreasing too much during capacitor discharge, one selects a value for  $C$  so that the time constant  $CR$  is much greater than the discharge interval.

We are now ready to analyze the circuit in detail. Figure 4.27(b) shows the steady-state input and output voltage waveforms under the assumption that  $CR \gg T$ , where  $T$  is the period of the input sinusoid. The waveforms of the load current

$$i_L = v_O/R \quad (4.23)$$

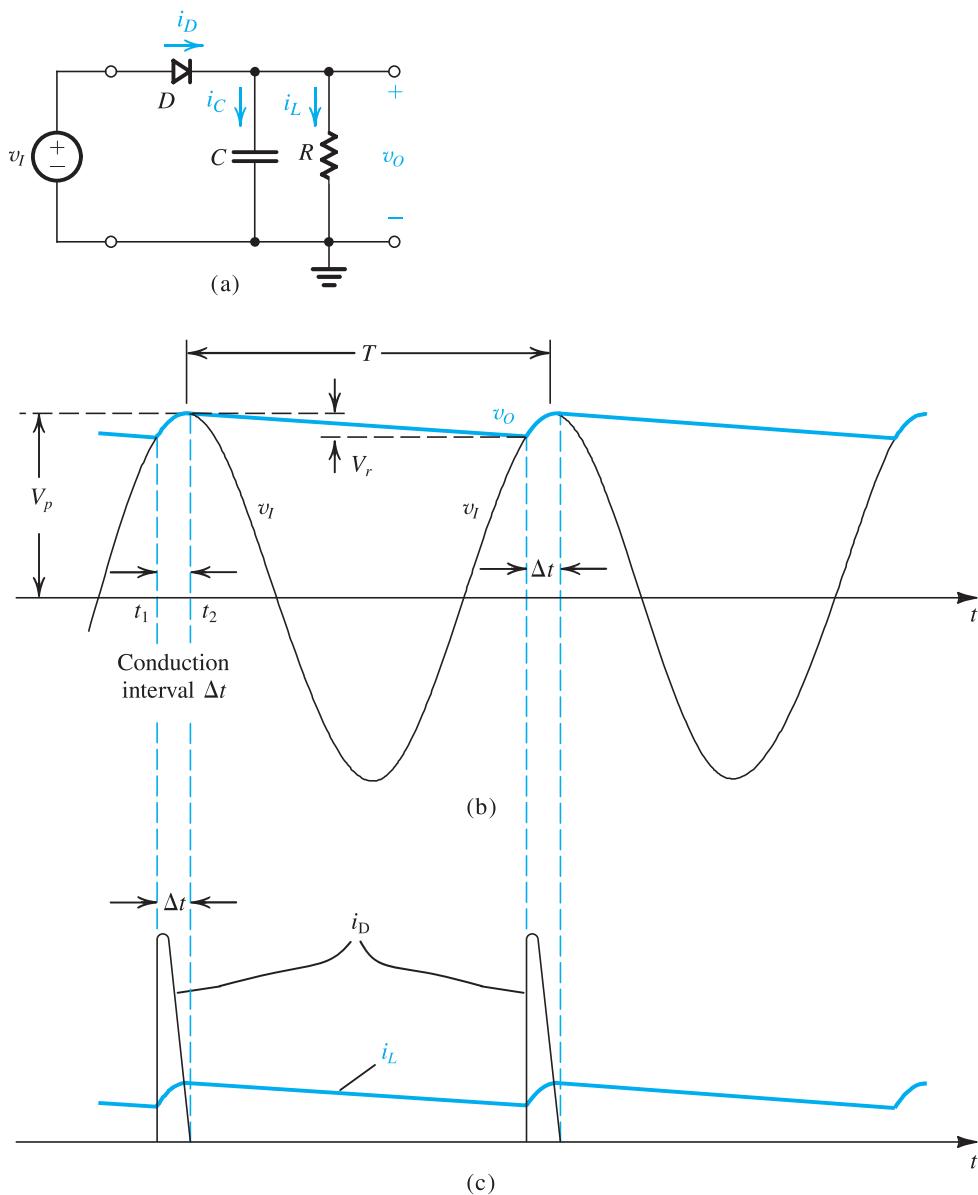
and of the diode current (when it is conducting)

$$i_D = i_C + i_L \quad (4.24)$$

$$= C \frac{dv_I}{dt} + i_L \quad (4.25)$$

are shown in Fig. 4.27(c). The following observations are in order:

1. The diode conducts for a brief interval,  $\Delta t$ , near the peak of the input sinusoid and supplies the capacitor with charge equal to that lost during the much longer discharge interval. The latter is approximately equal to the period  $T$ .



**Figure 4.27** Voltage and current waveforms in the peak-rectifier circuit with  $CR \gg T$ . The diode is assumed ideal.

2. Assuming an ideal diode, the diode conduction begins at time  $t_1$ , at which the input  $v_l$  equals the exponentially decaying output  $v_o$ . Conduction stops at  $t_2$  shortly after the peak of  $v_l$ ; the exact value of  $t_2$  can be determined by setting  $i_D = 0$  in Eq. (4.25).
3. During the diode-off interval, the capacitor  $C$  discharges through  $R$ , and thus  $v_o$  decays exponentially with a time constant  $CR$ . The discharge interval begins just past the peak of  $v_l$ . At the end of the discharge interval, which lasts for almost the entire period  $T$ ,  $v_o = V_p - V_r$ , where  $V_r$  is the peak-to-peak ripple voltage. When  $CR \gg T$ , the value of  $V_r$  is small.

4. When  $V_r$  is small,  $v_o$  is almost constant and equal to the peak value of  $v_i$ . Thus the dc output voltage is approximately equal to  $V_p$ . Similarly, the current  $i_L$  is almost constant, and its dc component  $I_L$  is given by

➤ 
$$I_L = \frac{V_p}{R} \quad (4.26)$$

If desired, a more accurate expression for the output dc voltage can be obtained by taking the average of the extreme values of  $v_o$ ,

➤ 
$$V_o = V_p - \frac{1}{2}V_r \quad (4.27)$$

With these observations in hand, we now derive expressions for  $V_r$  and for the average and peak values of the diode current. During the diode-off interval,  $v_o$  can be expressed as

$$v_o = V_p e^{-t/CR}$$

At the end of the discharge interval we have

$$V_p - V_r \simeq V_p e^{-T/CR}$$

Now, since  $CR \gg T$ , we can use the approximation  $e^{-T/CR} \simeq 1 - T/CR$  to obtain

$$V_r \simeq V_p \frac{T}{CR} \quad (4.28)$$

We observe that to keep  $V_r$  small we must select a capacitance  $C$  so that  $CR \gg T$ . The **ripple voltage**  $V_r$  in Eq. (4.28) can be expressed in terms of the frequency  $f = 1/T$  as

➤ 
$$V_r = \frac{V_p}{fCR} \quad (4.29a)$$

Using Eq. (4.26) we can express  $V_r$  by the alternate expression

$$V_r = \frac{I_L}{fC} \quad (4.29b)$$

Note that an alternative interpretation of the approximation made above is that the capacitor discharges by means of a constant current  $I_L = V_p/R$ . This approximation is valid as long as  $V_r \ll V_p$ .

Assuming that diode conduction ceases almost at the peak of  $v_i$ , we can determine the **conduction interval**  $\Delta t$  from

$$V_p \cos(\omega\Delta t) = V_p - V_r$$

where  $\omega = 2\pi f = 2\pi/T$  is the angular frequency of  $v_i$ . Since  $(\omega\Delta t)$  is a small angle, we can employ the approximation  $\cos(\omega\Delta t) \simeq 1 - \frac{1}{2}(\omega\Delta t)^2$  to obtain

➤ 
$$\omega\Delta t \simeq \sqrt{2V_r/V_p} \quad (4.30)$$

We note that when  $V_r \ll V_p$ , the conduction angle  $\omega\Delta t$  will be small, as assumed.

To determine the average diode current during conduction,  $i_{Dav}$ , we equate the charge that the diode supplies to the capacitor,

$$Q_{\text{supplied}} = i_{Cav} \Delta t$$

where from Eq. (4.24),

$$i_{Cav} = i_{Dav} - I_L$$

to the charge that the capacitor loses during the discharge interval,

$$Q_{lost} = CV_r$$

to obtain, using Eqs. (4.30) and (4.29a),

$$i_{Dav} = I_L \left( 1 + \pi \sqrt{2V_p/V_r} \right) \quad (4.31)$$

Observe that when  $V_r \ll V_p$ , the average diode current during conduction is much greater than the dc load current. This is not surprising, since the diode conducts for a very short interval and must replenish the charge lost by the capacitor during the much longer interval in which it is discharged by  $I_L$ .

The peak value of the diode current,  $i_{Dmax}$ , can be determined by evaluating the expression in Eq. (4.25) at the onset of diode conduction—that is, at  $t = t_1 = -\Delta t$  (where  $t = 0$  is at the peak). Assuming that  $i_L$  is almost constant at the value given by Eq. (4.26), we obtain

$$i_{Dmax} = I_L \left( 1 + 2\pi \sqrt{2V_p/V_r} \right) \quad (4.32)$$

From Eqs. (4.31) and (4.32), we see that for  $V_r \ll V_p$ ,  $i_{Dmax} \approx 2i_{Dav}$ , which correlates with the fact that the waveform of  $i_D$  is almost a right-angle triangle (see Fig. 4.27c).

### Example 4.8

Consider a peak rectifier fed by a 60-Hz sinusoid having a peak value  $V_p = 100$  V. Let the load resistance  $R = 10$  k $\Omega$ . Find the value of the capacitance  $C$  that will result in a peak-to-peak ripple of 2 V. Also, calculate the fraction of the cycle during which the diode is conducting and the average and peak values of the diode current.

#### Solution

From Eq. (4.29a) we obtain the value of  $C$  as

$$C = \frac{V_p}{V_r f R} = \frac{100}{2 \times 60 \times 10 \times 10^3} = 83.3 \mu\text{F}$$

The conduction angle  $\omega\Delta t$  is found from Eq. (4.30) as

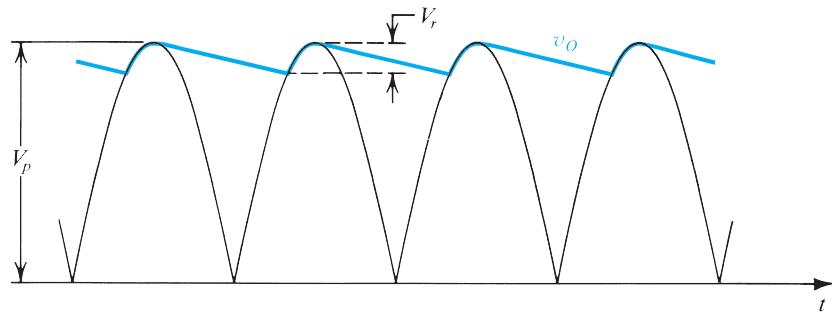
$$\omega\Delta t = \sqrt{2 \times 2/100} = 0.2 \text{ rad}$$

Thus the diode conducts for  $(0.2/2\pi) \times 100 = 3.18\%$  of the cycle. The average diode current is obtained from Eq. (4.31), where  $I_L = 100/10 = 10$  mA, as

$$i_{Dav} = 10 \left( 1 + \pi \sqrt{2 \times 100/2} \right) = 324 \text{ mA}$$

The peak diode current is found using Eq. (4.32),

$$i_{Dmax} = 10 \left( 1 + 2\pi \sqrt{2 \times 100/2} \right) = 638 \text{ mA}$$



**Figure 4.28** Waveforms in the full-wave peak rectifier.

The circuit of Fig. 4.27(a) is known as a half-wave **peak rectifier**. The full-wave rectifier circuits of Figs. 4.24(a) and 4.25(a) can be converted to peak rectifiers by including a capacitor across the load resistor. As in the half-wave case, the output dc voltage will be almost equal to the peak value of the input sine wave (Fig. 4.28). The ripple frequency, however, will be twice that of the input. The peak-to-peak ripple voltage, for this case, can be derived using a procedure identical to that above but with the discharge period  $T$  replaced by  $T/2$ , resulting in

$$V_r = \frac{V_p}{2fCR} \quad (4.33)$$

While the diode conduction interval,  $\Delta t$ , will still be given by Eq. (4.30), the average and peak currents in each of the diodes will be given by

$$i_{Dav} = I_L \left( 1 + \pi \sqrt{V_p/2V_r} \right) \quad (4.34)$$

$$i_{Dmax} = I_L \left( 1 + 2\pi \sqrt{V_p/2V_r} \right) \quad (4.35)$$

Comparing these expressions with the corresponding ones for the half-wave case, we note that for the same values of  $V_p$ ,  $f$ ,  $R$ , and  $V_r$  (and thus the same  $I_L$ ), we need a capacitor half the size of that required in the half-wave rectifier. Also, the current in each diode in the full-wave rectifier is approximately half that which flows in the diode of the half-wave circuit.

The analysis above assumed ideal diodes. The accuracy of the results can be improved by taking the diode voltage drop into account. This can be easily done by replacing the peak voltage  $V_p$  to which the capacitor charges with  $(V_p - V_D)$  for the half-wave circuit and the full-wave circuit using a center-tapped transformer and with  $(V_p - 2V_D)$  for the bridge-rectifier case.

We conclude this section by noting that peak-rectifier circuits find application in signal-processing systems where it is required to detect the peak of an input signal. In such a case, the circuit is referred to as a **peak detector**. A particularly popular application of the peak detector is in the design of a demodulator for amplitude-modulated (AM) signals. We shall not discuss this application further here.

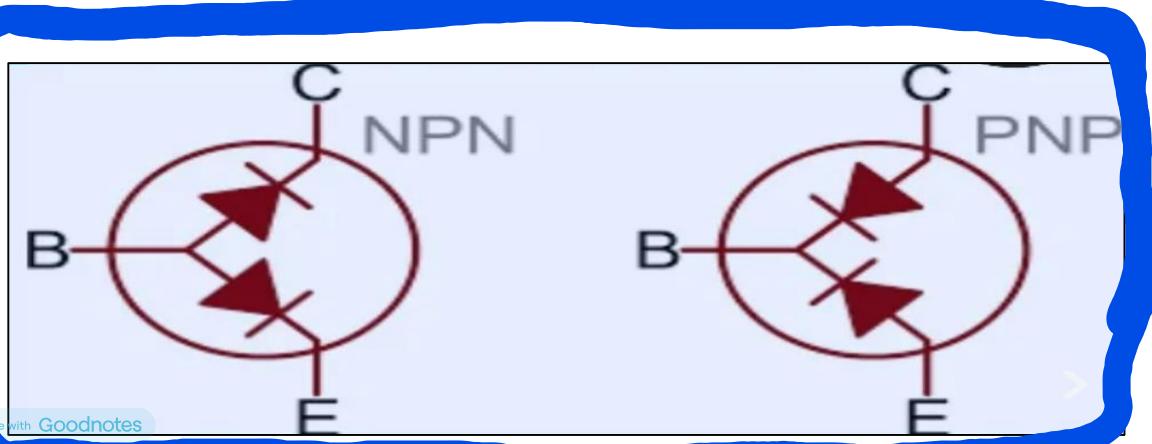
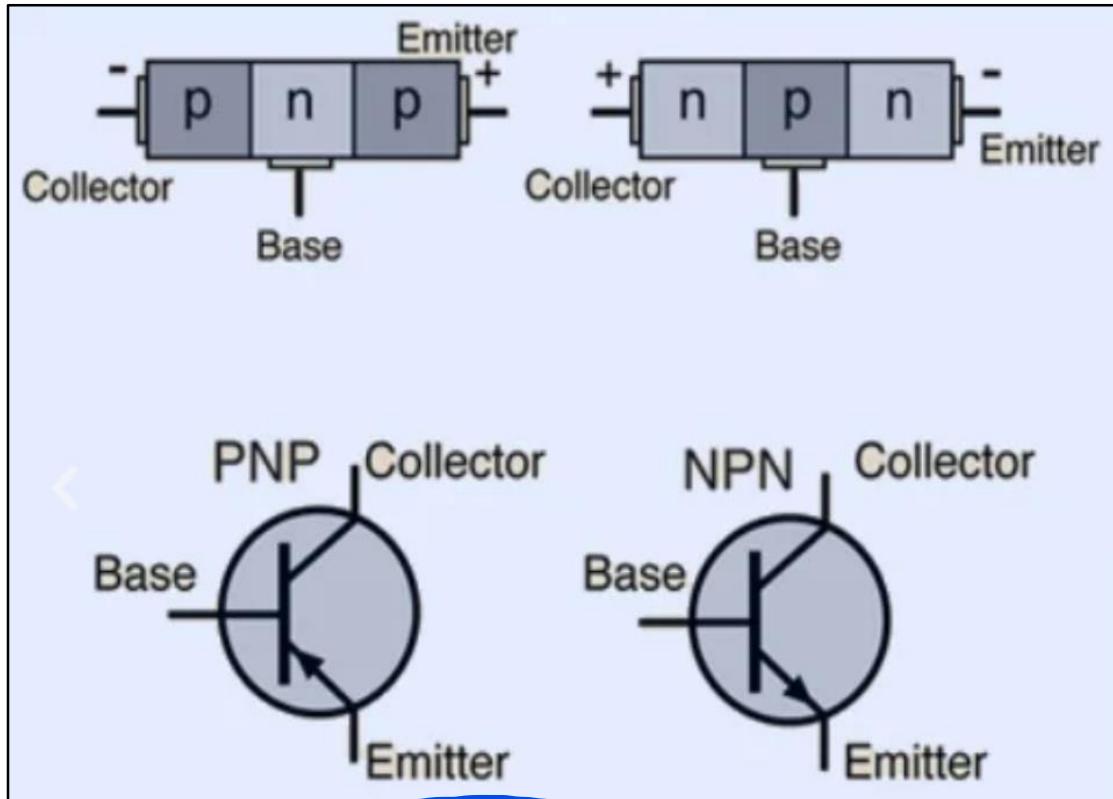
# Lecture 3B: BJT Circuits

EE 103

2023-24/I (Autumn)

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# Bipolar Junction Transistor (BJT)

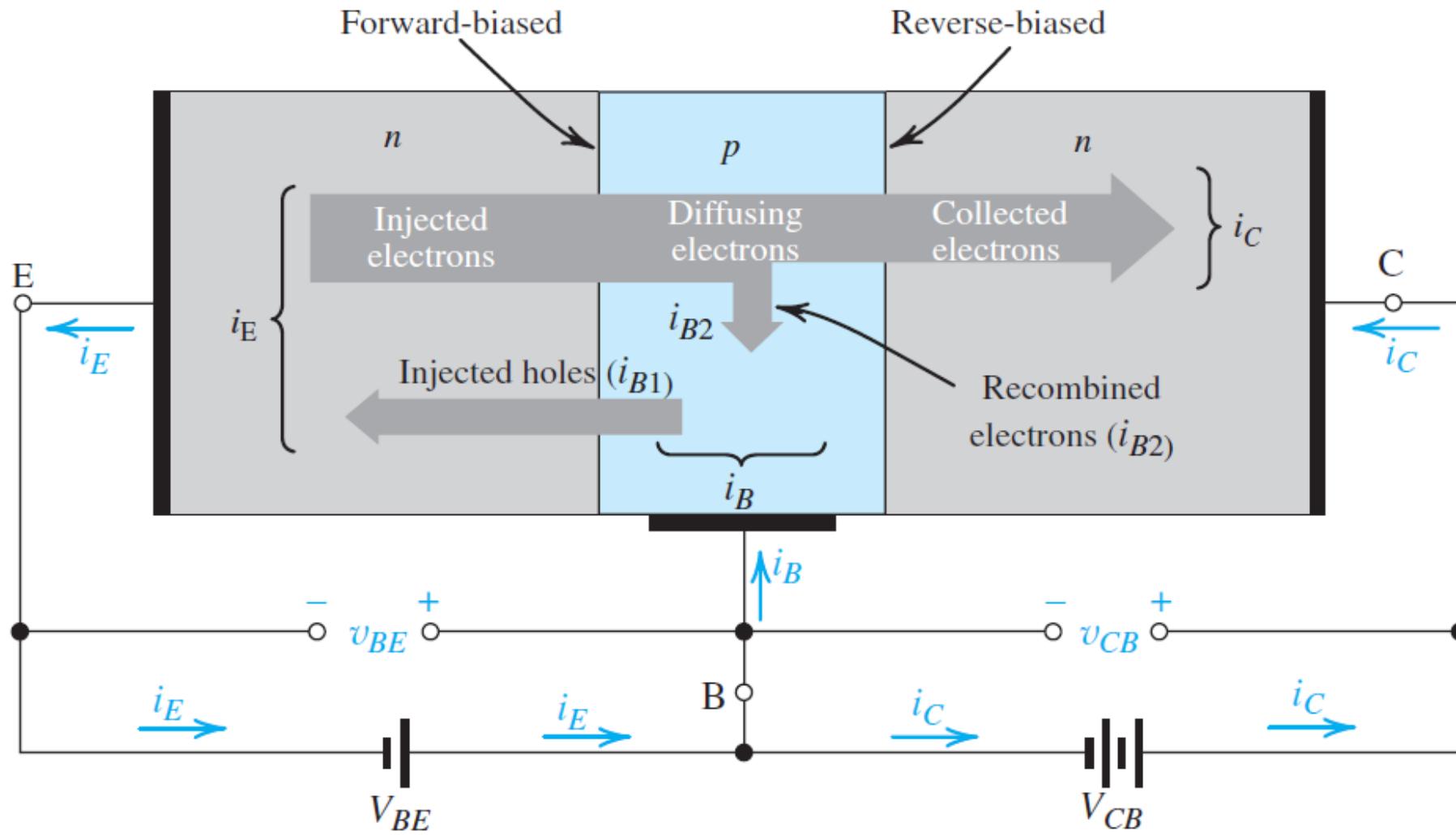


Parameter	BJT
<b>Types</b>	Based on the construction, BJTs are classified into two types: NPN and PNP
<b>Terminals</b>	BJT has three terminals viz. <b>emitter</b> , <b>base</b> and <b>collector</b> .
<b>Controlling quantity</b>	BJT is a current controlled device <b>Base current (<math>I_B</math>) controls the Collector Current (<math>I_C</math>)</b>
<b>Applications</b>	BJT is used in Following applications <ol style="list-style-type: none"><li>1. Amplifiers</li><li>2. Oscillators</li><li><b>3. Switches</b></li><li>4. Buffers</li></ol>

# Modes of Operation

- BJT has Three terminals, Two junctions:
  - Base-Emitter Junction and Base Collector Junction
- Base-Emitter is the main controlling junction

- Three main modes of operation:
  - Cut-off: Both Base-Emitter and Base-Collector junctions reverse-biased
  - Active : Base-Emitter junction is forward-biased, Base-Collector junction reverse biased.
  - Saturation: Both Base-Emitter and Base-Collector junctions are forward-biased



**Figure 6.3** Current flow in an *npn* transistor biased to operate in the active mode. (Reverse current components due to drift of thermally generated minority carriers are not shown.)

# Basic Equations

- $I_E = I_B + I_C$  (KCL) – always true
- $\beta = I_C/I_B$  (Current gain in the Common-Emitter mode)
  - $\beta \gg 1$
  - Common Emitter: Input applied between Base and Emitter, Output between Collector and Emitter. Emitter is common to both input and output.
- $\alpha = I_C/I_E$  (Current gain in the Common-Base mode)
  - $\alpha < 1$
  - Common Base: Input applied between Emitter and Base, Output between Collector and Base. Base is common to both input and output.
- $\beta = \alpha/(1-\alpha); \alpha = \beta/(\beta+1)$

# BJT Inverter

- **Case-1**  $V_{IN} < V_{BE}$  (Less than PN Junction Conduction Voltage)

$I_B = 0, I_C = 0 \rightarrow V_{out} = V_{CE} = V_{CC}$  (BJT is said to be Cut-off)

- **Case-2**  $V_{IN} > V_{BE}$  BJT Conducts, with  $I_B > 0$

$$I_B = (V_{IN} - V_{BE}) / R_B \quad \text{and} \quad I_C = \beta I_B \rightarrow V_{OUT} = V_{CE} = V_{CC} - I_C R_C$$

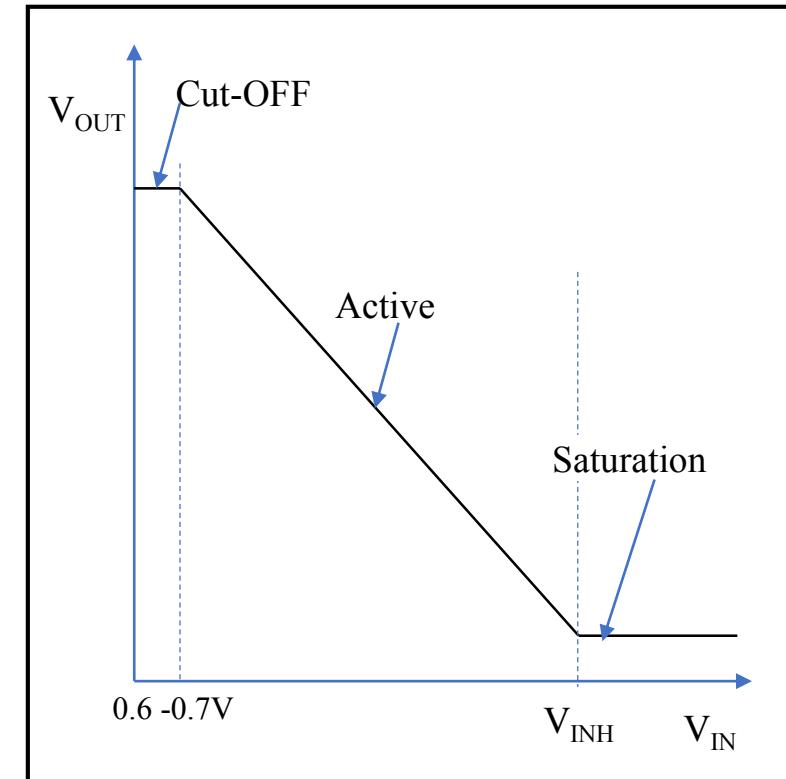
$$V_{CEmin} = V_{CESat} = 0.2 \text{ V} \quad I_{CMax} = (V_{CC} - V_{CESat}) / R_C = \beta I_{BSat}$$

At that point  $V_{BE} = 0.7 \text{ V}$  and Corresponding  $V_{INH} = I_{BSat} R_B + V_{BE}$   
(Active/ Linear Region)

- **Case-3**  $V_{IN} > V_{INH}$

$$I_B = (V_{IN} - V_{BESat}) / R_B \quad \text{and} \quad I_C = I_{CMax} \quad \text{But} \quad I_B \beta > I_{CMax}$$

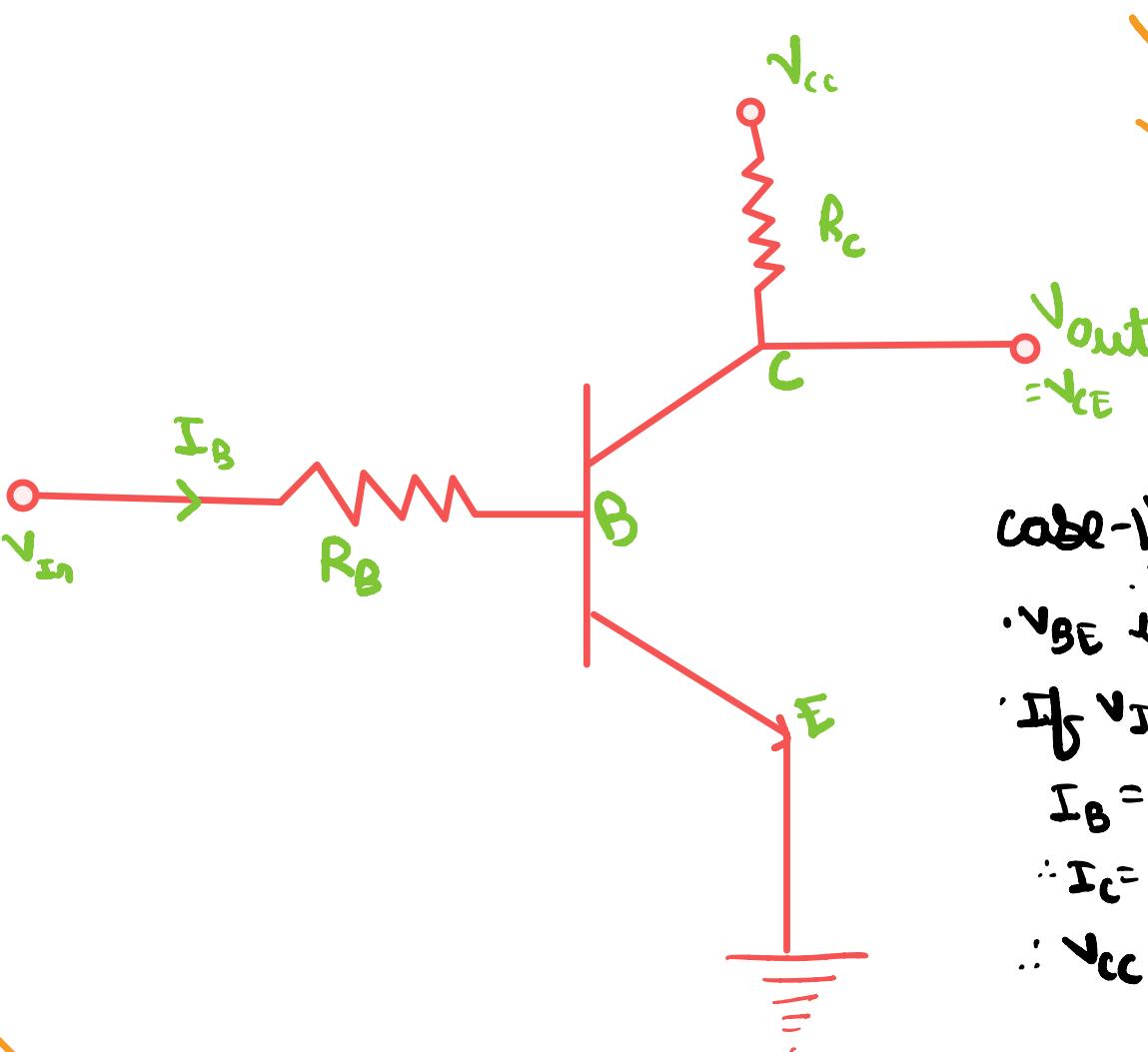
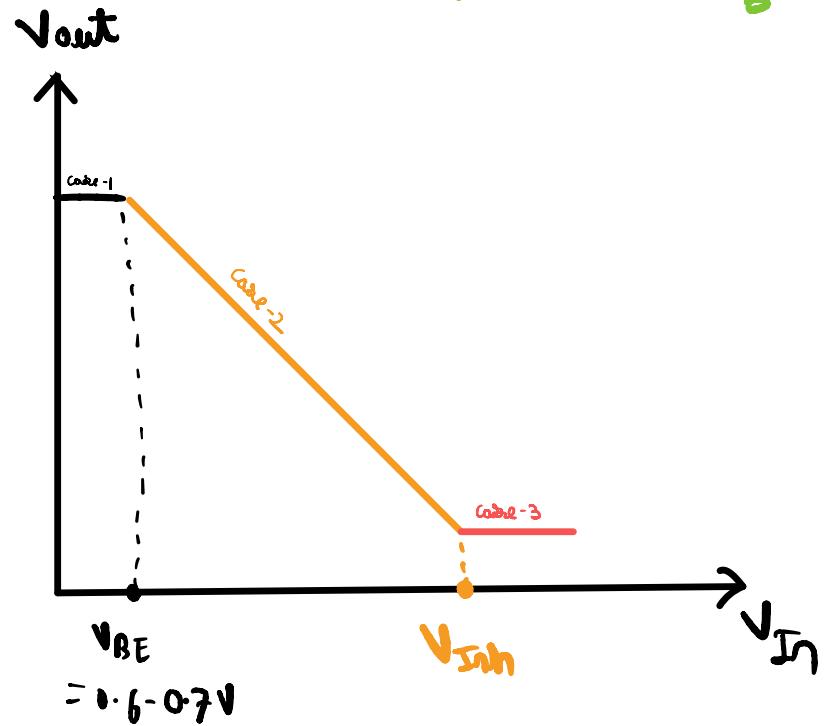
(BJT is said to be in Saturation)



Conditions on ( $V_{in}$ ) →

$V_{IN} < V_{BE}$  ( $=V_{IL}$ )  
BJT: OFF

$V_{IN} > V_{INH}$   
(BJT: Saturation)



$$V_{in} = I_B R_B + V_{BE}$$

$$V_{cc} = I_C R_C + V_{CE}$$

case-1)  $V_{in} < V_{BE}$

$\cdot V_{BE}$  is  $0.6 - 0.7\text{V}$  generally

If  $V_{in} < V_{BE}$

$$I_B = 0$$

$$\therefore I_C = \beta I_B = 0$$

$$\therefore V_{cc} = V_{CE} = V_{out}$$

Case-2)  $V_{IN} > V_{BE}$

$$I_B = \frac{V_{IN} - V_{BE}}{R_B}$$

$$I_C = \beta \left( \frac{V_{IN} - V_{BE}}{R_B} \right)$$

$$\therefore V_{OUT} = V_{CE} = V_{CC} - \beta \left( \frac{V_{IN} - V_{BE}}{R_B} \right) R_C$$

$\therefore$  Linear variation

Now  $V_{CE}$  has 0 min (diode drop)

$$V_{CE\min} = V_{CE\text{sat}} = 0.2V$$

$$I_{CM\max} = \frac{(V_{CC} - V_{CE\text{sat}})}{R_C}$$

$I_C$  can't exceed this

But as  $I_B$  inc. this extra is stored as base charge.

$$\overbrace{V_{CE}}^{0.2V} = V_{CB} + \underbrace{V_{BE}}_{0.6-0.7V}$$

$V_{CG} = -VE$  i.e. earlier it was in Inverse but now its  $-VE$   $\therefore$  Base-collector is Forward biased  $\Rightarrow$  Saturation mode

corresponding  $V_{IN}$ :

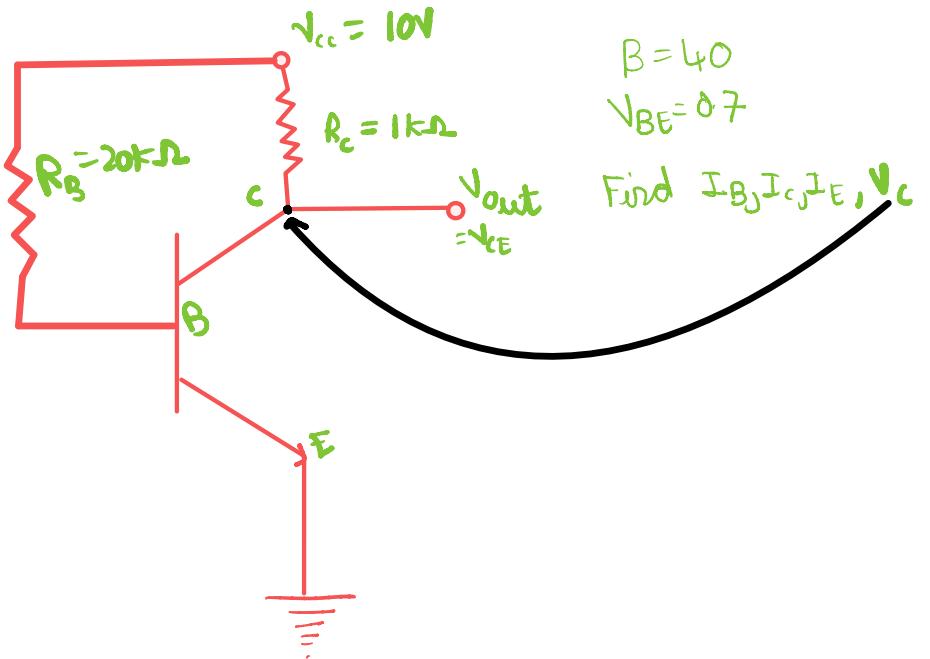
$$V_{IN} = V_{BE} + \frac{R_B}{\beta \cdot R_C} (V_{CC} - V_{CE\text{sat}}) = V_{INH}$$

Case-3)  $V_{IN} > V_{INH}$

$\therefore$  Saturation mode

$$I_C = \text{const} \quad \therefore V_{OUT} = \text{const}$$

EX-



$$\rightarrow V_{cc} - I_B R_b - V_{BE} = 0$$

$$\therefore I_B = \frac{V_{cc} - V_{BE}}{R_b} = \frac{10 - 0.7}{20 \times 10^3} = \frac{9.3}{20} \times 10^{-3} = 0.465 \text{ mA}$$

$$I_C = \beta I_B = 18.6 \text{ mA}$$

$$I_E = I_B + I_C = 19.065 \text{ mA}$$

$$V_C = 10 - I_C R_C = 10 - 18.6 = -8.6V \quad \left. \right\} V_{CE} = -8.6V < V_{CE \text{ sat}}$$

∴ Transistor is in Saturation mode

$$\therefore V_c = 0.2 \text{ V}$$

$$I_C = 9.8 \text{ mA}$$

$$I_B = 0.465 \text{ mA}$$

$$I_E = 10.265 \text{ mA}$$

## CHAPTER 6

# Bipolar Junction Transistors (BJTs)

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<b>6.1 Device Structure and Physical Operation</b>	<b>306</b>
<b>6.2 Current–Voltage Characteristics</b>	<b>320</b>
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## IN THIS CHAPTER YOU WILL LEARN

1. The physical structure of the bipolar transistor and how it works.
2. How the voltage between two terminals of the transistor controls the current that flows through the third terminal, and the equations that describe these current–voltage characteristics.
3. How to analyze and design circuits that contain bipolar transistors, resistors, and dc sources.

---

## Introduction

In this chapter, we study the other major three-terminal device: the bipolar junction transistor (BJT). The presentation of the material in this chapter parallels but does not rely on that for the MOSFET in Chapter 5; thus, if desired, the BJT can be studied before the MOSFET.

Three-terminal devices are far more useful than two-terminal ones, such as the diodes studied in Chapter 4, because they can be used in a multitude of applications, ranging from signal amplification to the design of digital logic and memory circuits. The basic principle involved is the use of the voltage between two terminals to control the current flowing in the third terminal. In this way, a three-terminal device can be used to realize a controlled source, which as we learned in Chapter 1 is the basis for amplifier design. Also, in the extreme, the control signal can be used to cause the current in the third terminal to change from zero to a large value, thus allowing the device to act as a switch. The switch is the basis for the realization of the logic inverter, the basic element of digital circuits.

The invention of the BJT in 1948 at the Bell Telephone Laboratories ushered in the era of solid-state circuits. The result was not just the replacement of vacuum tubes by transistors in radios and television sets but the eruption of an electronics revolution that led to major changes in the way we work, play, and indeed, live. The invention of the transistor also eventually led to the dominance of information technology and the emergence of the knowledge-based economy.

The bipolar transistor enjoyed nearly three decades as the device of choice in the design of both discrete and integrated circuits. Although the MOSFET had been known very early on, it was not until the 1970s and 1980s that it became a serious competitor to the BJT. By 2014, the MOSFET was undoubtedly the most widely used electronic device, and CMOS technology the technology of choice in the design of integrated circuits. Nevertheless, the BJT remains a significant device that excels in certain applications.

The BJT remains popular in discrete-circuit design, where it is used together with other discrete components such as resistors and capacitors to implement circuits that are assembled

on printed-circuit boards (PCBs). Here we note the availability of a very wide selection of BJT types that fit nearly every conceivable application. As well, the BJT is still the preferred device in some very demanding analog and digital integrated-circuit applications. This is especially true in very-high-frequency and high-speed circuits. In particular, a very-high-speed digital logic-circuit family based on bipolar transistors, namely, emitter-coupled logic, is still in use (Chapter 15). Finally, bipolar transistors can be combined with MOSFETs to create innovative circuits that take advantage of the high-input-impedance and low-power operation of MOSFETs and the very-high-frequency operation and high-current-driving capability of bipolar transistors. The resulting technology is known as BiCMOS, and it is finding increasingly larger areas of application (see Chapters 8, 9, 13, and 15).

In this chapter, we shall start with a description of the physical operation of the BJT. Though simple, this physical description provides considerable insight regarding the performance of the transistor as a circuit element. We then quickly move from describing current flow in terms of electrons and holes to a study of the transistor terminal characteristics. Circuit models for transistor operation in different modes will be developed and utilized in the analysis and design of transistor circuits. The main objective of this chapter is to develop in the reader a high degree of familiarity with the BJT. Thus, it lays the foundation for the use of the BJT in amplifier design (Chapter 7).

## 6.1 Device Structure and Physical Operation

### 6.1.1 Simplified Structure and Modes of Operation

Figure 6.1 shows a simplified structure for the BJT. A practical transistor structure will be shown later (see also Appendix A, which deals with fabrication technology).

As shown in Fig. 6.1, the BJT consists of three semiconductor regions: the emitter region (*n* type), the base region (*p* type), and the collector region (*n* type). Such a transistor is called an *npn* transistor. Another transistor, a dual of the *npn* as shown in Fig. 6.2, has a *p*-type emitter, an *n*-type base, and a *p*-type collector, and is appropriately called a *pnp* transistor.

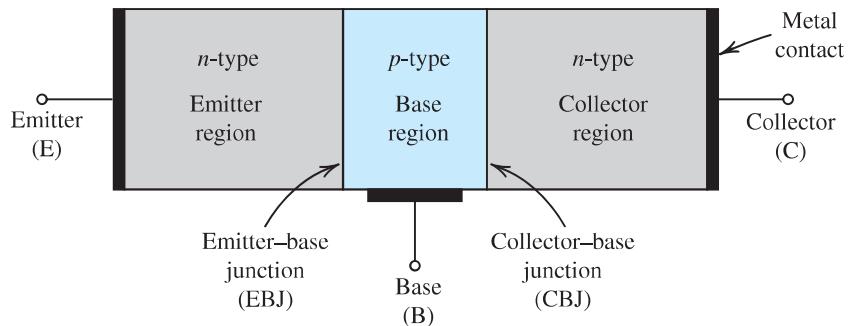
A terminal is connected to each of the three semiconductor regions of the transistor, with the terminals labeled **emitter** (E), **base** (B), and **collector** (C).

The transistor consists of two *pn* junctions, the **emitter-base junction** (EBJ) and the **collector-base junction** (CBJ). Depending on the bias condition (forward or reverse) of each of these junctions, different modes of operation of the BJT are obtained, as shown in Table 6.1. The **active mode** is the one used if the transistor is to operate as an amplifier. Switching applications (e.g., logic circuits) utilize both the **cutoff mode** and the **saturation mode**. As the name implies, in the cutoff mode no current flows because both junctions are reverse biased.

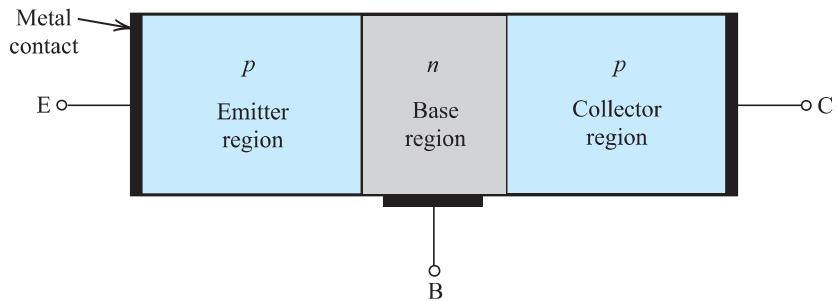
As we will see shortly, charge carriers of both polarities—that is, electrons and holes—participate in the current-conduction process in a bipolar transistor, which is the reason for the name *bipolar*.<sup>1</sup>

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<sup>1</sup>This should be contrasted with the situation in the MOSFET, where current is conducted by charge carriers of one type only: electrons in *n*-channel devices or holes in *p*-channel devices. In earlier days, some referred to FETs as unipolar devices.



**Figure 6.1** A simplified structure of the *npn* transistor.



**Figure 6.2** A simplified structure of the *pnp* transistor.

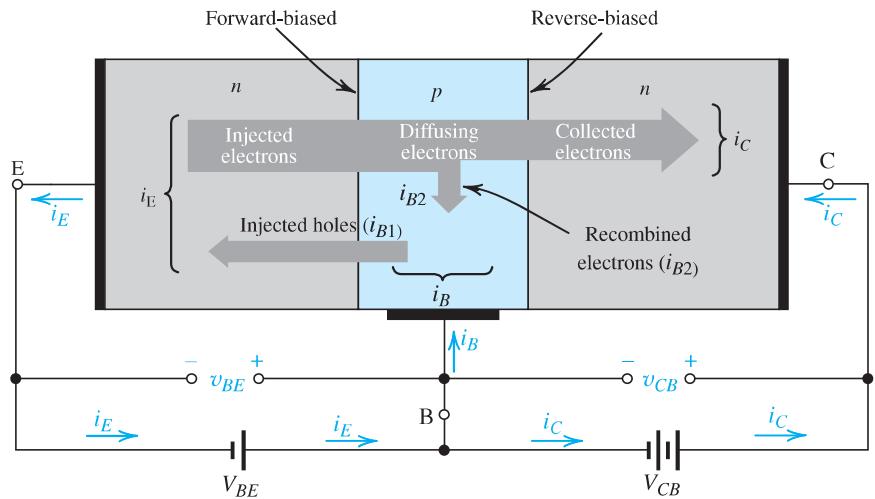
**Table 6.1** BJT Modes of Operation

Mode	EBJ	CBJ
Cutoff	Reverse	Reverse
Active	Forward	Reverse
Saturation	Forward	Forward

### 6.1.2 Operation of the npn Transistor in the Active Mode

Of the three modes of operation of the BJT, the active mode is the most important. Therefore, we begin our study of the BJT by considering its physical operation in the active mode.<sup>2</sup> This situation is illustrated in Fig. 6.3 for the *npn* transistor. Two external voltage sources (shown as batteries) are used to establish the required bias conditions for active-mode operation. The voltage  $V_{BE}$  causes the *p*-type base to be higher in potential than the *n*-type emitter, thus forward biasing the emitter-base junction. The collector-base voltage  $V_{CB}$  causes the *n*-type collector to be at a higher potential than the *p*-type base, thus reverse biasing the collector-base junction.

<sup>2</sup>The material in this section assumes that the reader is familiar with the operation of the *pn* junction under forward-bias conditions (Section 3.5).



**Figure 6.3** Current flow in an *npn* transistor biased to operate in the active mode. (Reverse current components due to drift of thermally generated minority carriers are not shown.)

**Current Flow** The forward bias on the emitter–base junction will cause current to flow across this junction. Current will consist of two components: electrons injected from the emitter into the base, and holes injected from the base into the emitter. As will become apparent shortly, it is highly desirable to have the first component (electrons from emitter to base) be much larger than the second component (holes from base to emitter). This can be accomplished by fabricating the device with a heavily doped emitter and a lightly doped base; that is, the device is designed to have a high density of electrons in the emitter and a low density of holes in the base.

The current that flows across the emitter–base junction will constitute the emitter current  $i_E$ , as indicated in Fig. 6.3. The direction of  $i_E$  is “out of” the emitter lead, which, following the usual conventions, is in the direction of the positive-charge flow (hole current) and opposite to the direction of the negative-charge flow (electron current), with the emitter current  $i_E$  being equal to the sum of these two components. However, since the electron component is much larger than the hole component, the emitter current will be dominated by the electron component.

From our study in Section 3.5 of the current flow across a forward-biased *pn* junction, we know that the magnitude of both the electron component and the hole component of  $i_E$  will be proportional to  $e^{v_{BE}/V_T}$ , where  $v_{BE}$  is the forward voltage across the base–emitter junction and  $V_T$  is the thermal voltage (approximately 25 mV at room temperature).

Let’s now focus our attention on the first current component, namely, that carried by electrons injected from the emitter into the base. These electrons will be **minority carriers** in the *p*-type base region. Because their concentration will be highest at the emitter side of the base, the injected electrons will diffuse through the base region toward the collector. In their journey across the base, some of the electrons will combine with holes, which are majority carriers in the base. However, since the base is usually very thin and, as mentioned earlier, lightly doped, the proportion of electrons that are “lost” through this **recombination process** will be quite small. Thus, most of the diffusing electrons will reach the boundary of the collector–base depletion region. Because the collector is more positive than the base (by the

reverse-bias voltage  $v_{CB}$ ), these successful electrons will be swept across the CBJ depletion region into the collector. They will thus get collected and constitute the collector current  $i_C$ .

**The Collector Current** From the foregoing statements, we see that the collector current is carried by the electrons that reach the collector region. Its direction will be opposite to that of the flow of electrons, and thus into the collector terminal. Its magnitude will be proportional to  $e^{v_{BE}/V_T}$ , thus

$$i_C = I_S e^{v_{BE}/V_T} \quad (6.1)$$

where the constant of proportionality  $I_S$ , as in the case of the diode, is called the **saturation current** and is a transistor parameter. We will have more to say about  $I_S$  shortly.

An important observation to make here is that  $i_C$  is independent of the value of  $v_{CB}$ . That is, as long as the collector is positive with respect to the base, the electrons that reach the collector side of the base region will be swept into the collector and will register as collector current.

**The Base Current** Reference to Fig. 6.3 shows that the base current  $i_B$  is composed of two components. The first component  $i_{B1}$  is due to the holes injected from the base region into the emitter region. This current component is proportional to  $e^{v_{BE}/V_T}$ . The second component of base current,  $i_{B2}$ , is due to holes that have to be supplied by the external circuit in order to replace the holes lost from the base through the recombination process. Because  $i_{B2}$  is proportional to the number of electrons injected into the base, it also will be proportional to  $e^{v_{BE}/V_T}$ . Thus the total base current,  $i_B = i_{B1} + i_{B2}$ , will be proportional to  $e^{v_{BE}/V_T}$ , and can be expressed as a fraction of the collector current  $i_C$  as follows:

$$i_B = \frac{i_C}{\beta} \quad (6.2)$$

That is,

$$i_B = \left( \frac{I_S}{\beta} \right) e^{v_{BE}/V_T} \quad (6.3)$$

where  $\beta$  is a transistor parameter.

For modern *n*p*n* transistors,  $\beta$  is in the range 50 to 200, but it can be as high as 1000 for special devices. For reasons that will become clear later, the parameter  $\beta$  is called the **common-emitter current gain**.

The above description indicates that the value of  $\beta$  is highly influenced by two factors: the width of the base region,  $W$ , and the relative dopings of the base region and the emitter region,  $N_A/N_D$ . To obtain a high  $\beta$  (which is highly desirable since  $\beta$  represents a gain parameter) the base should be thin ( $W$  small) and lightly doped and the emitter heavily doped (making  $N_A/N_D$  small). For modern integrated circuit fabrication technologies,  $W$  is in the nanometer range.

**The Emitter Current** Since the current that enters a transistor must leave it, it can be seen from Fig. 6.3 that the emitter current  $i_E$  is equal to the sum of the collector current  $i_C$  and the base current  $i_B$ ; that is,

$$i_E = i_C + i_B \quad (6.4)$$

Use of Eqs. (6.2) and (6.4) gives

$$i_E = \frac{\beta + 1}{\beta} i_C \quad (6.5)$$

That is,

$$i_E = \frac{\beta + 1}{\beta} I_S e^{v_{BE}/V_T} \quad (6.6)$$

Alternatively, we can express Eq. (6.5) in the form

➤  $i_C = \alpha i_E \quad (6.7)$

where the constant  $\alpha$  is related to  $\beta$  by

➤  $\alpha = \frac{\beta}{\beta + 1} \quad (6.8)$

Thus the emitter current in Eq. (6.6) can be written

➤  $i_E = (I_S/\alpha) e^{v_{BE}/V_T} \quad (6.9)$

Finally, we can use Eq. (6.8) to express  $\beta$  in terms of  $\alpha$ , that is,

➤  $\beta = \frac{\alpha}{1 - \alpha} \quad (6.10)$

It can be seen from Eq. (6.8) that  $\alpha$  is a constant (for a particular transistor) that is less than but very close to unity. For instance, if  $\beta = 100$ , then  $\alpha \simeq 0.99$ . Equation (6.10) reveals an important fact: Small changes in  $\alpha$  correspond to very large changes in  $\beta$ . This mathematical observation manifests itself physically, with the result that transistors of the same type may have widely different values of  $\beta$ . For reasons that will become apparent later,  $\alpha$  is called the **common-base current gain**.

**Minority-Carrier Distribution** Our understanding of the physical operation of the BJT can be enhanced by considering the distribution of minority charge carriers in the base and the emitter. Figure 6.4 shows the profiles of the concentration of electrons in the base and holes in the emitter of an *n*p*n* transistor operating in the active mode. Observe that since the doping concentration in the emitter,  $N_D$ , is much higher than the doping concentration in the base,  $N_A$ , the concentration of electrons injected from emitter to base,  $n_p(0)$ , is much higher than the concentration of holes injected from the base to the emitter,  $p_n(0)$ . Both quantities are proportional to  $e^{v_{BE}/V_T}$ , thus

$$n_p(0) = n_{p0} e^{v_{BE}/V_T} \quad (6.11)$$

where  $n_{p0}$  is the thermal-equilibrium value of the minority-carrier (electron) concentration in the base region.

Next, observe that because the base is very thin, the concentration of excess electrons decays almost linearly (as opposed to the usual exponential decay, as observed for the excess holes in the emitter region). Furthermore, the reverse bias on the collector–base junction causes the concentration of excess electrons at the collector side of the base to be zero. (Recall that electrons that reach that point are swept into the collector.)

The tapered minority-carrier concentration profile (Fig. 6.4) causes the electrons injected into the base to diffuse through the base region toward the collector. This electron diffusion