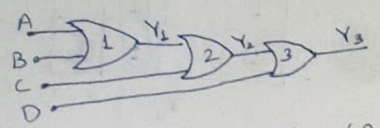
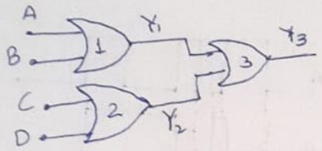
1. Implement a four-input OR gate using two-input OR gates only?

Ans1→ Fig (a) is showing one possible arrangement of 2-i/p OR gate
A, B, C, D are the logic inputs & Y_3 is the output



The o/p of OR gate 1 is $Y_1 = (A+B)$
The o/p of OR gate 2 is $Y_2 = (Y_1 + C) = (A+B+C)$
The o/p of OR gate 3 is $Y_3 = (Y_2 + D) = (A+B+C+D)$

→ Fig (b) showing another arrangement possible with 4-i/ps.



The o/p of OR gate 1 is, $Y_1 = (A+B)$
The o/p of OR gate 2 is, $Y_2 = (C+D)$
The o/p of OR gate 3 is, $Y_3 = Y_1 + Y_2 = (A+B+C+D)$

2. Simplify the following

a) $(A.B + C.D).[(\bar{A} + \bar{B}).(\bar{C} + \bar{D})]$

b) $(1 + L.M + L.\bar{M} + \bar{L}.M).[(L + \bar{M}).(\bar{L}.M) + (\bar{L}.\bar{M}).(L + M)]$

Ans2) a) $(A \cdot B + C \cdot D).[(\bar{A}+\bar{B}).(\bar{C}+\bar{D})]$

→ Let $(A \cdot B + C \cdot D) = X$

Then $(\bar{A}+\bar{B}).(\bar{C}+\bar{D}) = \bar{X}$

The given expression reduced to $X \cdot \bar{X}$

$\therefore$ $(A \cdot B + C \cdot D).[(\bar{A}+\bar{B}).(\bar{C}+\bar{D})] = 0$

b) $(1 + L \cdot M + L \cdot \bar{M} + \bar{L} \cdot M).[(L+\bar{M}).(\bar{L} \cdot M) + (\bar{L} \cdot \bar{M})(L+M)]$

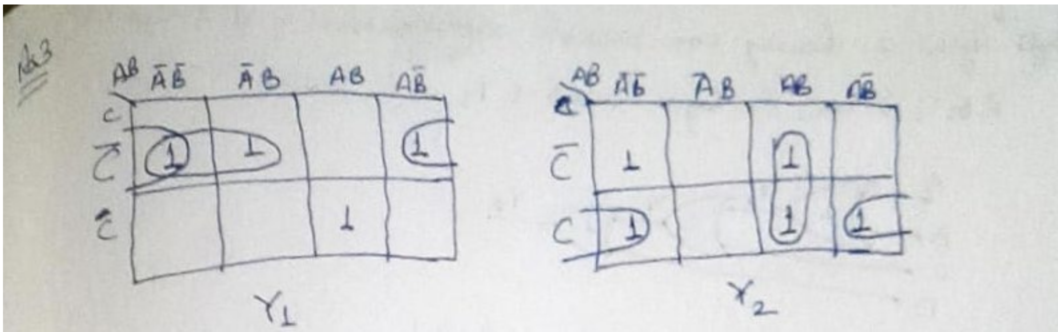
- (1+ Boolean Expression) = 1
- ($\bar{L}M$ is complement of $(L+\bar{M})$ & $\bar{L} \cdot \bar{M}$ is complement of $(L+M)$
- The given expression is $1 \cdot (0+0) = 0$

3. Using Karnaugh maps, write the minimized Boolean expressions for the output functions of a two-output logic system whose outputs Y1 and Y2 are given by the following Boolean functions:

$$Y_1 = \bar{A}.B.\bar{C} + A.\bar{B}.\bar{C} + A.B.C + \bar{A}.\bar{B}.\bar{C}$$

$$Y_2 = \bar{A}.\bar{B}.C + A.B.\bar{C} + A.\bar{B}.C + A.B.C$$

Ans 3



The minimized expressions for Y_1 & Y_2 are as follows

$$Y_1 = \bar{A}\bar{C} + \bar{B}.\bar{C} + A.B.C$$

$$Y_2 = A.B + \bar{B}.C + \bar{A}.\bar{B}.\bar{C}$$

4. For the half-adder circuit of Fig. 4(a), the inputs applied at A and B are as shown in Fig.4(b). Plot the corresponding SUM and CARRY outputs on the same scale.

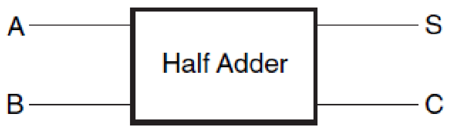


Fig. 4(a)

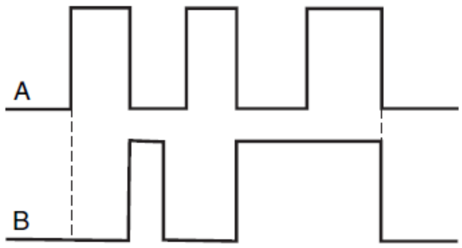
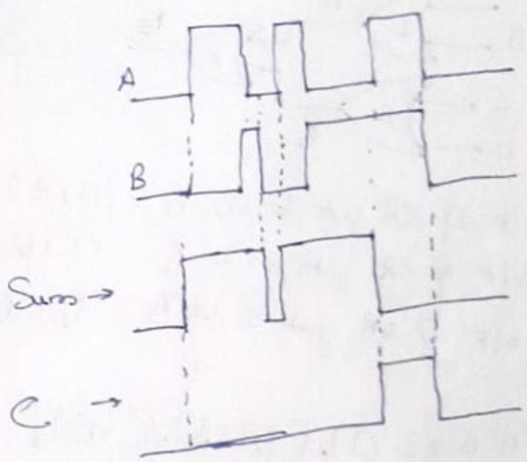


Fig. 4(b)

Ans 4: Half Adder.

A	B	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1



5. Write the simplified Boolean expressions for **DIFFERENCE** and **BORROW** outputs for the Fig. 5. **(HA- Half adder; HS- Half Subtractor)**

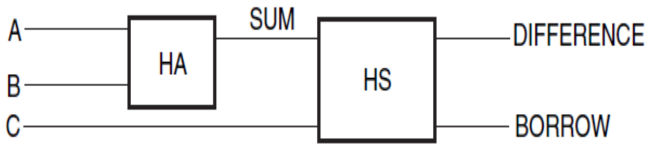


Fig.5

Let us assume that the two inputs to the half-subtractor circuit are X and Y, with X equal to the SUM output of the half-adder and Y equal to C. DIFFERENCE and BORROW outputs can then be expressed as follows:

$$\text{DIFFERENCE output} = X \oplus Y = \overline{X}.Y + X.\overline{Y} \quad \text{and} \quad \text{BORROW output} = \overline{X}.Y$$

Also, $X = \overline{A}.B + A.\overline{B}$ and $Y = C$.

Substituting the values of X and Y, we obtain

$$\begin{aligned}\text{DIFFERENCE output} &= (\overline{\overline{A}.B + A.\overline{B}}).C + (\overline{A}.B + A.\overline{B}).\overline{C} = (A.B + \overline{A}.\overline{B}).C + (\overline{A}.B + A.\overline{B}).\overline{C} \\ &= A.B.C + \overline{A}.\overline{B}.C + \overline{A}.B.\overline{C} + A.\overline{B}.\overline{C}\end{aligned}$$

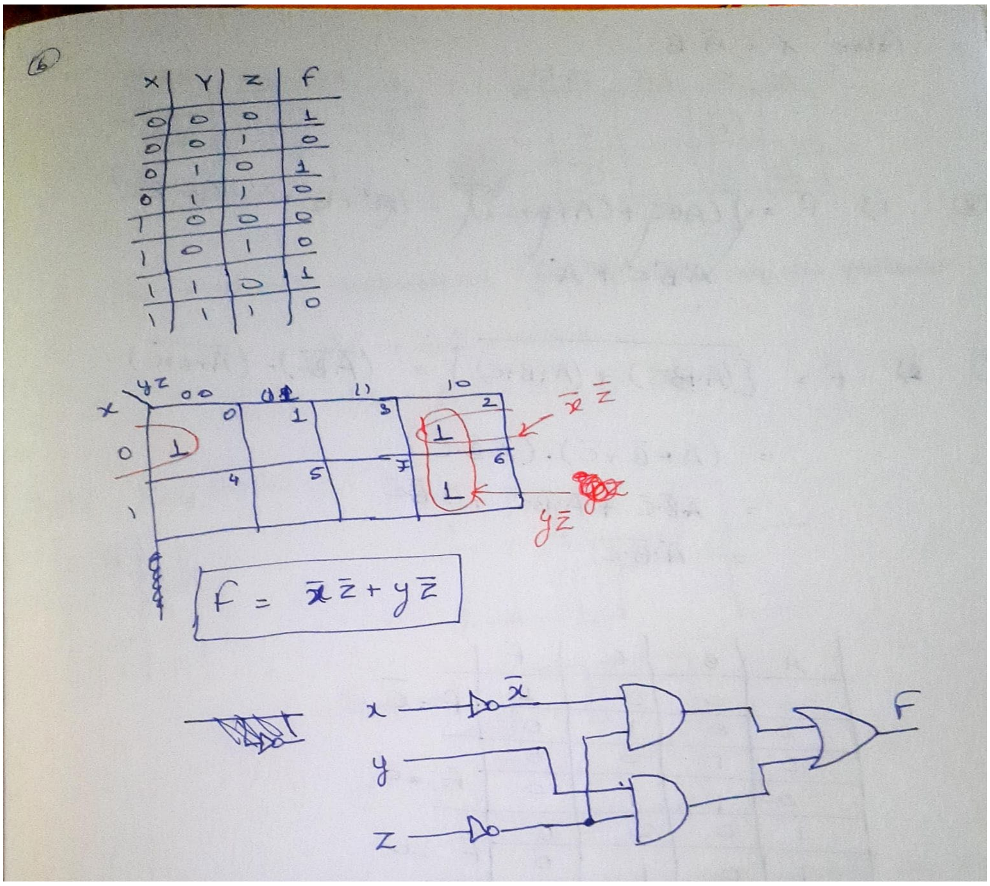
$$\text{BORROW output} = \overline{X}.Y = (\overline{\overline{A}.B + A.\overline{B}}).C = (A.B + \overline{A}.\overline{B}).C = A.B.C + \overline{A}.\overline{B}.C$$

6. a) Make a truth table for the Boolean function $F = \bar{x}.\bar{y}.\bar{z} + \bar{x}.y.\bar{z} + x.y.\bar{z}$

b) Simplify the above function to a minimum number of literals.

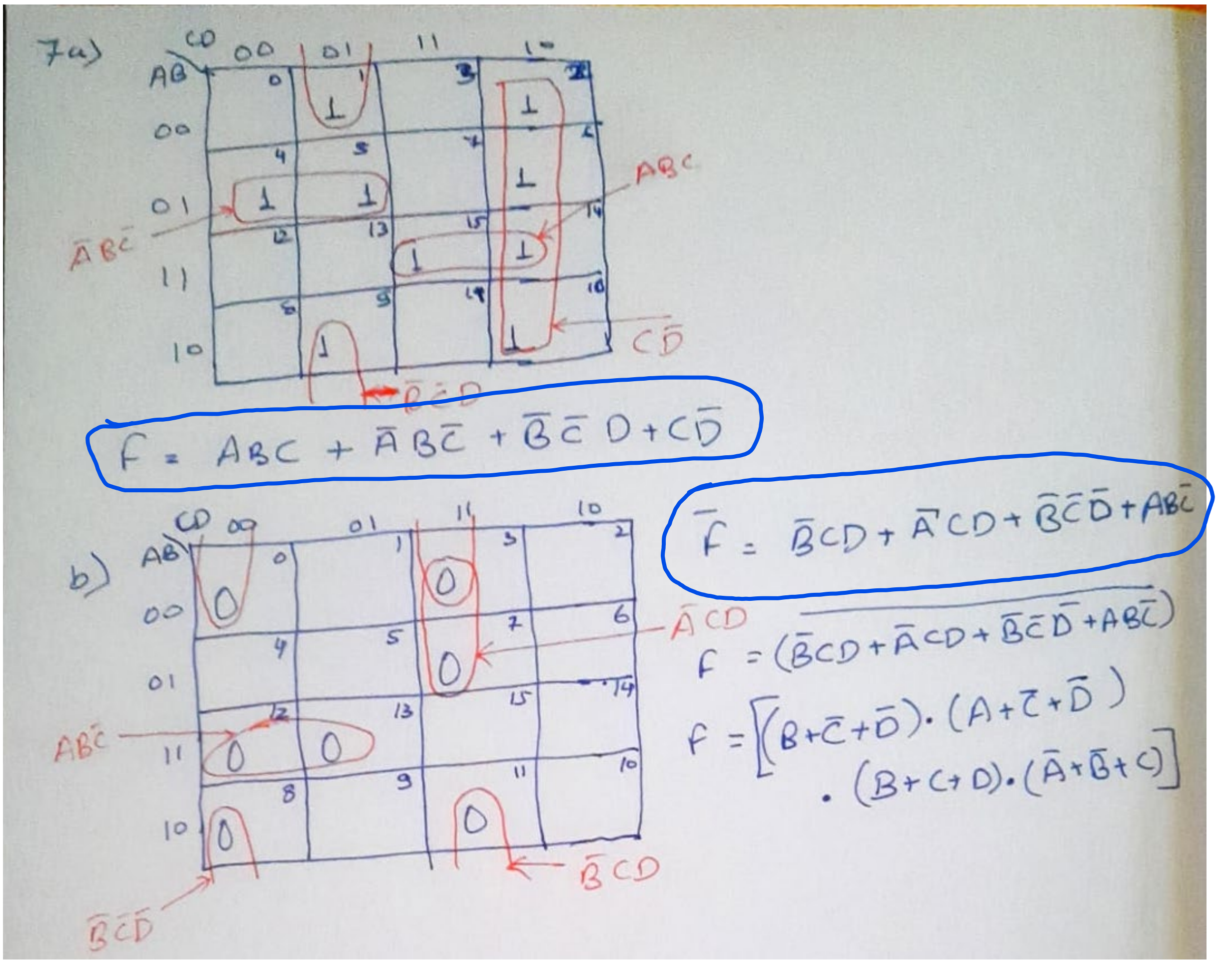
c) Now use Karnaugh map to simplify F.

d) Sow implementation of F using NOT, OR and AND gates. What is the total count of gates?

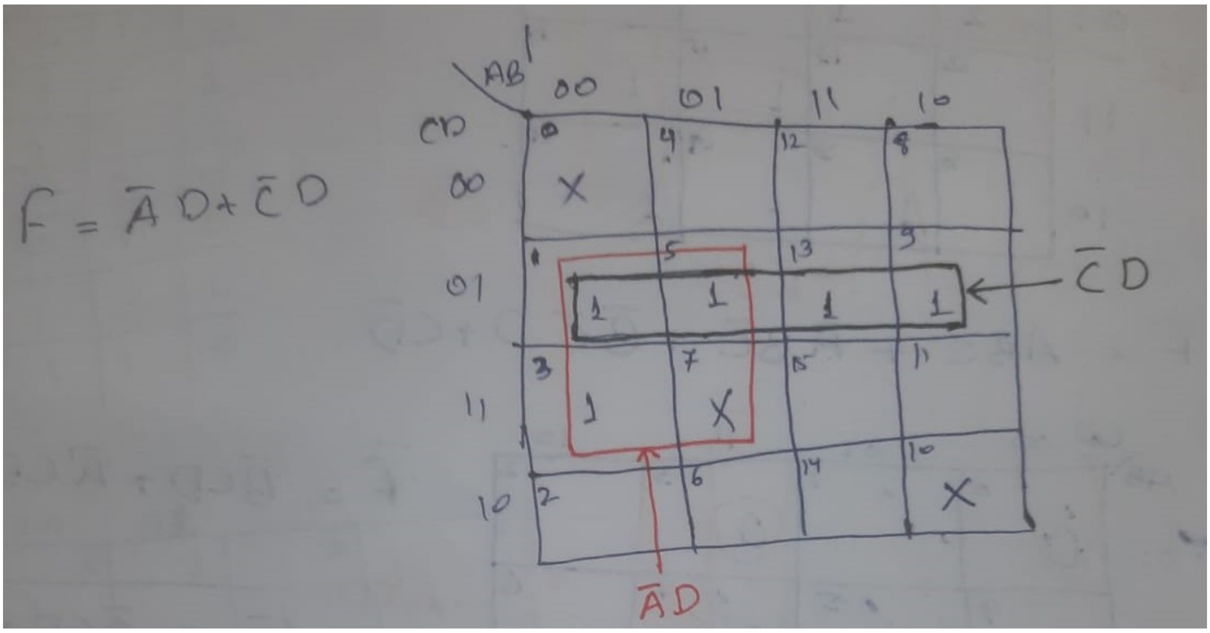


7. a) Minimize the following function using K-Map and write the minimized function in sum-of products form
$F(A, B, C, D) = \sum(1, 2, 4, 5, 6, 9, 10, 14, 15)$

b) Using K-map simplify the above function and expression it in product -of-sums form.



8. Minimize the following function using K-Map and write the minimized function in sum-of products form
$F(A, B, C, D) = \sum(1,3,5,9,13) + d(0,7,10)$

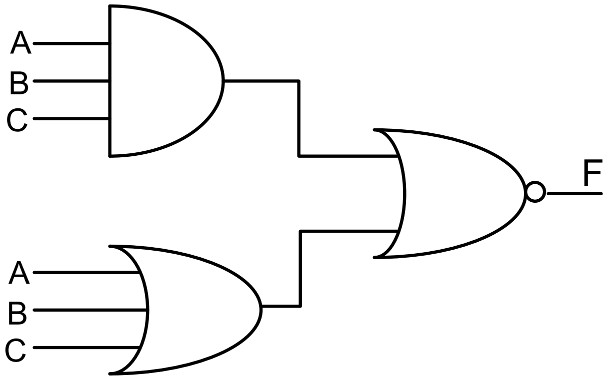


9. The logic diagram of the Boolean function is given below.

i) Analyze the diagram and write its truth table

ii) Analyze the diagram and write the Boolean function id sum-of-product form.

iii) Implement the function using 4-to-1 line multiplexer.



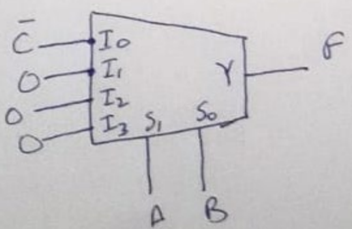
i) $F = \overline{[(A \cdot B \cdot C) + (A+B+C)]} = (\overline{ABC}) \cdot (\overline{A+B+C})$

$= (\bar{A} + \bar{B} + \bar{C}) \cdot (\bar{A} \cdot \bar{B} \cdot \bar{C})$

$= \bar{A}\bar{B} \cdot \bar{C} + \bar{A} \cdot \bar{B} \cdot \bar{C} + \bar{A} \cdot \bar{B}\bar{C}$

$= \bar{A} \cdot \bar{B} \cdot \bar{C}$

A	B	C	F	
0	0	0	1	$F = \bar{C}$
0	0	1	0	
0	1	0	0	$F = 0$
0	1	1	0	
1	0	0	0	$F = 0$
1	0	1	0	
1	1	0	0	$F = 0$
1	1	1	0	



10. Design an X-NOR gate (i.e. $F(x, y) = \bar{x}\bar{y} + xy$) using only 2-input NOR gates. You are given only x and y inputs. You are allowed to use only a maximum of FIVE 2-input NOR gates. Draw a clear circuit diagram.