Introduction to Electrical Engineering

Course Code: EE 103

Department: Electrical Engineering

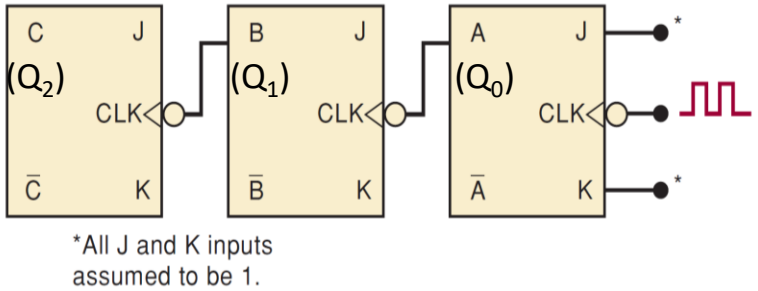
Instructor Name: B. G. Fernandes

E-mail id: bgf@ee.iitb.ac.in

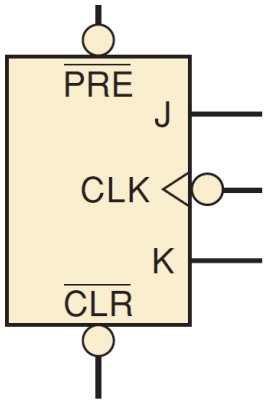
Review:

Asynchronous (Ripple) Counter

Outputs of all the Flip-Flops do not change simultaneously. Hence Asynchronous or ripple (Flip-Flops respond one after another).



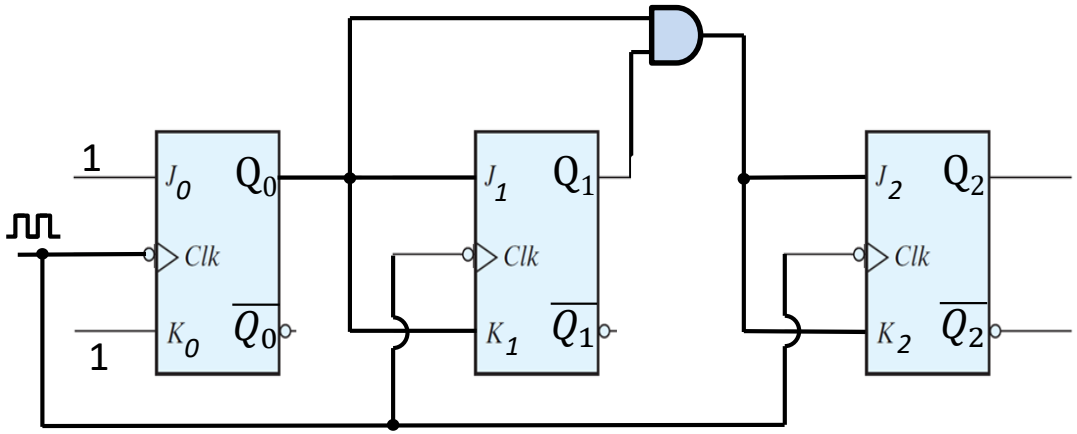
*All J and K inputs assumed to be 1.



J	K	*Clk*	*Q*
0	0	↓	Q_o(Hold)
1	0	↓	1
0	1	↓	0
1	1	↓	toggle

Synchronous Counter (Parallel Counter):

- All Flip-Flops receive clock simultaneously.
- Some means must be used to control when an Flip-Flop should toggle and when it remains unaffected by a clock pulse.



Design Procedure: Mod-8 Synchronous Counter

1. Determine the desired number of bits (Flip-Flops) and the possible states .

Q_2	Q_1	Q_0				
0	0	0				
0	0	1				
0	1	0				
0	1	1				
1	0	0				
1	0	1				
1	1	0				
1	1	1				
0	0	0				

Design Procedure: Mod-8 Synchronous Counter

2. Prepare a table that lists all the present states and their next state.

Q_2	Q_1	Q_0	Q_{2+}	Q_{1+}	Q_{0+}			
0	0	0	0	0	1			
0	0	1	0	1	0			
0	1	0	0	1	1			
0	1	1	1	0	0			
1	0	0	1	0	1			
1	0	1	1	1	0			
1	1	0	1	1	1			
1	1	1	0	0	0			
0	0	0	0	0	1			

N^{th} state	$(N+1)^{th}$ state	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Design Procedure: Mod-8 Synchronous Counter

3. Add two column per Flip-Flop (one for each J and K). There will be six columns for each 'PRESENT' state, indicate the levels requires at each J and K input in order to produce the transition to the 'NEXT' state

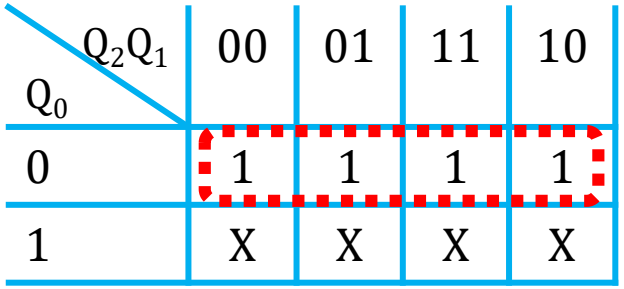
Q_2	Q_1	Q_0	Q_{2+}	Q_{1+}	Q_{0+}	J_0	K_0	J_1	K_1	J_2	K_2
0	0	0	0	0	1	1	X	0	X	0	X
0	0	1	0	1	0	X	1	1	X	0	X
0	1	0	0	1	1	1	X	X	0	0	X
0	1	1	1	0	0	X	1	X	1	1	X
1	0	0	1	0	1	1	X	0	X	X	0
1	0	1	1	1	0	X	1	1	X	X	0
1	1	0	1	1	1	1	X	X	0	X	0
1	1	1	0	0	0	X	1	X	1	X	1
0	0	0	0	0	1						

N^{th} state	$(N+1)^{th}$ state	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Design Procedure: Mod-8 Synchronous Counter

4. Design the logic circuit needed to generate the levels required at each J&K input

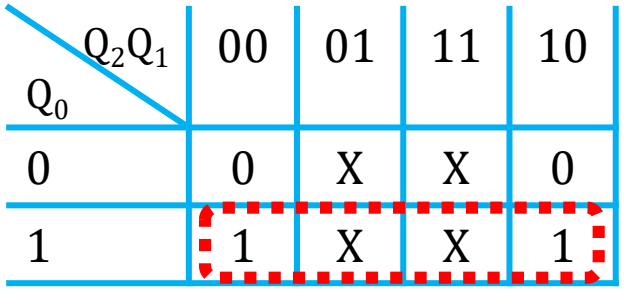
J_0



Q_0 \ Q_2Q_1	00	01	11	10
0	1	1	1	1
1	X	X	X	X

$J_0=1 (\text{or } J_0=\overline{Q_0})$

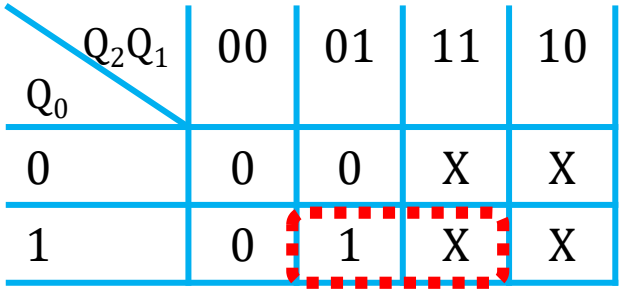
J_1



Q_0 \ Q_2Q_1	00	01	11	10
0	0	X	X	0
1	1	X	X	1

$J_1=Q_0$

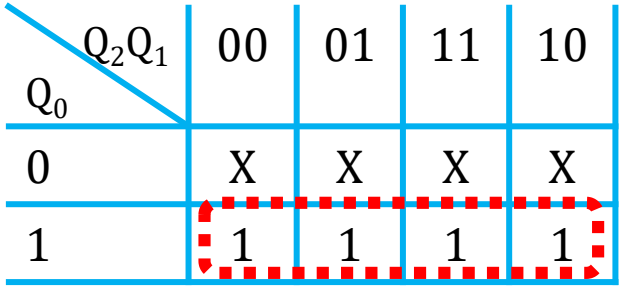
J_2



Q_0 \ Q_2Q_1	00	01	11	10
0	0	0	X	X
1	0	1	X	X

$J_2=Q_0Q_1$

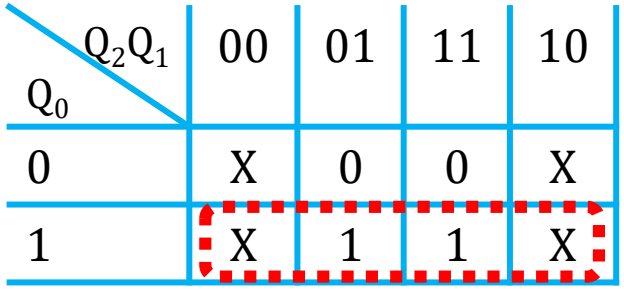
K_0



Q_0 \ Q_2Q_1	00	01	11	10
0	X	X	X	X
1	1	1	1	1

$K_0=1 (\text{or } K_0=Q_0)$

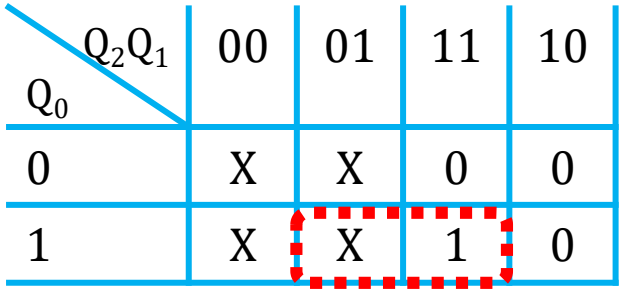
K_1



Q_0 \ Q_2Q_1	00	01	11	10
0	X	0	0	X
1	X	1	1	X

$K_1=Q_0$

K_2

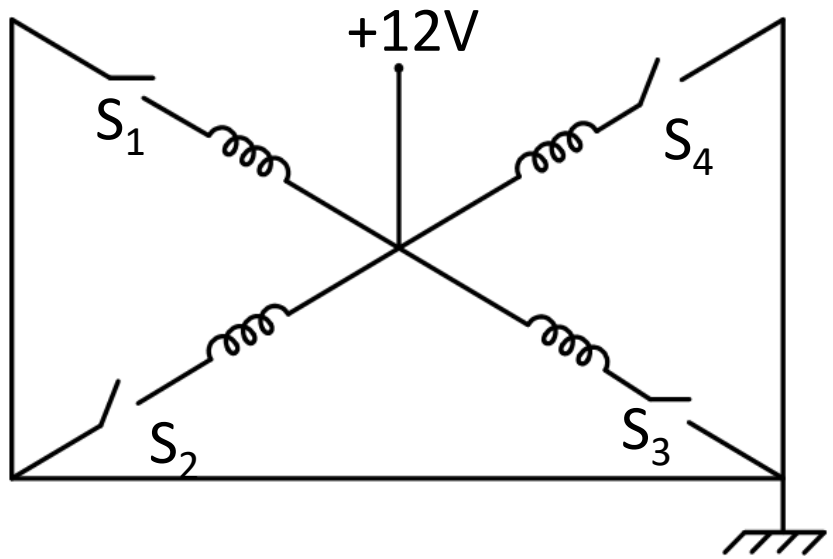


Q_0 \ Q_2Q_1	00	01	11	10
0	X	X	0	0
1	X	X	1	0

$K_2=Q_0Q_1$

Problem:

The figure shown is used for generating a magnetic field rotating in steps of 90^o by selectively switching the currents in 4 coils by means of switches S_1, S_2, S_3 & S_4.



S_1 ON & S_3 OFF if $Q_1 = 0$. S_1 OFF & S_3 ON if $Q_1 = 1$.

S_2 ON & S_4 OFF if $Q_2 = 0$. S_2 OFF & S_4 ON if $Q_2 = 1$.

The sequence for rotating the field in counter clockwise direction is given below

Q_2	Q_1	Direction of field
0	0	←
0	1	↓
1	1	→
1	0	↑

EXCITATION TABLE

Q_N	Q_{N+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

PRESENT STATE		NEXT STATE					
Q_2	Q_1	Q_{2+}	Q_{1+}	J_1	K_1	J_2	K_2
0	0	0	1	1	X	0	X
0	1	1	1	X	0	1	X
1	1	1	0	X	1	X	0
1	0	0	0	0	X	X	1

for J1

Q_1 \ Q_2	0	1
0	1	0
1	X	X

$J_1 = \overline{Q_2}$

for K1

Q_1 \ Q_2	0	1
0	X	X
1	0	1

$K_1 = Q_2$

for J2

Q_1 \ Q_2	0	1
0	0	X
1	1	X

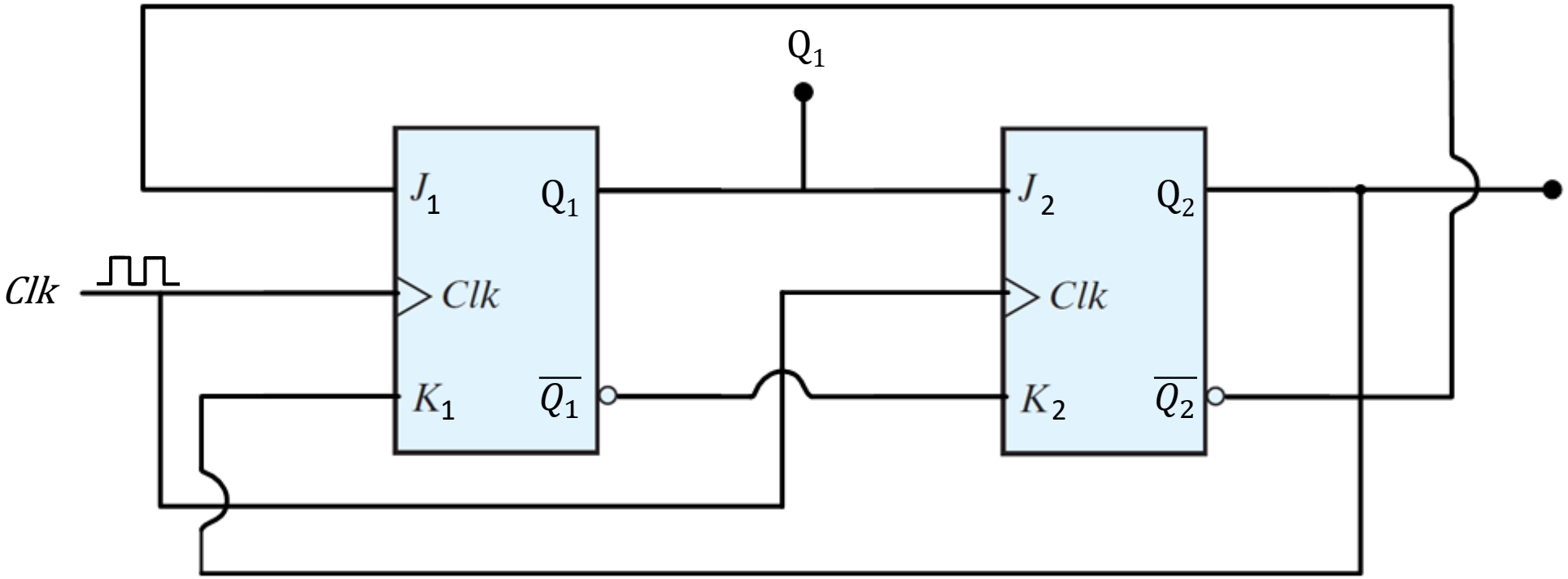
$J_2 = Q_1$

for K2

Q_1 \ Q_2	0	1
0	X	1
1	X	0

$K_2 = \overline{Q_1}$

Logic Realisation:



$$J_1 = \overline{Q_2} \qquad J_2 = Q_1$$

$$K_1 = Q_2 \qquad K_2 = \overline{Q_1}$$

Interfacing with the Analog World

Most physical variables are analog in nature.

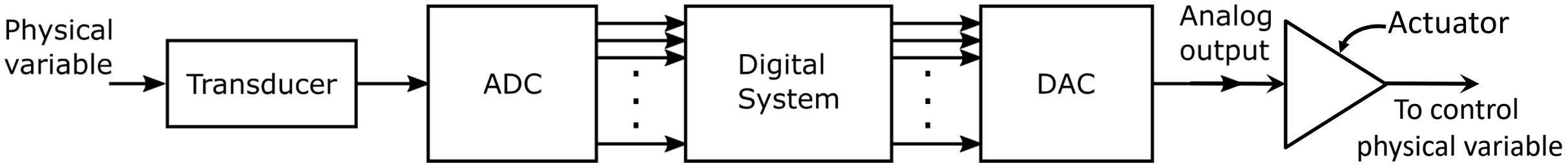
Transducer ⇒ Convert the physical variable to an electrical variable (solar cell, photodiode).

Analog to Digital Converter

ADC ⇒ Electrical output of transducer is converted to equivalent digital value.

8 bit ADC ⇒ output is digital code of 8 bits.

12 bit ADC ⇒ output is digital code of 12 bits.



ADCs and DACs

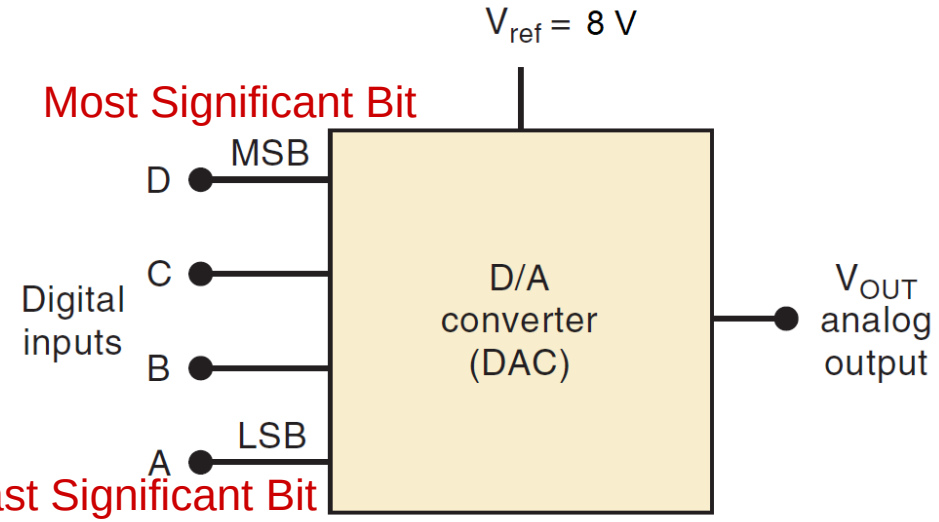
Functions as an interface between computer(digital) and the real(analog) world.

D/A Conversion : It is the process of taking a value represented in digital code and converting it to a voltage or current that is proportional to the digital value.

⇒ Input for a voltage reference. V_{ref}

⇒ This is used to determine full scale output
or maximum value that D/A can produce.

For each input number ⇒ unique output



D	C	B	A	V_{OUT}
0	0	0	0	0 V
0	0	0	1	0.5 V
.	.	.	.	
.	.	.	.	
.	.	.	.	
1	1	1	1	7.5 V

D/A Conversion

- V_{ref} → used to define full scale reading (FSR)

0 0 0 0 → 0 V
1 1 1 1 → 7.5 V
} 16 different binary numbers → 16 different analog values

MAX → 7.5 V

Example:
If 10100 → gives output of 10 mV,
Then 11101 → ???

10100 → $(20)_{\text{decimal}}$ → 10 mV
11101 → $(29)_{\text{decimal}}$ → $\frac{29}{20}$ 10 mV
→ 14.5 mV

D/A Conversion Resolution

- Output changes in steps ⇒ Not strictly analog
- If the no. of bits ↑, step size ↓, ⇒ Resolution can be improved

Resolution: Smallest change that can occur in the analog output for a change in digital input.

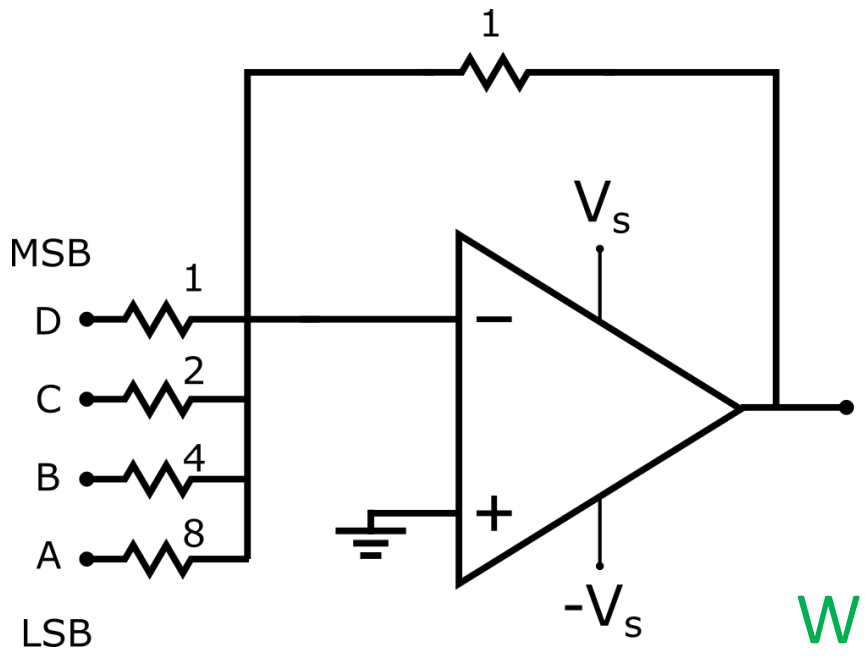
For an N-bit DAC ⇒ there are 2^N different levels

⇒ No. of steps is $(2^N - 1)$

$$\text{Resolution} = \frac{FSR}{2^N - 1}$$

Simple D/A circuit

- Inputs – 0 or 1 , 0 or 5 V



Input resistors are binary weighted!

For 12 bit DAC: If MSB = 1kΩ

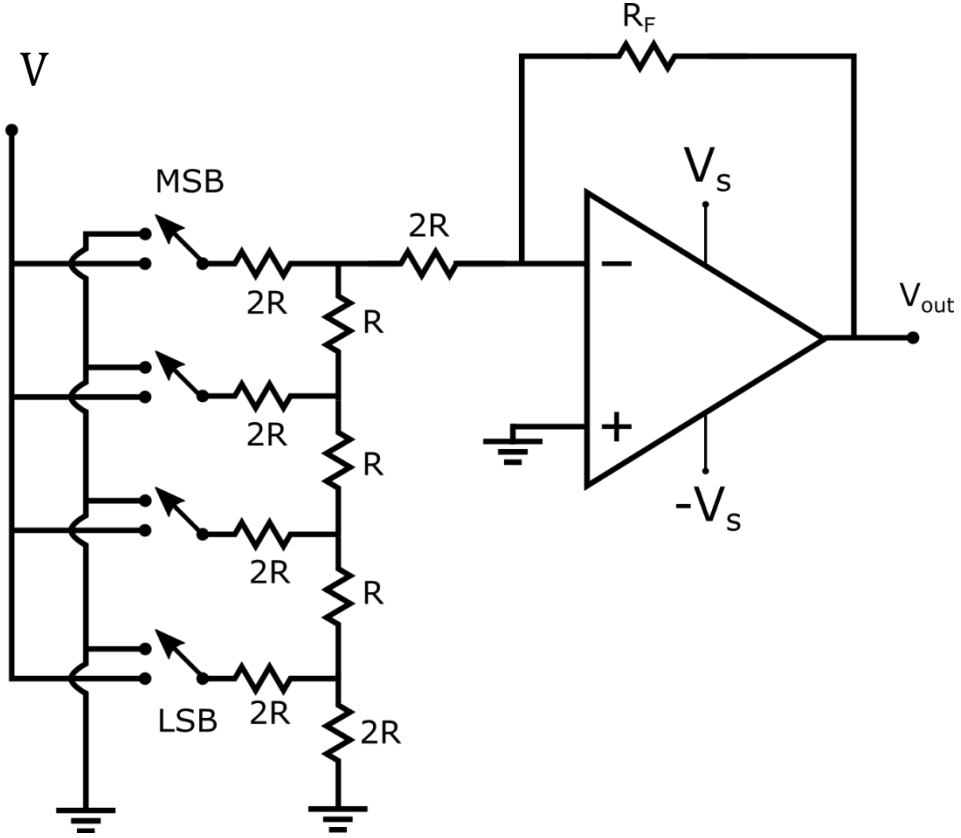
⇒ LSB > 2MΩ

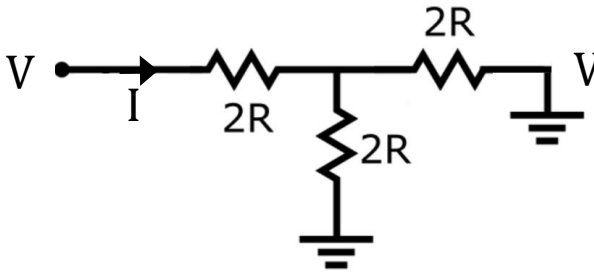
$$V_{out} = -\left(V_D + \frac{V_C}{2} + \frac{V_B}{4} + \frac{V_A}{8}\right)$$

What happens if feedback resistor R_F is reduced?

- Output ∝ weighted sum of the digital inputs
- Resolution of the D/A ⇒ weights of LSB = $\frac{1}{8}$ 5 V = 0.625 V

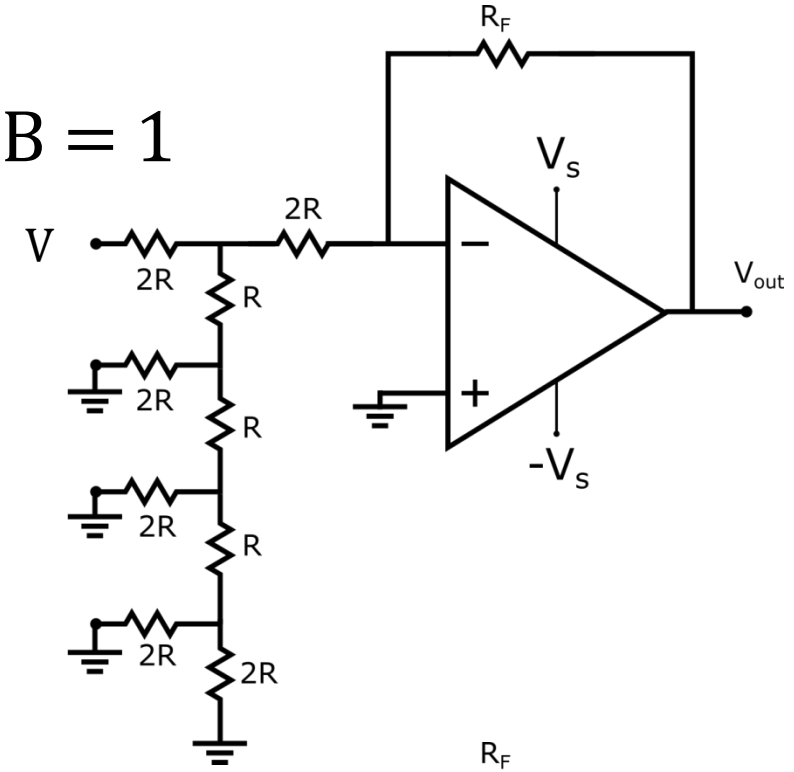
R-2R Ladder D/A

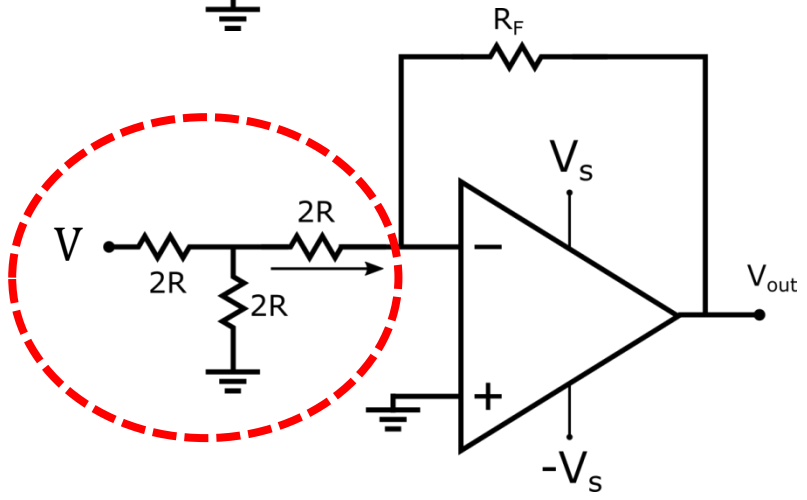




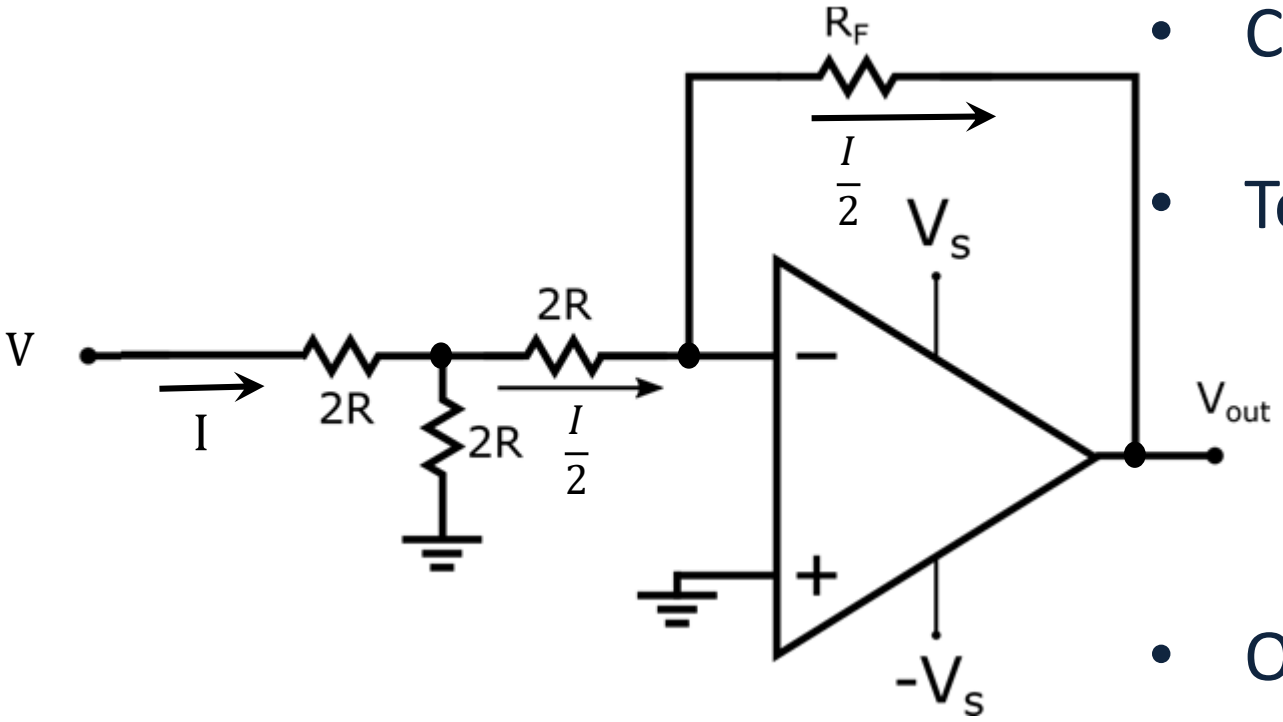
$$\therefore I = \frac{V}{3R}$$

Only MSB = 1





R-2R Ladder D/A



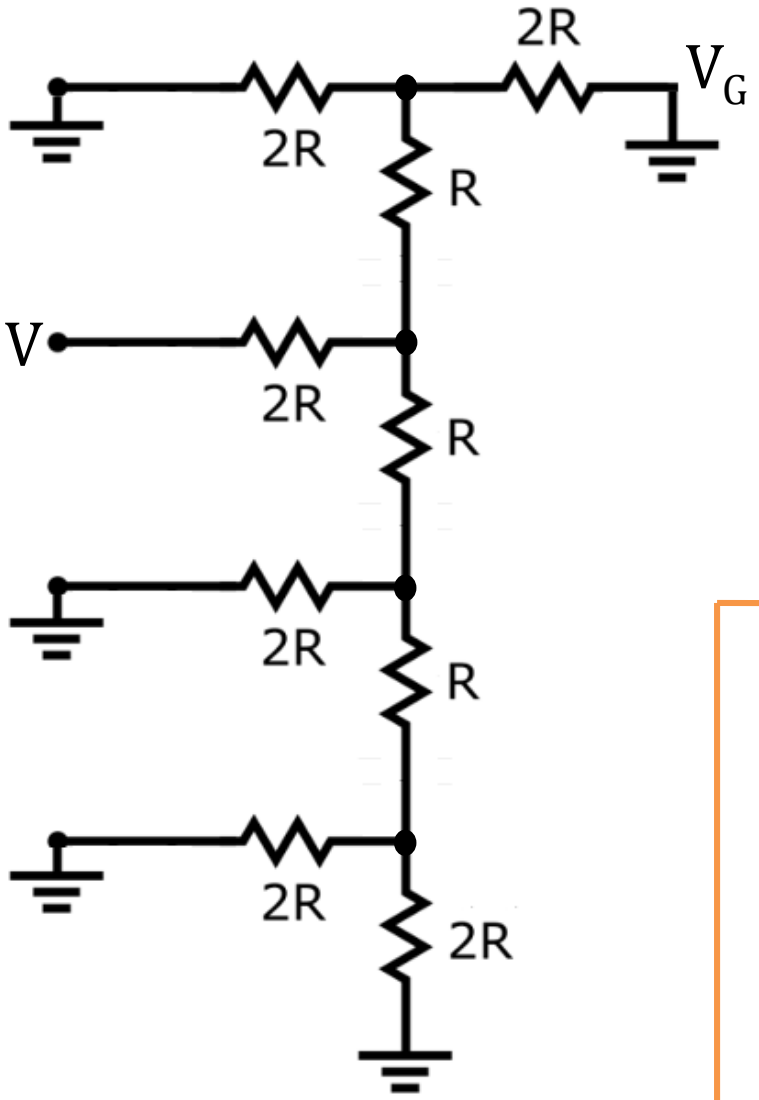
- Current in $R_F = \frac{I}{2}$, where $I = \frac{V}{3R}$
- Current due to II^{nd} bit $= \frac{I}{4}$ (See next page for derivation)
- Total current due to all bits

$$= \frac{I}{2} + \frac{I}{4} + \frac{I}{8} + \frac{I}{16}$$

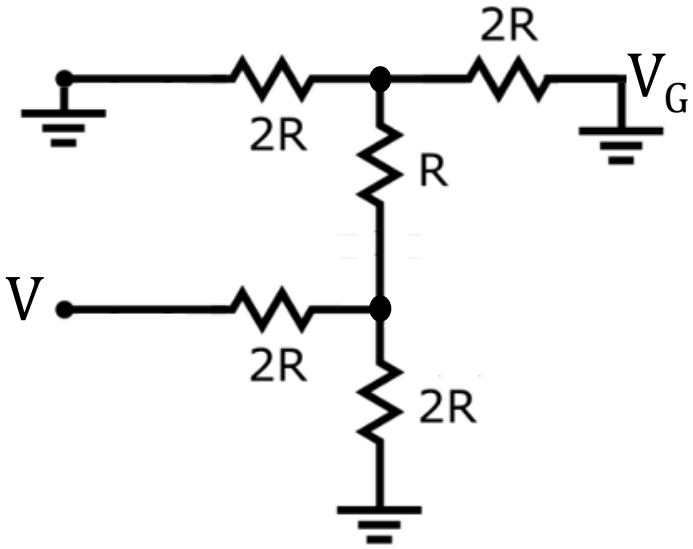
$$= \frac{I}{2}\left[1 + \frac{1}{2} + \frac{1}{2^2} + \frac{1}{2^3}\right]$$

- Output $= V_O = \frac{-R_F I}{2}\left[1 + \frac{1}{2} + \frac{1}{2^2} + \frac{1}{2^3}\right]$

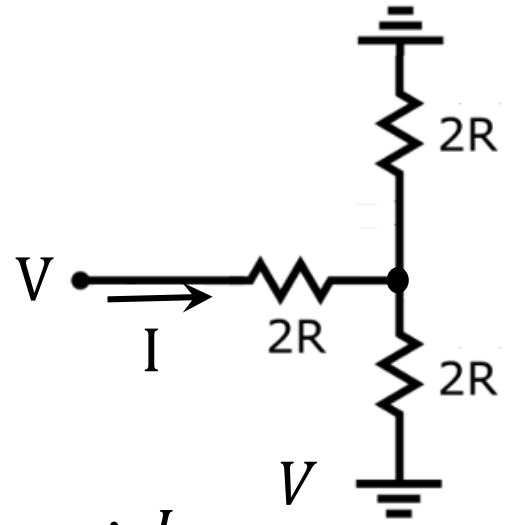
Assume all left nodes to be at GND and calculate the current through each of the bits individually using R equivalent and add all of them in the end.



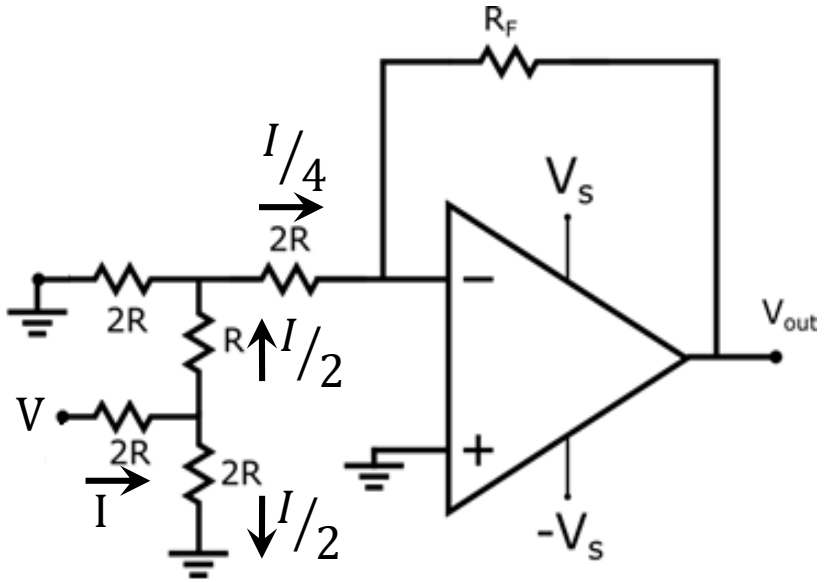
=



=



$$\therefore I = \frac{V}{3R}$$

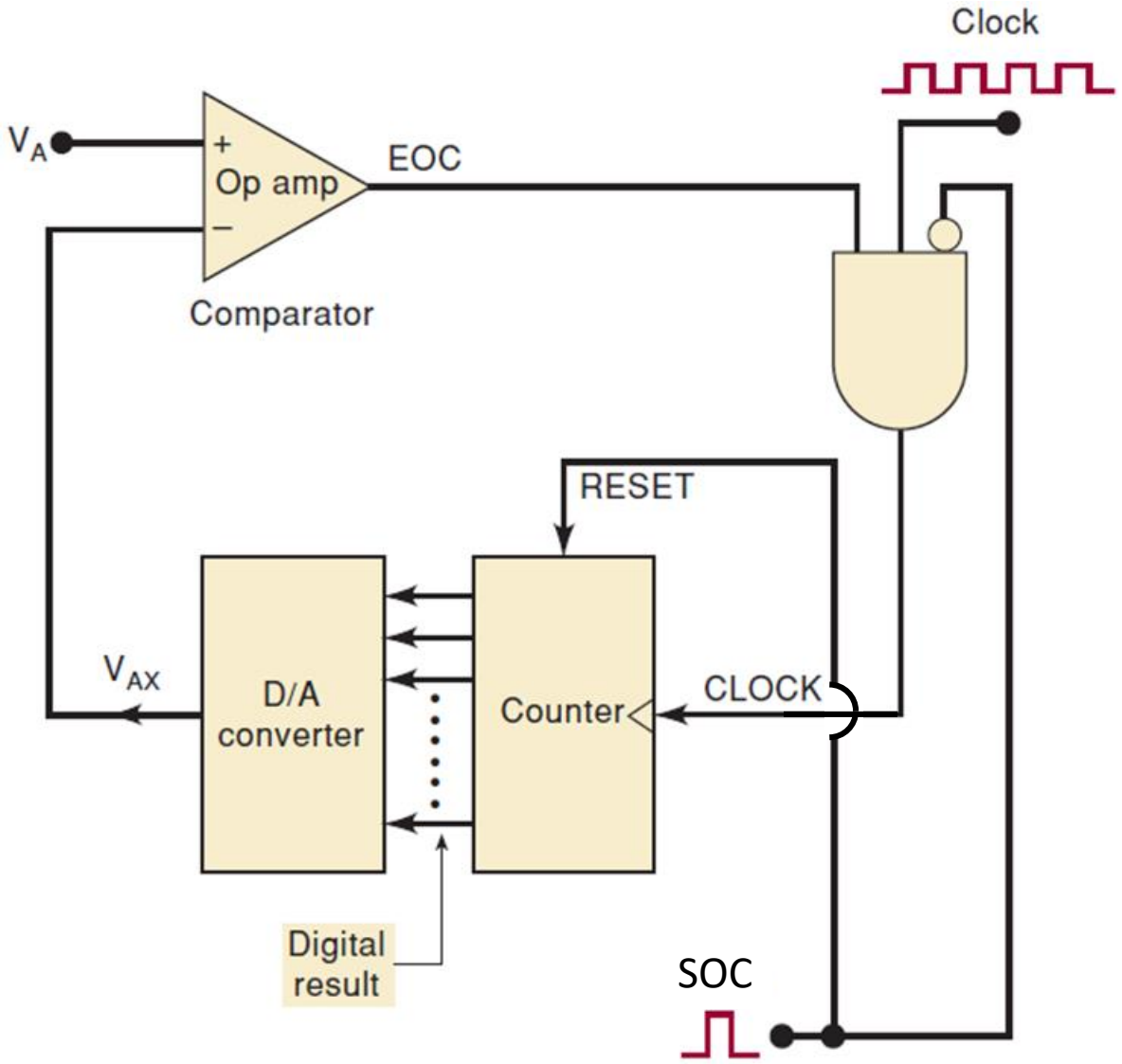


$I_1 \Rightarrow$ current through 'R_F'?

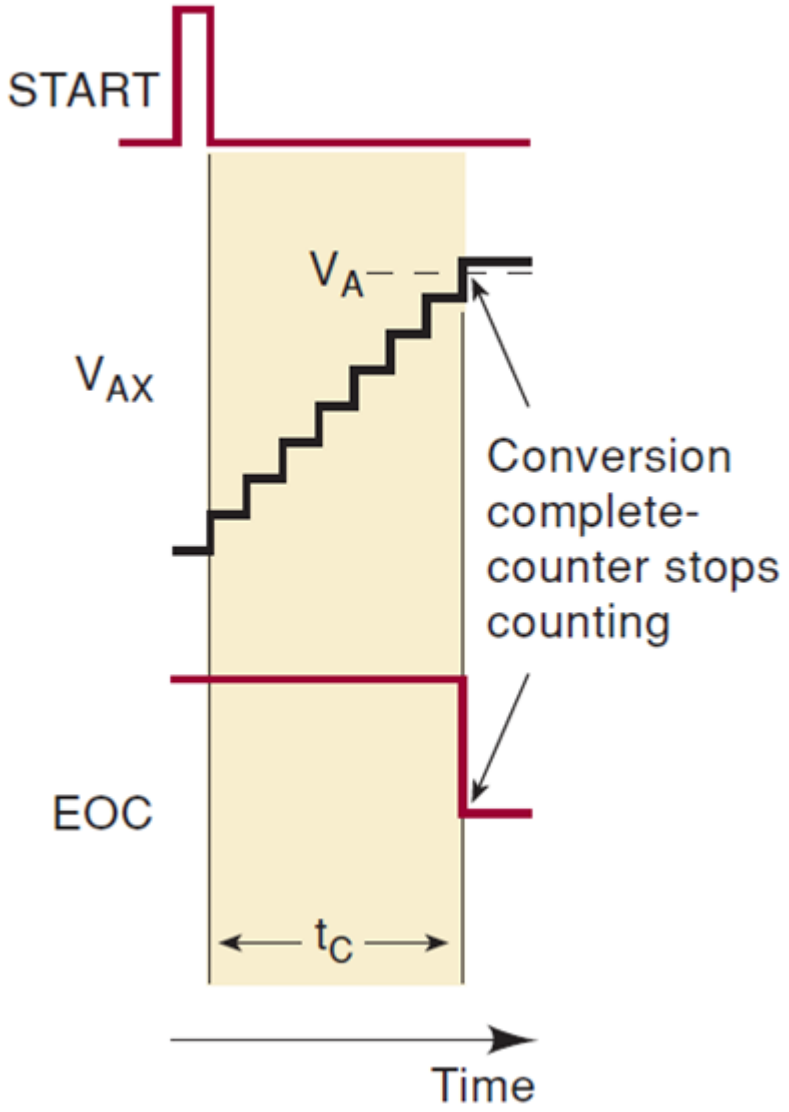
Simple ADC

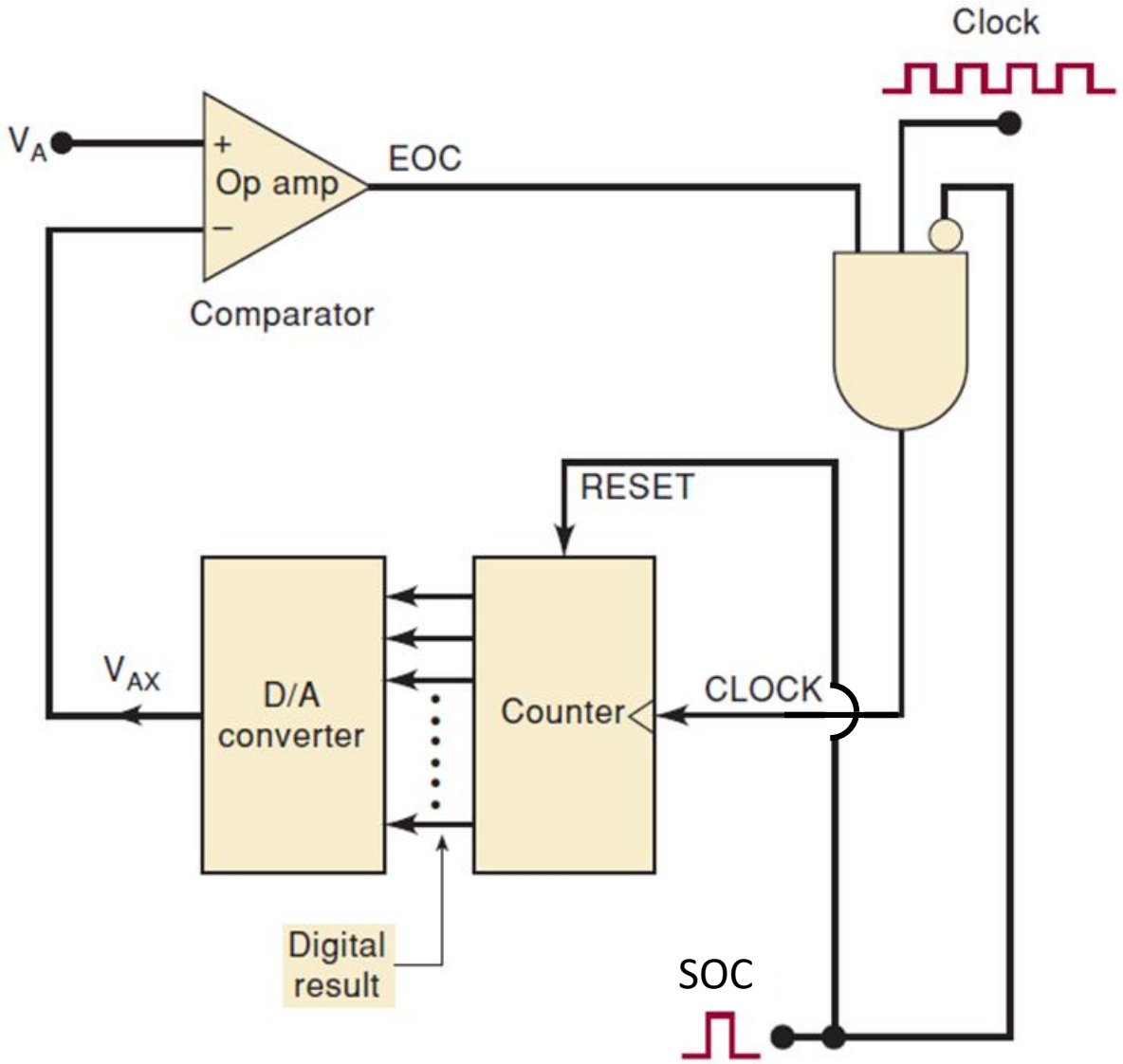
System on a Chip

- Apply SOC =1 ⇒ Reset the Counter. Also the clock gets disabled for a short duration.
- All Outputs of the converter = 0
- $V_{AX} = 0$
- D/A output connected to $-ve$ input of comparator ⇒ $\mathrm{EOC} = 1$, till $V_{AX} < V_A$.
- Output of 3-input AND is CLOCK signal
- At every CLOCK signal, counter output ↑, 000…0 – 000…1
- D/A output ↑ in steps
- If $V_{AX} < V_A$, $\mathrm{EOC} = +\mathrm{ve}\ (1)$
- As soon as $V_{AX} > V_A$,
  $\mathrm{EOC} = -\mathrm{ve}\ (0)$



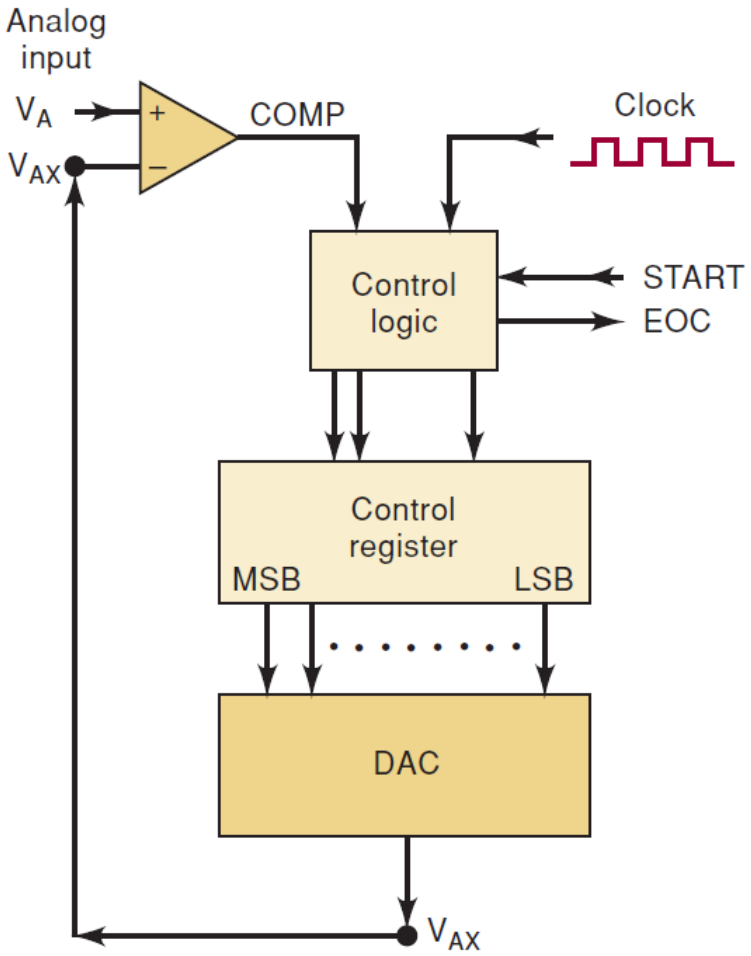
Simple ADC

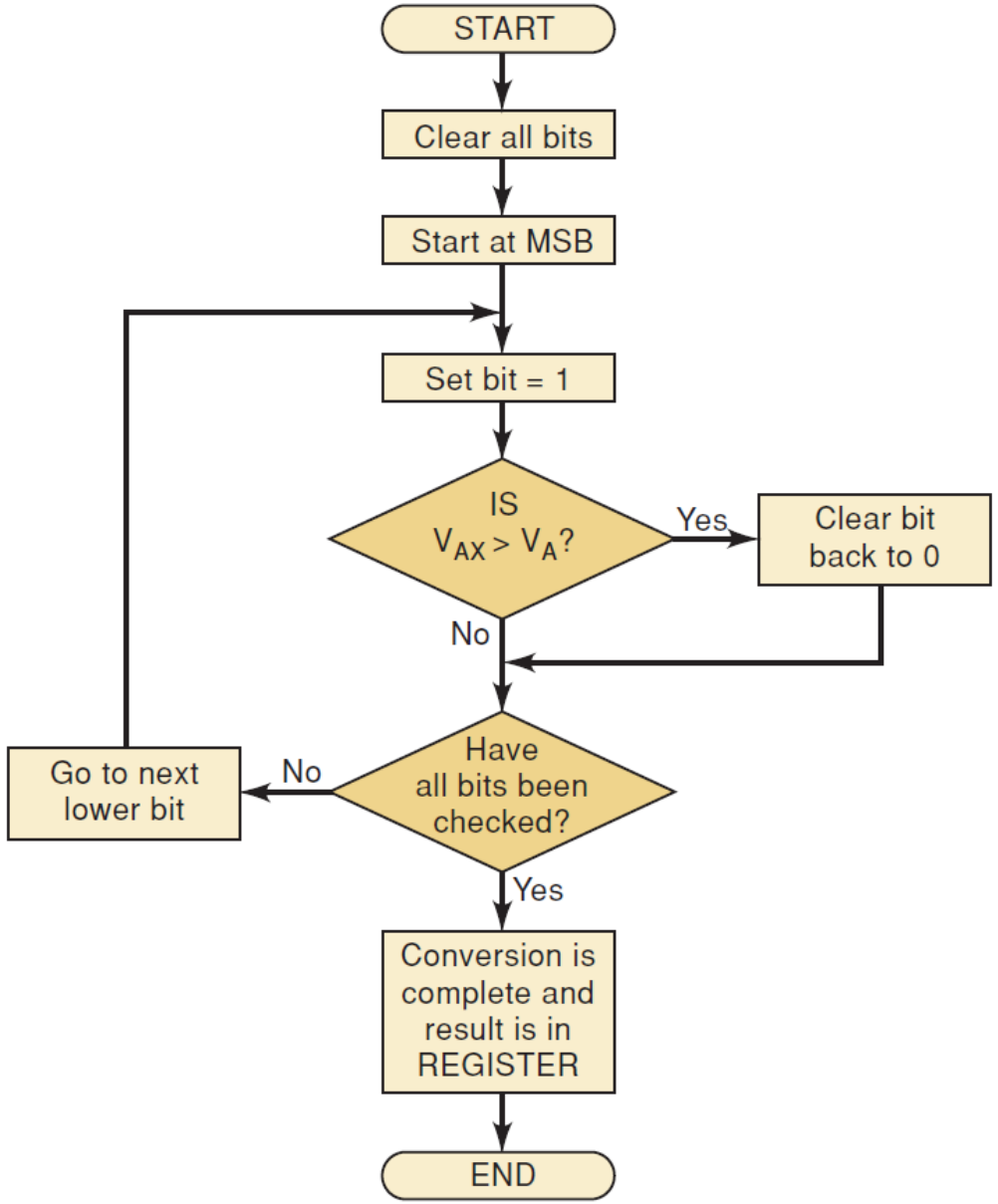

START
V_A
V_{AX}
Conversion complete- counter stops counting
EOC
t_C
Time


Clock
V_A
+
Op amp
−
EOC
Comparator
RESET
V_{AX}
D/A converter
Counter
CLOCK
Digital result
SOC

Successive Approximation ADC

- Most widely used.
- Much shorter conversion time than precision ADC.





Successive Approximation ADC