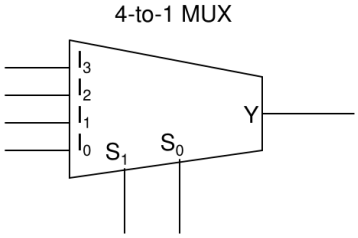
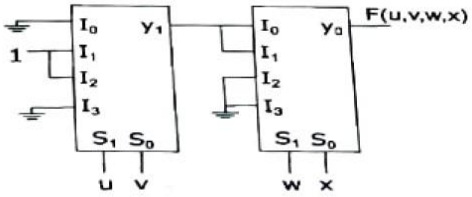
**1.** Write the Truth table for a Full Subtractor. Implement its DIFF and BORROW outputs using only 4-to-1 Mux, (4-to-1 MUX block diagram shown in Fig.3). You may assume that the true and complement forms of the input variables are available.




**2.** A 4 variable Boolean function is realized using 4 x 1 multiplexers as shown in figure. Determine boolean expression of

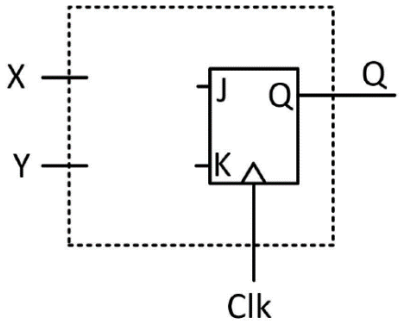
(a) Output (y1) of 1" multiplexer in terms of u and v

(b) Output of second multiplexer in terms of u, v, w & x.




**3.** X and Y are the inputs to a flip flop and Q is its output. The truth table for this flip flop is given below. How will you realize this flip- flop using J-K flip flop.

| X | Y | Q |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | $Q_0$ |
| 1 | 0 | Toggle |
| 1 | 1 | 0 |




**4.**

The circuit shown in figure uses four JK flip flops with negative edge triggered clock. JK inputs of all flip flops are made high and 1 kHz clock is applied to $clk_0$

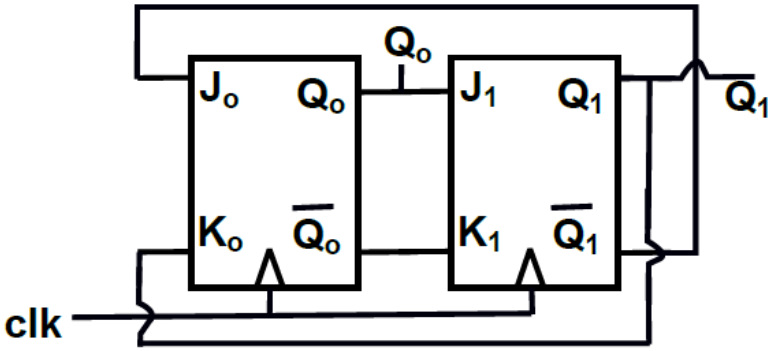
a. Assume that all outputs are cleared initially. Write the truth table for $Q_3$(MSB), $Q_2$, $Q_1$, $\bar{Q}_0$, $Q_0$ and decimal equivalent of $(Q_3Q_2Q_1Q_0)$ for each clock pulse. (2)

b. Draw the waveforms of output $Q_0$, $Q_1$, $Q_2$, $Q_3$ in response to the $clk_0$ (3)

c. Sketch on the timescale, the resulting waveform of the DAC output voltage $V_0$, the full-scale output of the DAC is 7.5V (3)

5. Assume that all the outputs are cleared prior to occurrence of first rising edge of the clock determine the ratio of $F_{out}/F_{Clk}$.
Where $F_{out}$ is the frequency of output and $F_{Clk}$ is the frequency of the clock.

6. In a sequential circuit, the initial state (before the 1st clock pulse) of the circuit is $Q_1Q_0$ = 00. Write down the truth table for the first five clock pulses and therefore what would be the state ($Q_1Q_0$) at the end of 33rd clock pulse. Note that $J_0 = \overline{Q_1}$, $K_0 = Q_1$, $J_1 = Q_0$, $K_1 = \overline{Q_0}$ .




7. Design a modulo-3 synchronous UP counter using –ve edge triggered JK flip-flops, with the sequence of states (BA): 00, 01, 10, 00, …. If the state 11 comes the next state should be 00. Give all the design steps, i.e. the table of present states and the required JK inputs for the next state, and the K map minimizations for the J and K inputs of the flip-flops.

8. A counter circuit is shown below. The Clear inputs of the flip-flops are active-low type n. Analyze the circuit and answer the following questions.

a) Write the counter sequence of stable states.
b) Based on the answer (a) above, specify whether it is an UP counter or a DOWN counter.
c) What are the limitations of the above counter? Write two limitations and briefly justify your answer.
d) Sketch the timing diagram of the counter, i.e. the A, B, C (i.e. $Q_A$, $Q_B$ and $Q_C$) outputs of the counter with respect to the CLOCK for at least 8 clock cycles.

9. Design a synchronous mod-8 down counter (CBA states: 111, 110, 101, 100, 011, 010, 001, 000, 111,…) using positive-edge triggered JK flip-flops.

i) Show your design using a table with the present states ($Q_n$), required J, K inputs, and the next states ($Q_{n+1}$).
ii) Using K-maps obtain minimized Boolean expressions for the J, K inputs of the flip-flops.
iii) Draw the final circuit diagram.

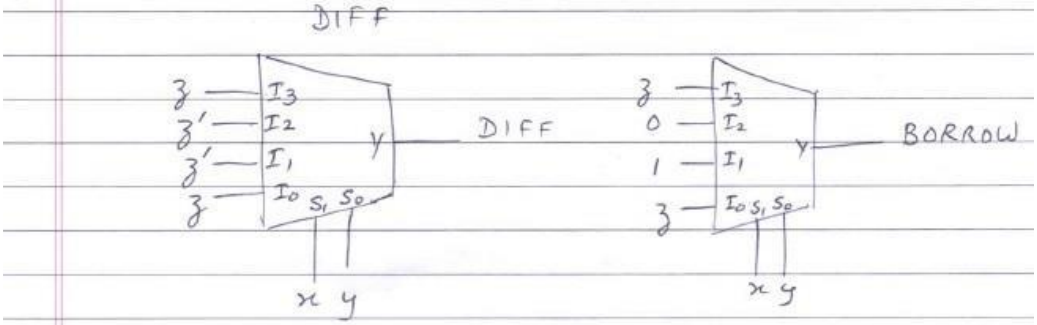
**Solution Q1.**

Full Subtractor

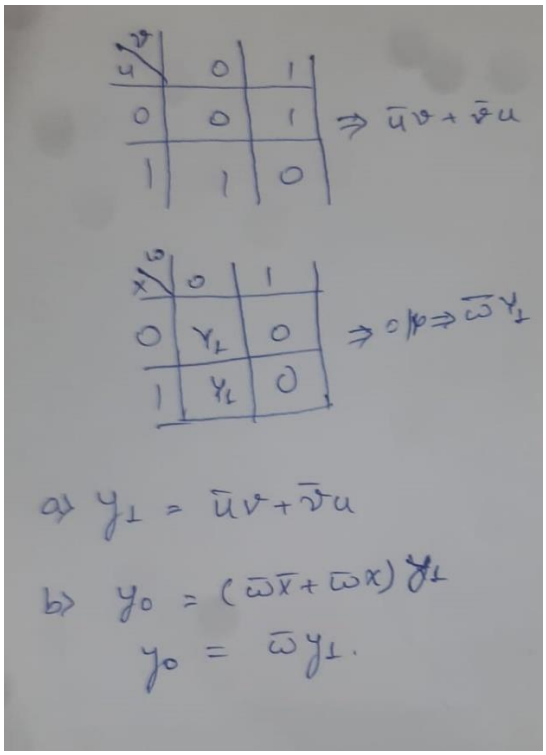
| Minuend x | Subtrahend y | Borrow IN z | DIFF | BORROW |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 |

$I_0 = z$, $I_1 = z'$, $I_2 = z'$, $I_3 = z$ for DIFF

$I_0 = z$, $I_1 = 1$, $I_2 = 0$, $I_3 = z$ for BORROW

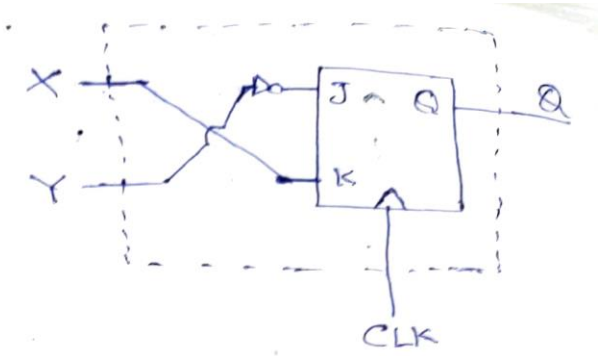



**Solution 2.**

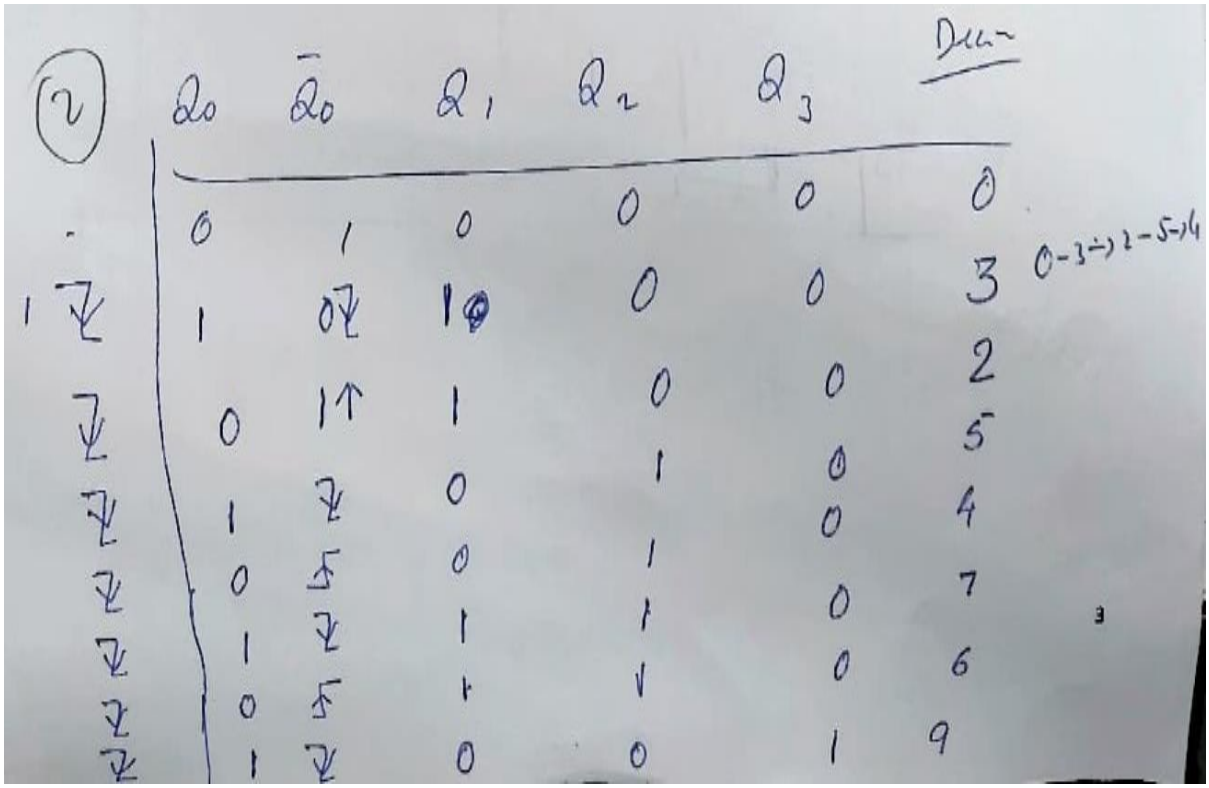


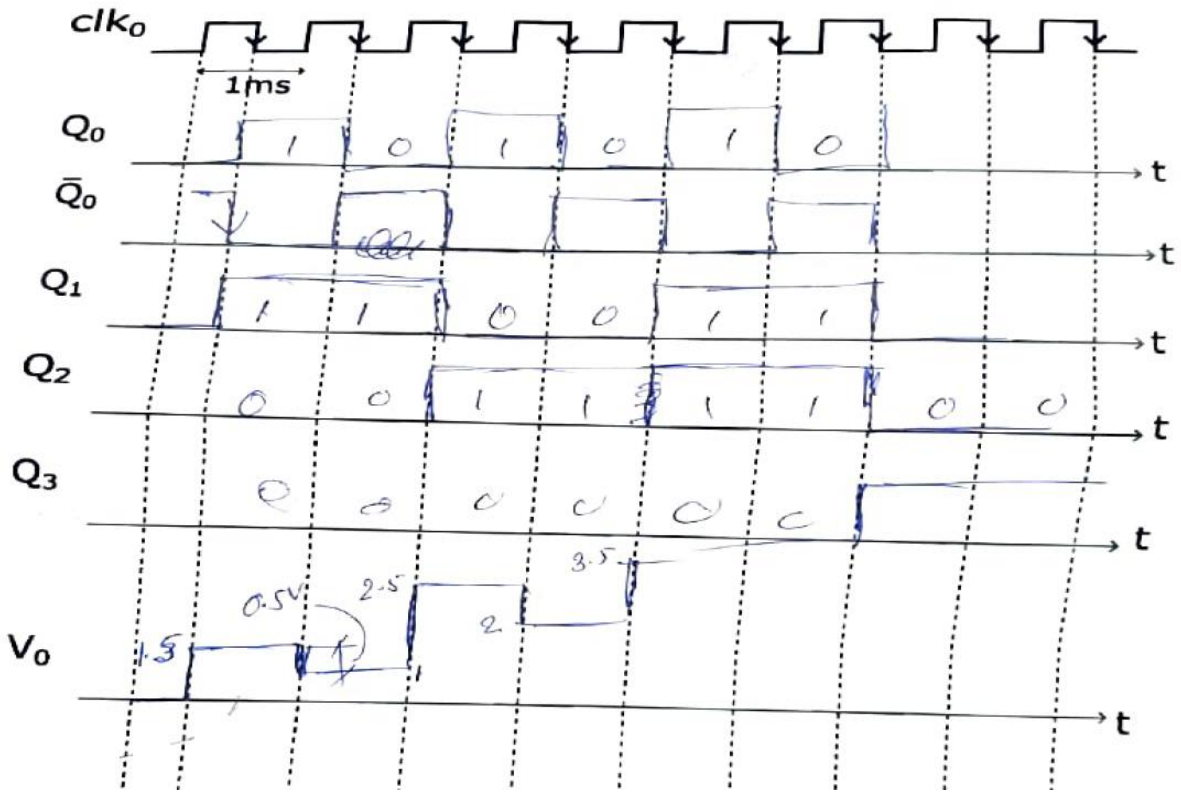
**Solution 3.**

| X | Y | Q | J | K |
|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | $Q_0$ | 0 | 0 |
| 1 | 0 | Toggle | 1 | 1 |
| 1 | 1 | 0 | 0 | 1 |




**Solution 4.**






Question5.

| $Q_0$ | $Q_1$ | $Q_2$ | $Q_0^{n+1}$ | $Q_1^{n+1}$ | $Q_2^{n+1}$ |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 0 |

This is a MOD 5 counter

$\therefore \frac{F_{out}}{F_{clk}} = \frac{1}{5}$

Question 6.

| $J_0^n$ | $K_0^n$ | $Q_0^n$ | $J_1^n$ | $K_1^n$ | $Q_1^n$ | $Q_0^{n+1}$ | $Q_1^{n+1}$ |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 |

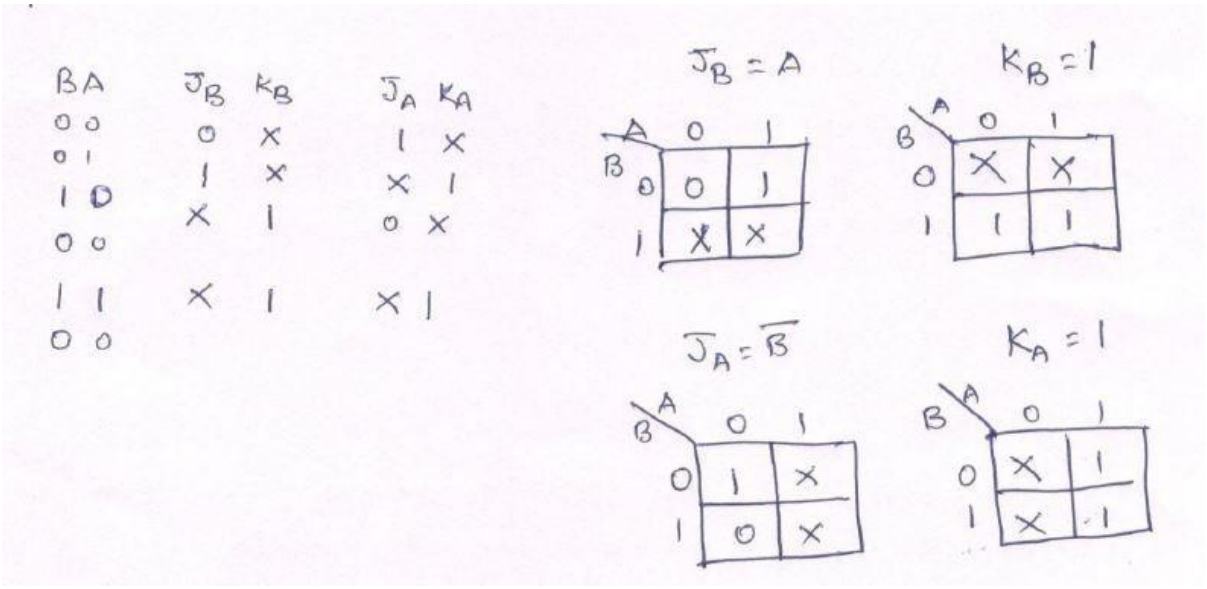
MOD 4 counter

at the end of 33rd clock pulse it would be at

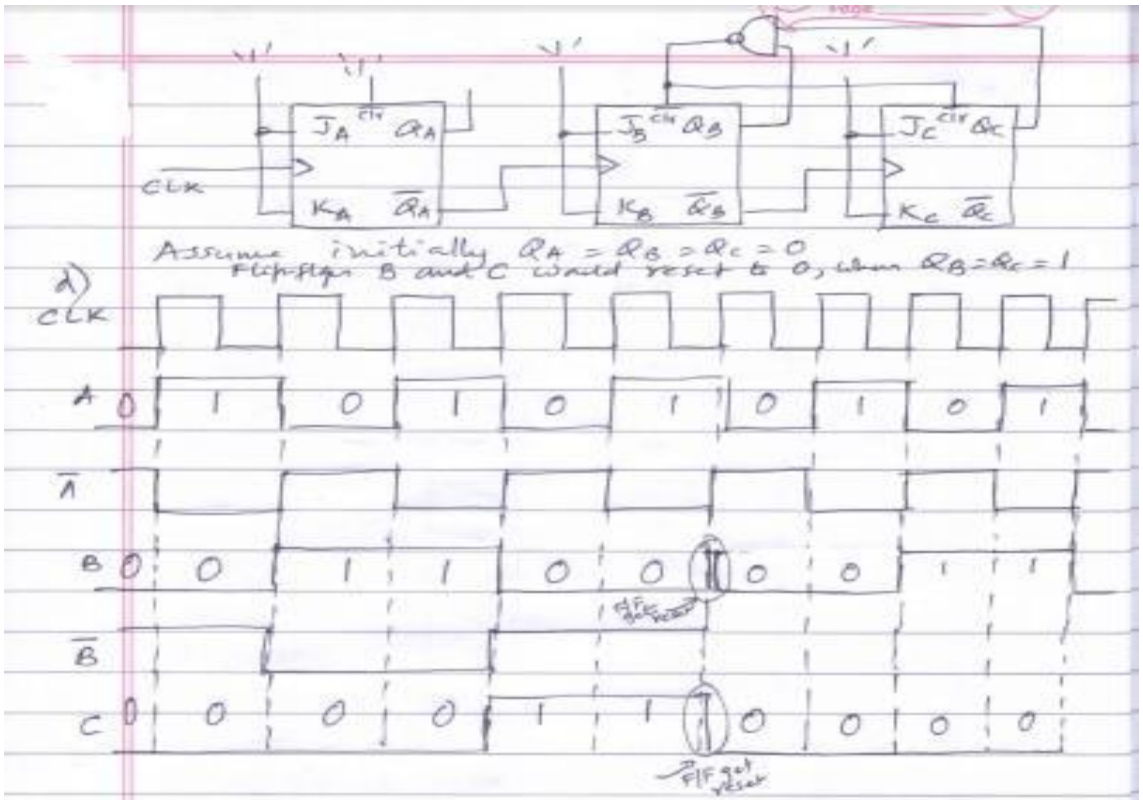
$MOD\left(\frac{33}{4}\right) = 1^{st}$ state

$\therefore Q_1 Q_0 = 01$

Question7.



Question 8.




a) The stable sequence of states are:
CBA: 000, 001, 010, 011, 100, 101
(The counter resets to 000 at '110')

b) UP counter

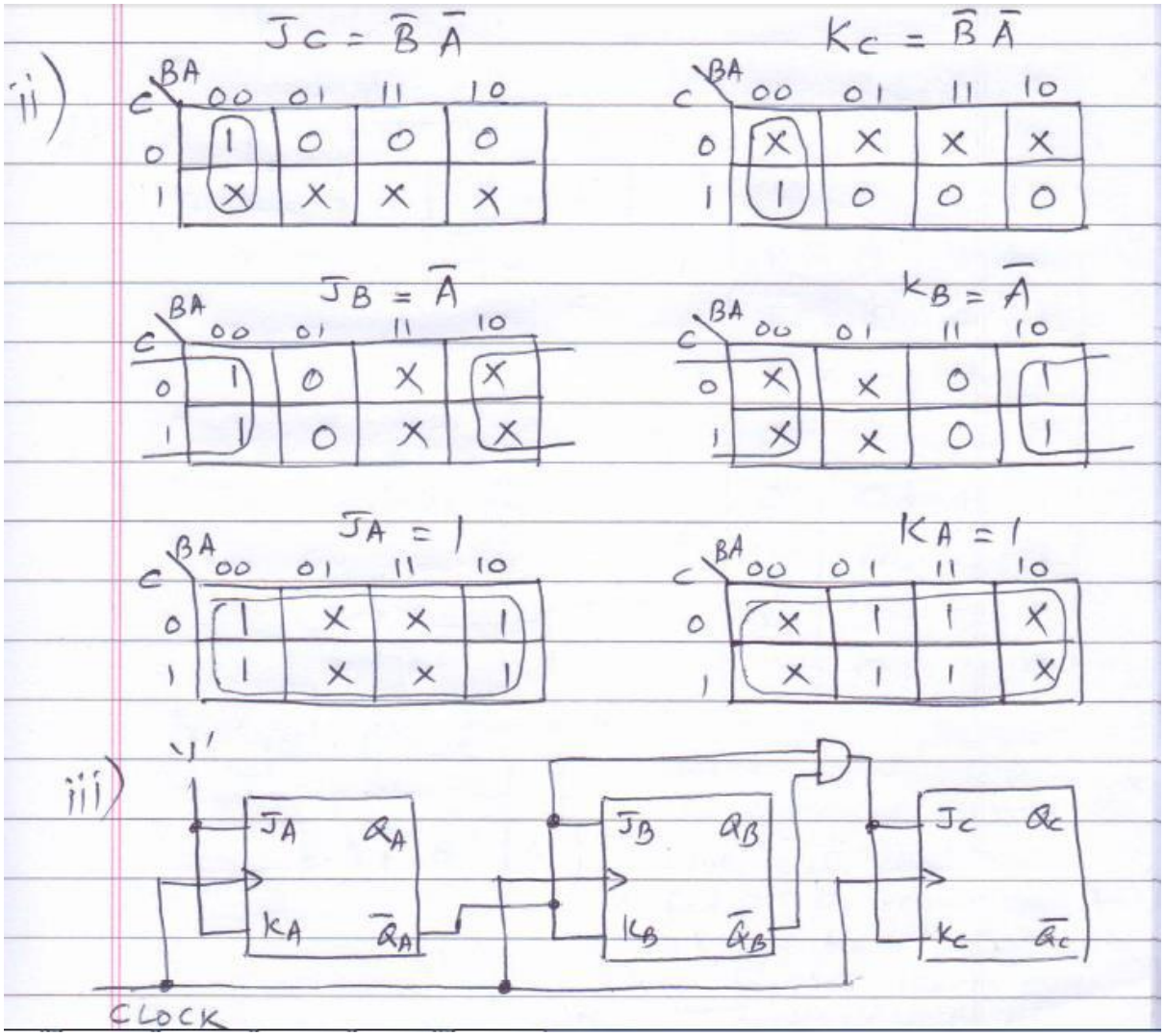
c) Two limitations
i) Being a ripple counter, its maximum frequency of operation will be much less than a synchronous counter
ii) This is not suitable for applications which can misbehave if the quasi stable states are present

Question 9.

| $Q_n$ | $Q_{n+1}$ | Required J | Required K |
|---|---|---|---|
| 0 | 0 | 0 | X |
| 0 | 1 | 1 | X |
| 1 | 0 | X | 1 |
| 1 | 1 | X | 0 |

i) $Q_n$ Sequence

| Present state | | | Required | | | | | | $Q_{n+1}$ Next State | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| C | B | A | $J_C$ | $K_C$ | $J_B$ | $K_B$ | $J_A$ | $K_A$ | C | B | A |
| 1 | 1 | 1 | X | 0 | X | 0 | X | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | X | 0 | X | 1 | 1 | X | 1 | 0 | 1 |
| 1 | 0 | 1 | X | 0 | 0 | X | X | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | X | 1 | 1 | X | 1 | X | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | X | X | 0 | X | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | X | X | 1 | 1 | X | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | X | 0 | X | X | 1 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | X | 1 | X | 1 | X | 1 | 1 | 1 |
| 1 | 1 | 1 | | | | | | | | | |


ii)
$J_C = \bar{B}\,\bar{A}$
$K_C = \bar{B}\,\bar{A}$
$J_B = \bar{A}$
$K_B = \bar{A}$
$J_A = 1$
$K_A = 1$
BA
C
00 01 11 10
iii)
$J_A$ $Q_A$ $K_A$ $\bar{Q}_A$
$J_B$ $Q_B$ $K_B$ $\bar{Q}_B$
$J_C$ $Q_C$ $K_C$ $\bar{Q}_C$
CLOCK

**10.**