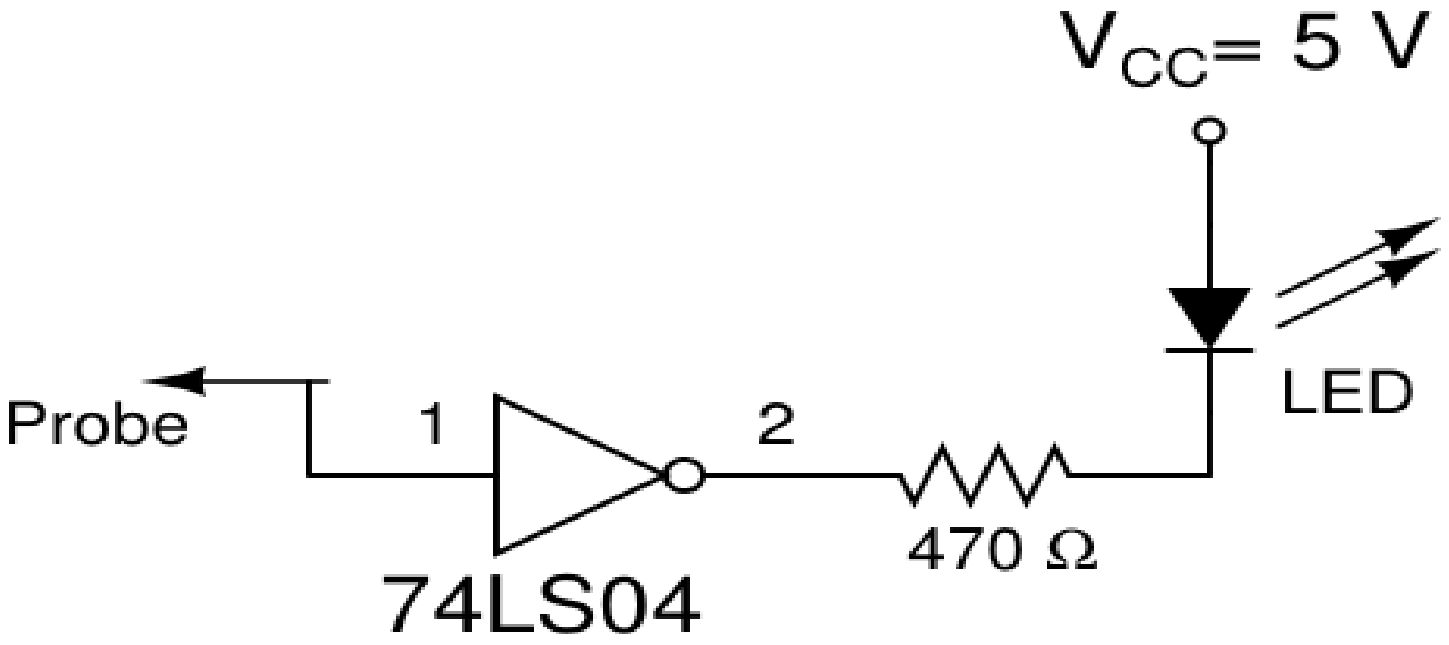
EE103 – Digital Lab Demo

2023-24/I Autumn

A) Logic Probe Circuit



'1' : LED ON

'0' : LED OFF

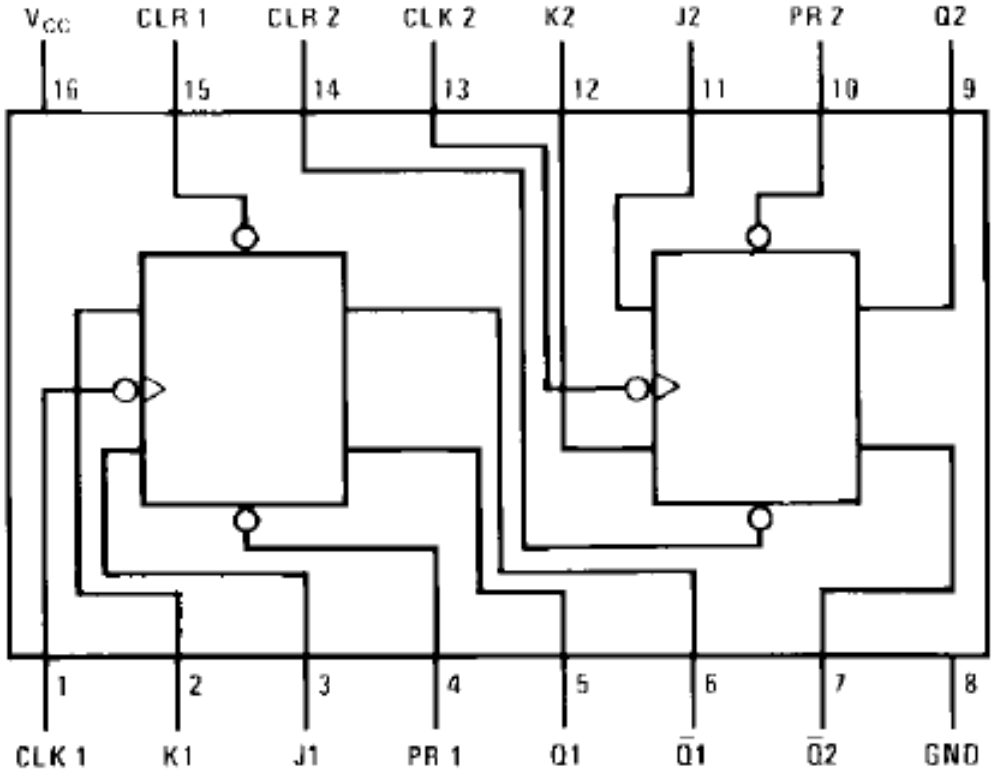
V_{cc}= 5 V (Pin 14)

GND - Pin 7

JK Flip-flop Function Table

Function Table

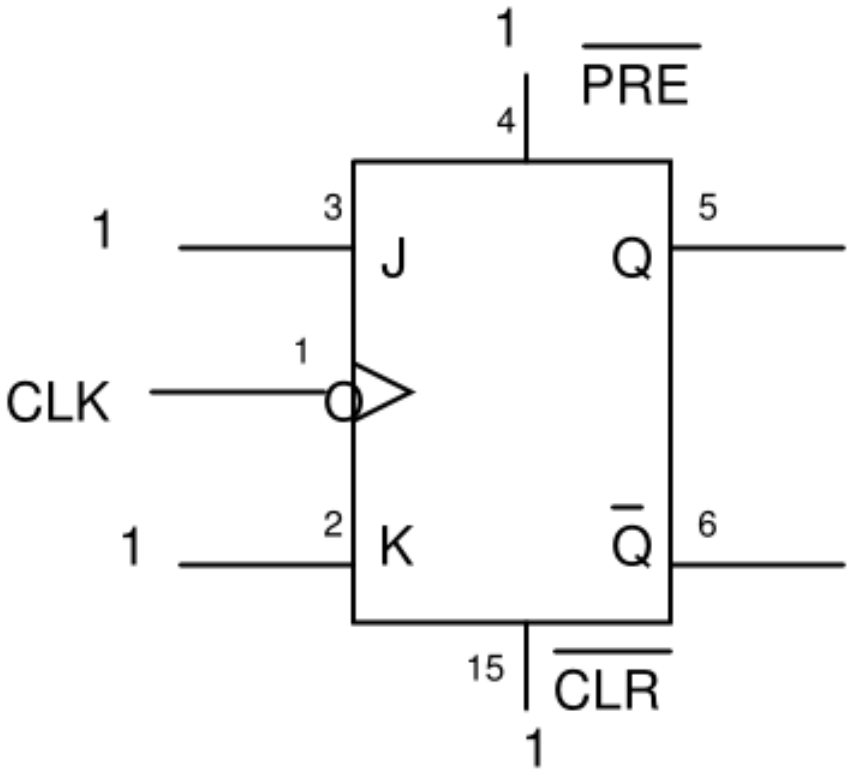
Inputs					Outputs	
PR	CLR	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q_0	$\overline{Q}_0$



- Synchronous inputs: J and K
- Asynchronous inputs: PRE’ and CLR’

74S112 JK Flip-flop Pin-out

B) Toggle Flip-flop (using JK Flip-flop)



74S112 -ve Edge-triggered JK F/F

Pin 16 : +5 V ; Pin 8 : GND

- JK Flip-flop wired as a Toggle Flip-flop (Mod-2 counter)
- J = K = 1; PRE'= CLR'= 1
- Q changes at the negative Clock edges

- V_{cc} line corrupted by switching noise
- Should use a de-coupling capacitor (between V_{cc} and GND – typ 0.1 µF)

C) Mod-6 Ripple UP Counter

- Problem Statement: Design a modulo-6 Ripple UP counter using negative-edge triggered JK flip-flops.
- (Hint: Being an UP counter, use the following sequence of states (CBA): 000, 001, 010, 011, 100, 101, 000, 001,…. – will make design simpler)

- Solution: Connect input Clock to FF-A Clock input; Q_A output to FF-B Clock; Q_B output to FF-C Clock. Outputs $Q_CQ_BQ_A$ (or CBA).

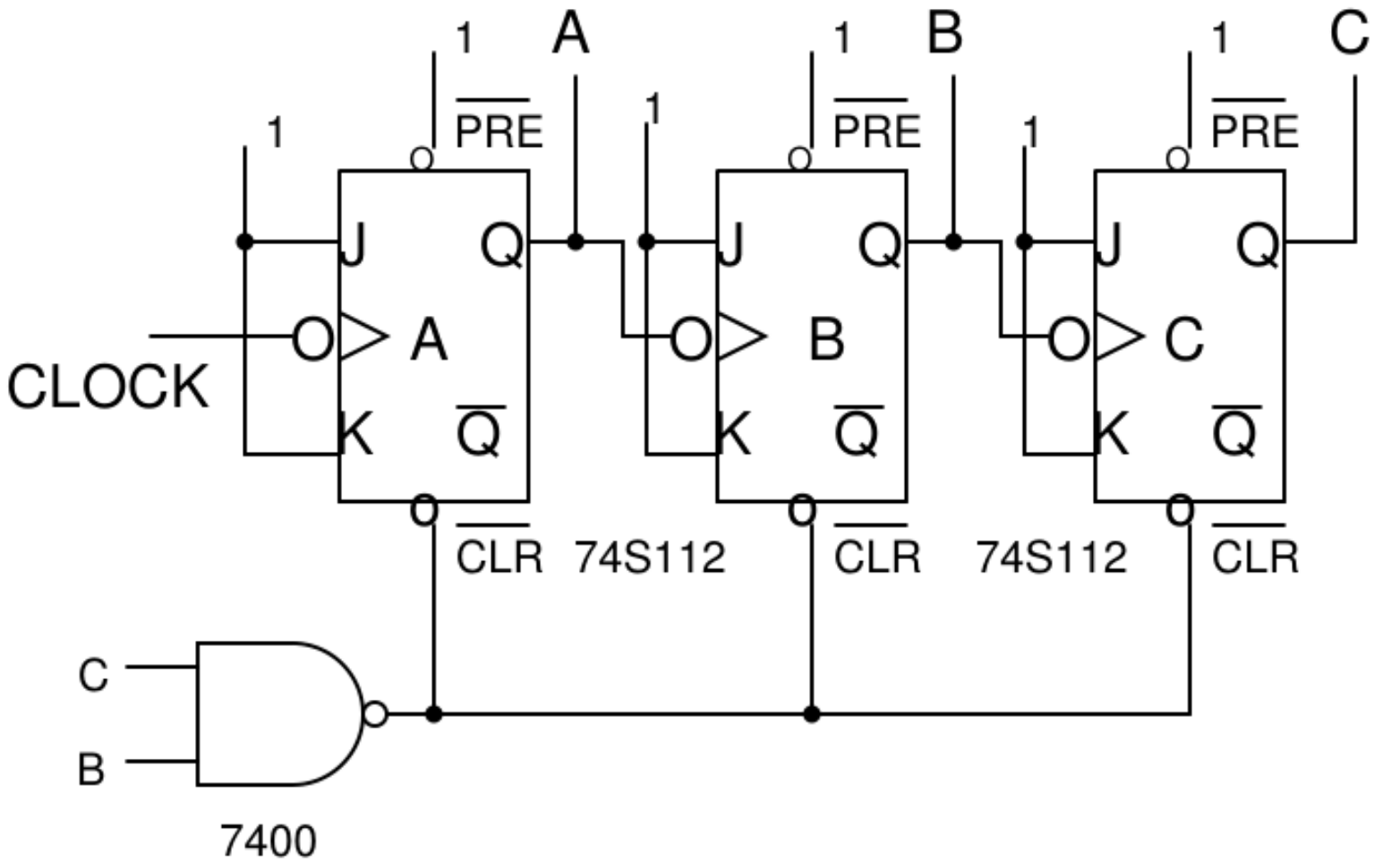
Stable States (CBA):

000, 001, 010, 011, 100, 101

Unstable (Quasi-stable) State (CBA):

110 (we will decode this state and clear the flip-flop)

Mod-6 Ripple UP Counter



Stable States (CBA):

000, 001, 010, 011, 100, 101

Unstable State (CBA):

110

State 111 can occur only at Power ON

Ripple Counter Behaviour at Higher Clock Frequencies

- Advantage
  - Easy to design

- Disadvantages
  - Ripple counters used only up to a few MHz
  - Asynchronous outputs
  - The Quasi-stable state can create problems (in time critical applications)

D) Mod-5 Ripple DOWN Counter

- Problem Statement: Design a modulo-5 Ripple DOWN counter using negative-edge triggered JK flip-flops.
- (Hint: Being a DOWN counter, use the following sequence of states (CBA): 111, 110, 101, 100, 011, 111, 110,…. – will make design simpler)

- Solution: Connect input Clock to FF-A Clock input; Q_A' output to FF-B Clock; Q_B' output to FF-C Clock. Outputs Q_C Q_B Q_A (or CBA).

Stable States (CBA):

111, 110, 101, 100, 011

Unstable (Quasi-stable) State (CBA):

010 (we will decode this state and clear the flip-flop). Decode BA'

Mod-5 Ripple DOWN Counter

Stable States (CBA):

111, 110, 101, 100, 011

Unstable State (CBA):

010

States 001 and 000 can occur only at Power ON