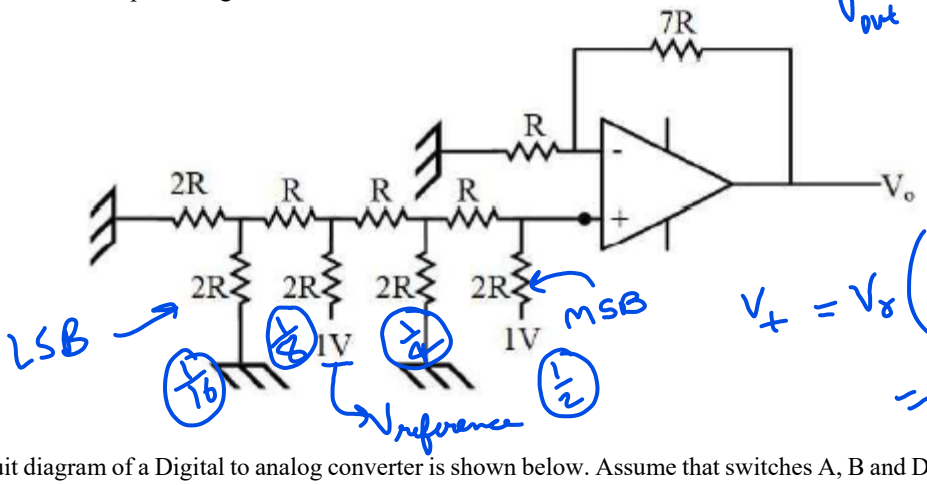
Practice Problem Set

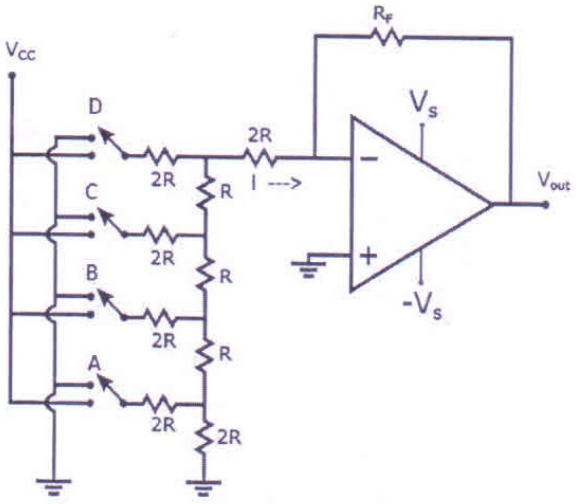
1. Determine the output voltage V_0 of a 4 bit DAC shown below.



2. Circuit diagram of a Digital to analog converter is shown below. Assume that switches A, B and D are in the 'GND' position, while switch C is in the 'V_{on}' position.

a) Obtain an expression for the current I in terms of V_{cc} and R.

b) If V_{cc} = 6 Volts and R_F = R, calculate V_{out} (for the switch positions as mentioned above).



3. Circuit diagram of a Digital-to-Analog Converter is shown below.

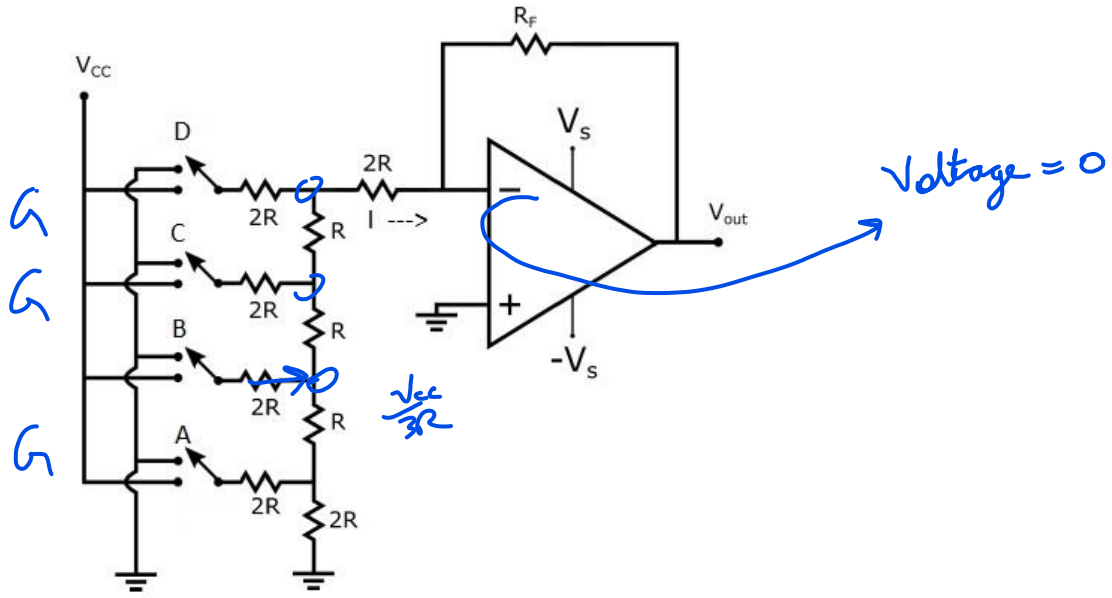
a) Assuming that switches D, C and B are in the 'GND' position, while switch A is in the 'V_{cc}' position, write current I (as indicated in the figure) in terms of V_{cc} and R. Show steps. No marks without steps.

b) Assuming that switches D, C and A are in the 'GND' position, while switch B is in the 'V_{cc}' position, write current I (as indicated in the figure) in terms of V_{cc} and R. Show steps. No marks without steps.

c) Based on the expressions you obtained in (a) and (b) above, write I (as indicated in the figure) in terms of V_{cc} and R assuming switches D and C are in the 'GND' position, while switches B and A are in the 'V_{cc}' position.

d) For case (c) calculate V_{out} assuming V_{cc} = 5 V and R_F = 2R.

e) What is the 'step-size' or 'resolution' (in Volts) of the given DAC?



4. Design a modulo-6 synchronous DOWN counter using +ve edge triggered JK flip-flops, with the following sequence of states (CBA): 111, 110, 101, 100, 011, 010, 111, …. If any of the unused states, i.e. if states (CBA): 001 or 000 comes, the next state should be 111.
Give all the design steps, i.e. the table of present states and the required JK inputs for the next state, and the K map minimizations for the J and K inputs of the flip-flops.

5.
Design a modulo-3 synchronous UP counter using +ve edge triggered JK flip-flops, with the sequence of states (BA): 01, 10, 11, 01, …. If the unused state 00 comes, the next state should be 01. Give all the design steps, i.e. the table of present states and the required JK inputs for the next state, and the K map minimizations for the J and K inputs of the flip-flops. No need to draw the final circuit diagram.

6. Block diagram of a simple analog-to-digital converter (ADC) is given below. Assume that the ADC is 4-bit with digital outputs D, C, B and A, where D is the MSB and A the LSB. The Opamp comparator output EOC gives '1' when $V_A > V_{AX}$, else '0'. The digital-to-analog converter (DAC) output V_{AX} is given by:

$$V_{AX} = V_{REF}\,[D(1/2) + C(1/4) + B(1/8) + A(1/16)\,]$$

It is assumed that, each time a valid input voltage V_A is applied to the ADC input, a short SOC pulse is applied to the circuit as shown, which resets the Binary counter and starts the ADC operation, giving a 4-bit digital value corresponding to the given analog input V_A. Assume $V_{REF} = 5V$ and the Clock frequency is 20 kHz.

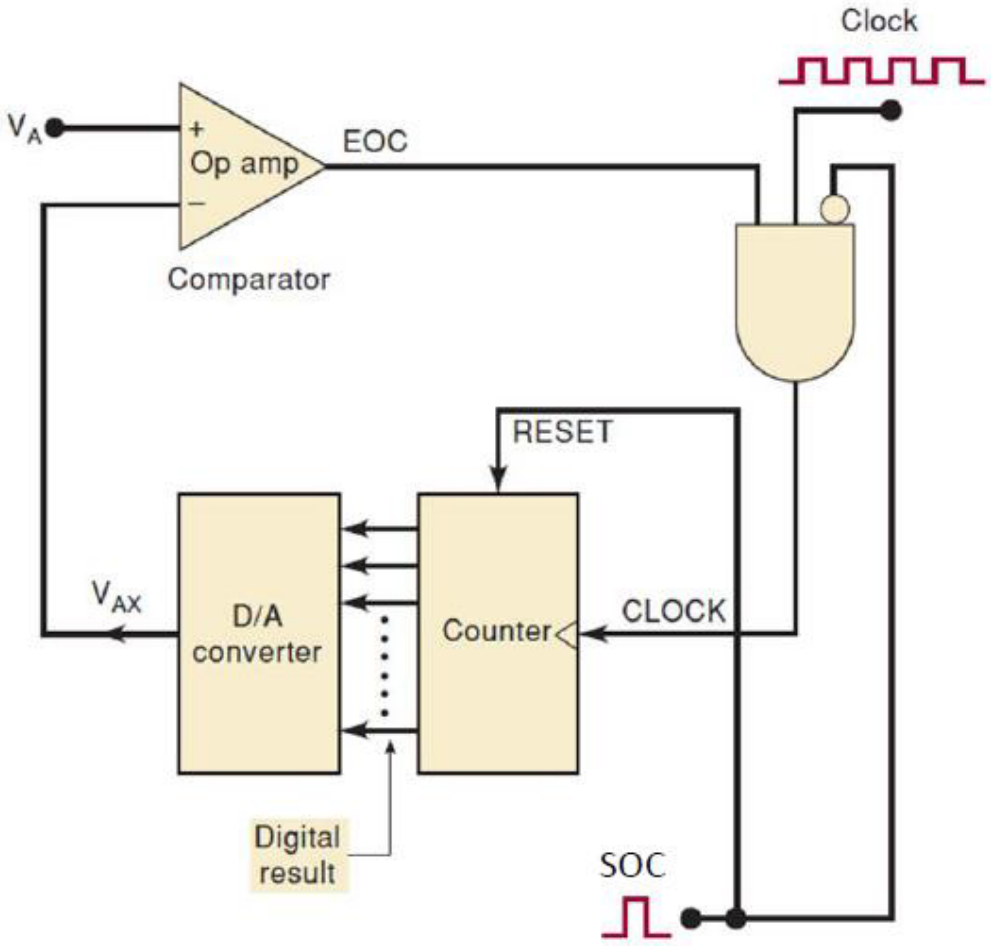
a) What is the step-size (or resolution) of this ADC in Volts?

b) What range of V_A values can be digitized by this ADC? Show steps to justify your answer.

c) For $V_A = 3$ V, what will be the digital output (DCBA)? Show steps to justify your answer.

d) What will be the time taken (in µsec, i.e. micro seconds) to get the digital output for the ADC operation in (c). You may neglect the delays caused by the Opamp comparator, DAC and the AND gate.

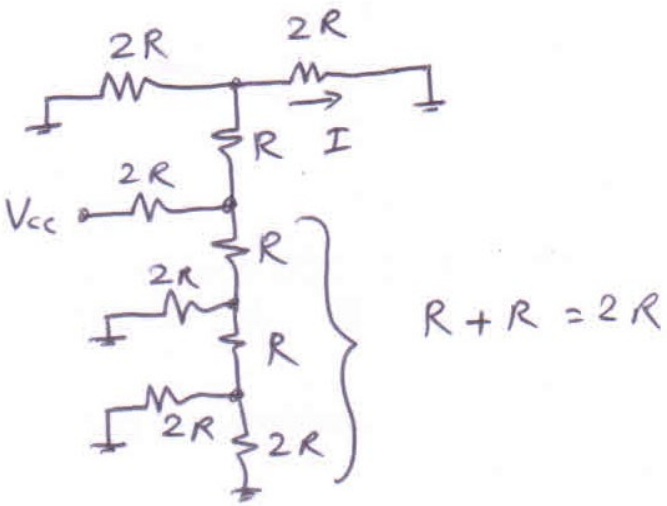
e) What will be the maximum time taken (in µsec) to digitize the highest V_A value?


Clock
V_A
+
Op amp
−
EOC
Comparator
RESET
V_{AX}
D/A
converter
Counter
CLOCK
Digital
result
SOC

Solution Q1.

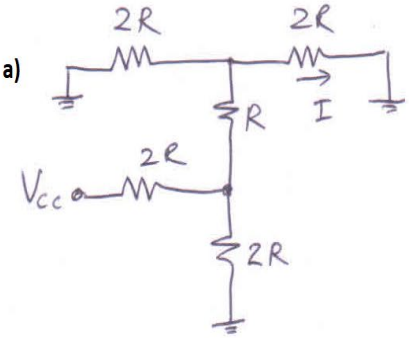
$$V_o = \left(\frac{1}{8} + \frac{1}{2}\right) \times 8 = \frac{5}{8} \times 8 = 5V$$

Solution 2.

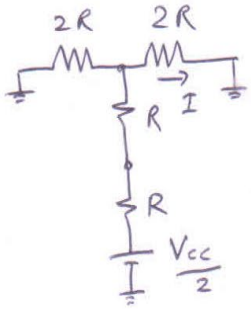


$R + R = 2R$

a)



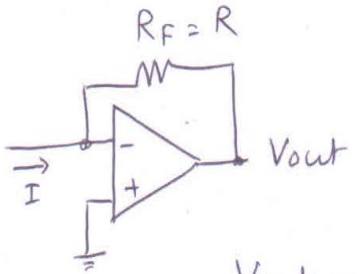
$\Rightarrow$



$$\therefore I = \frac{1}{2}\left(\frac{V_{cc}/2}{3R}\right) = \frac{V_{cc}}{12R}$$

b) $V_{cc} = 6V$

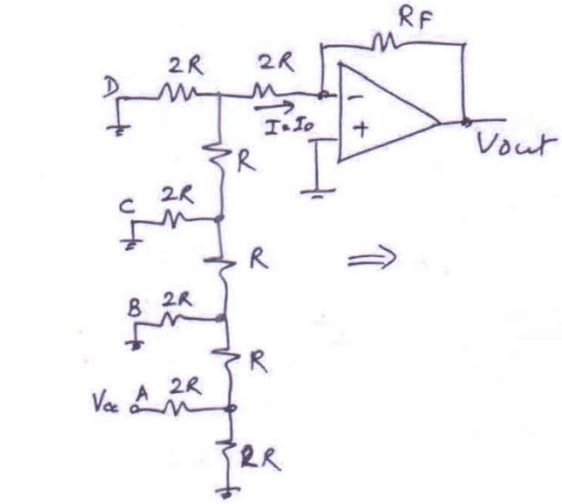
$R_F = R$



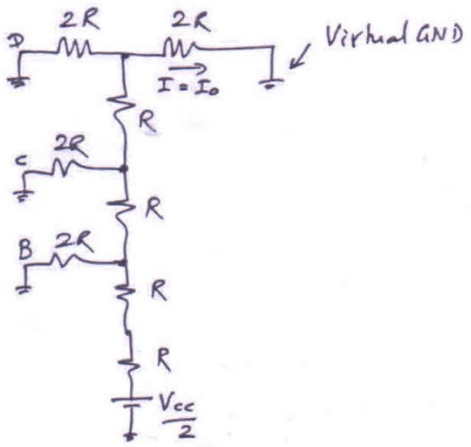
$$V_{out} = -\left(\frac{V_{cc}}{12R}\right) \cdot R = -\frac{V_{cc}}{12} = -0.5V$$

Solution 3.

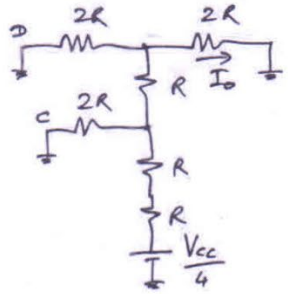
a) D, C, and B are in GND position; A in V_{cc} position



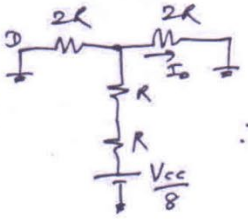
$\Rightarrow$



$\Rightarrow$

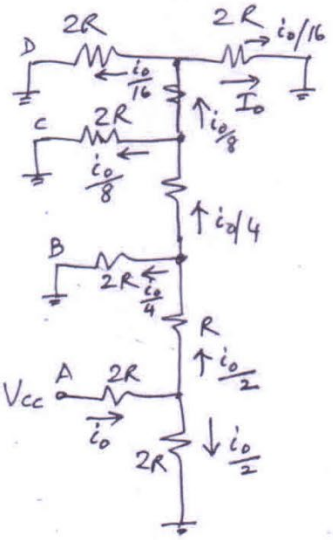


$\Rightarrow$

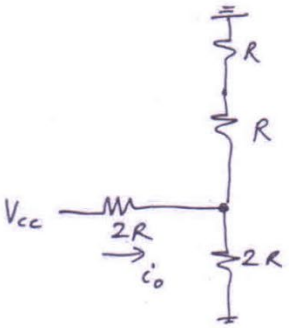


$$\therefore I_o = \frac{(V_{cc}/8)}{3R} \cdot \left(\frac{1}{2}\right) = \frac{V_{cc}}{48R}$$

OR



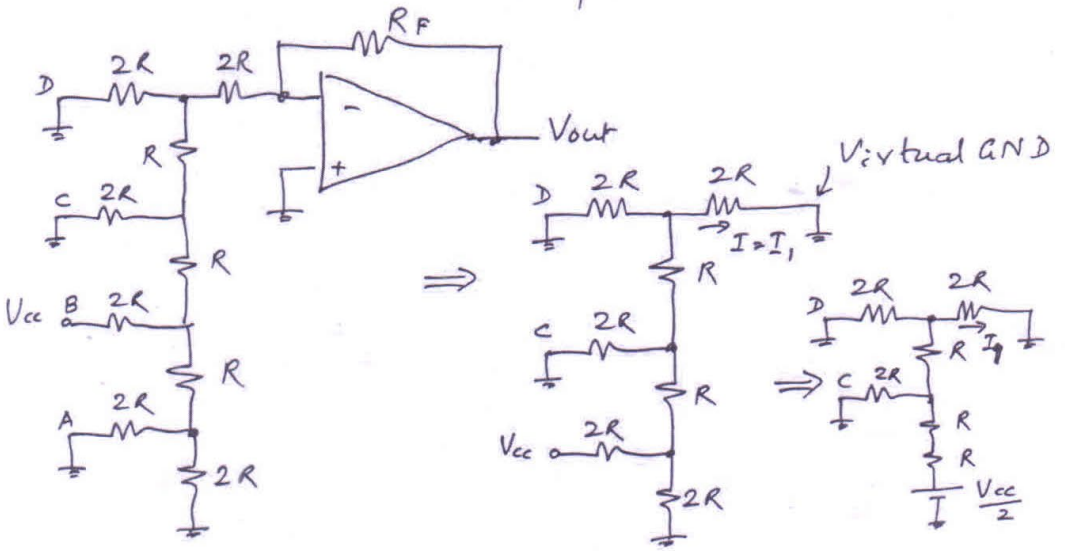
i.e. $I_o = \frac{i_o}{16}$,

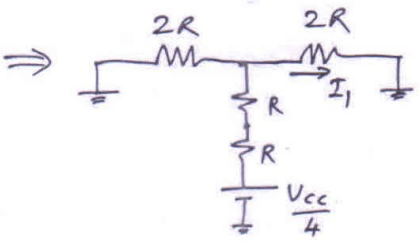


$$i_o = \frac{V_{cc}}{3R}$$

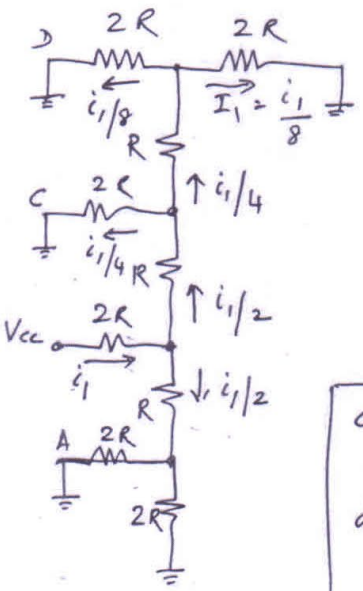
$$\therefore I_o = I = \frac{i_o}{16} = \frac{V_{cc}}{48R}$$

b) D, C, and A are in GND position,
B in V_{cc} position:





$$\Rightarrow I = I_1 = \frac{(V_{cc}/4)}{3R} \cdot \left(\frac{1}{2}\right) = \frac{V_{cc}}{24R}$$



OR

$$\therefore I_1 = \frac{i_1}{8} \quad ; \quad i_1 = \frac{V_{cc}}{3R}$$

$$\therefore I = I_1 = \frac{V_{cc}}{24R}$$

c) $I = I_0 + I_1 = \frac{V_{cc}}{48R} + \frac{V_{cc}}{24R} = \frac{3\,V_{cc}}{48R}$

d) $V_{cc} = 5V$, $R_F = 2R$;

$$V_{out} = -I \cdot R_F = -\frac{3V_{cc}}{48R} \cdot 2R$$

$$= -0.625V$$

e) Stepsize or Resolution $(= -I_0 \cdot R_F) = \left(\frac{V_{cc}}{48R}\right) \cdot 2R = 0.2083V$

Solution 4.

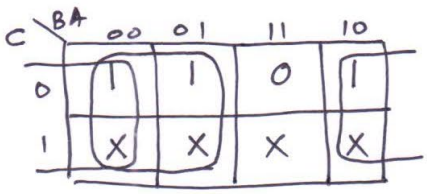
Transition Table for a JK flip-flop

Q_n	Q_{n+1}		J	K
0	0		0	X
0	1		1	X
1	0		X	1
1	1		X	0

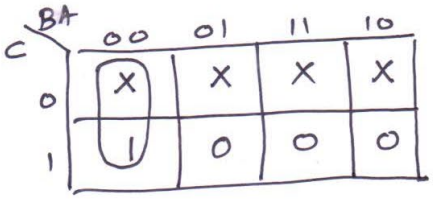
Design Table: Sequence of states, and required J,K inputs

C	B	A		J_C	K_C	J_B	K_B	J_A	K_A
1	1	1		X	0	X	0	X	1
1	1	0		X	0	X	1	1	X
1	0	1		X	0	0	X	X	1
1	0	0		X	1	1	X	1	X
0	1	1		0	X	X	0	X	1
0	1	0		1	X	X	0	1	X
1	1	1							
0	0	1		1	X	1	X	X	0
1	1	1							
0	0	0		1	X	1	X	1	X
1	1	1							

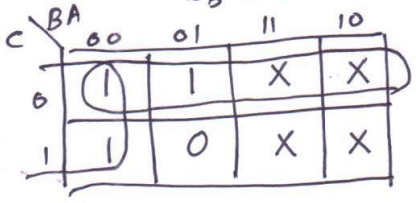
$J_C = \bar{B} + \bar{A}$



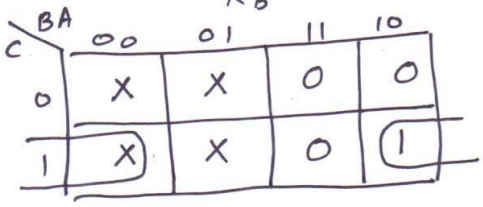
$K_C = \bar{B}\bar{A}$



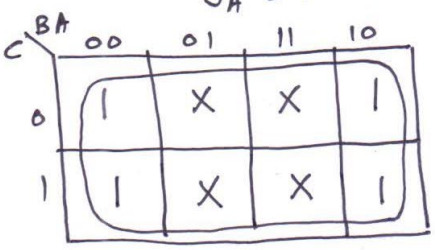
$J_B = \bar{C} + \bar{A}$



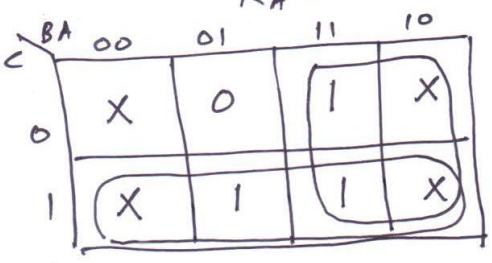
$K_B = C\bar{A}$



$J_A = 1$



$K_A = C + B$



Question5.

B	A	J_B	K_B	J_A	K_A
0	1	1	X	X	1
1	0	X	0	1	X
1	1	X	1	X	0
0	1				
0	0	0	X	1	X
0	1				

Excitation Table

Q_n	Q_{n+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

J_B

B \ A	0	1
0	0	1
1	X	X

$J_B = A$

K_B

B \ A	0	1
0	X	X
1	0	1

$K_B = A$

J_A

B \ A	0	1
0	1	X
1	1	X

$J_A = 1$

K_A

B \ A	0	1
0	X	1
1	X	0

$K_A = \bar{B}$

Question6.

8. ADC

$$V_{XD} = V_{ref}\left[D(0.5) + C(0.25) + B(0.125) + A(0.0625)\right]$$

$V_{ref} = 5V$

a) Step-size or resolution

$$= \overset{5V}{V_{ref}} \cdot (0.0625) = 0.3125\ V$$

b) Max. range of ADC $= (V_{ref} - LSB)$

Since $V_{ref}\left[0.5 + 0.25 + 0.125 + 0.0625\right]$

$= 5 \times 0.9375 = 4.6875\ V$ (Ideally, max range should be within 4.375 and 4.6875 V)

Range of ADC $= \dfrac{0 - 4.6875\ V}{0 < V_A < 4.6875\ V} \rightarrow \dfrac{75}{16}$

c) $V_A = 3V$

Step size $= 0.3125$

Digitization is completed when $V_{AX} > V_A$

# of steps $= \dfrac{3V}{0.3125} = 9.6 \Rightarrow 10$ steps

$\therefore$ DCBA output is : 1010

d) Time taken $= (10 \text{ steps}) \times \left(\dfrac{1}{20kHz}\right) = 500\ \mu s$

e) Maximum time taken $= 15 \times 50\ \mu s = 750\ \mu s$