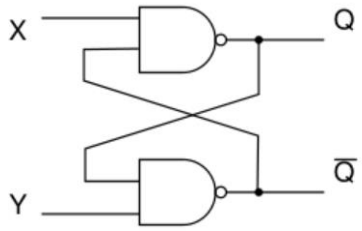
EE 113 – Intro to Electrical Engg Practice: 2021-22/I

Problem Sheet – 5: Digital Electronics

Topics: Sequential Circuits – NAND latch, SR Flip-flop, JK flip-flop, D-flip-flop, Ripple counters (Asynchronous counters), Synchronous counters

Part A– Latches and Flip-flops

1. The circuit diagram of a NAND latch is shown below.



a) Assume that initially $Q = 1$ and $\bar{Q} = 0$. Analyze the NAND latch and verify that if the inputs are $X = 0\ and\ Y = 1$, then the outputs will continue to be at the same states.

b) Verify again that if now the inputs are made $X = 1\ and\ Y = 1$, then also the outputs $Q\ and\ \bar{Q}$ will remain at the same state as before.

c) Now change input conditions to $X = 1\ and\ Y = 0$. Analyze the circuit and determine the outputs $Q\ and\ \bar{Q}$.

d) Verify again that if now the inputs are made $X = 1\ and\ Y = 1$, then the outputs $Q\ and\ \bar{Q}$ will remain at the same state as before.

e) Now change input conditions to $X = 0\ and\ Y = 0$. Analyze the circuit and determine the outputs $Q\ and\ \bar{Q}$.

f) Find out what will happen if now the inputs are made $X = 1\ and\ Y = 1$. (If you analyse the circuit now to determine $Q\ and\ \bar{Q}$, you will see that you get two valid sets of results, i.e. $Q = 1$ and $\bar{Q} = 0$ or $Q = 0$ and $\bar{Q} = 1$).

Note: The above inconsistent result is one of the main reasons for not allowing the input condition $X = 0\ and\ Y = 0$. In actual practice, when the condition mentioned in (e) is followed by (f), then NAND gate with the shorter propagation delay would force its output to be '0'. Accordingly, the second NAND gate output would become '1'.

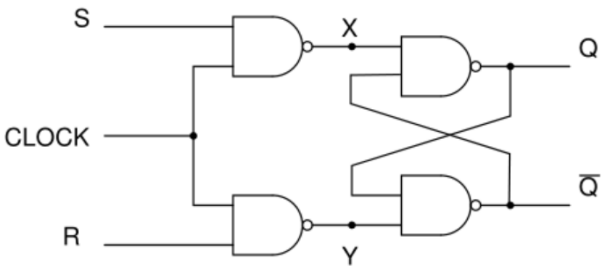
The second reason why the input condition $X = 0\ and\ Y = 0$ is not allowed is that for other except this input condition the outputs of the NAND latch are complimentary. In sequential circuits this property of the outputs being complementary is very useful.

For the above two reasons, we write the input condition $X = 0\ and\ Y = 0$ as 'Not allowed'.

2. The schematic diagram of an SR flip-flop is shown below. Analyse the circuit and write the truth table for the same (Inputs: S, R and CLOCK; Outputs Q *and* $\bar{Q}$).

a) For which input condition do you find inconsistency in the Q *and* $\bar{Q}$ outputs?

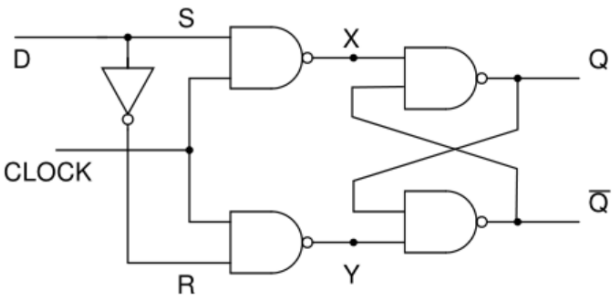
b) Based on the above truth table define what is the role of the Clock input, also for what condition of the Clock (i.e. High, Low or +ve or -ve edge) the flip-flop is able to operate normally.



3. An SR flip-flop modified to give is a D flip-flop shown below.

a) Write the truth table for this flip-flop.

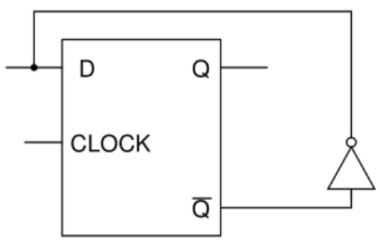
b) What is the utility of this flip-flop? A common question/confusion by students is that since in a D flip-flop, output is the same as the input, why do we use this flip-flop? Go through the reference material uploaded on Moodle and find at least two major applications of the D flip-flop.



4.An interesting application of the D flip-flop is shown below. Assume that the input Clock signal is a square wave of 1 kHz (i.e. Clock High = Clock Low = 0.5 msec). Assume that the D flip-flop used here is the same as used in problem 3.

a) Sketch the Q output with respect to the Clock for at least eight clock periods. Assume that initially Q = '0'. What is the frequency of the waveform at the Q output?

b) Assume that the Clock signal is now changed to a waveform of 1 kHz, but with Clock High = 0.25 msec, Clock Low = 0.75 msec. Sketch the Q output with respect to the Clock for at least eight clock periods. Assume that initially Q = '0'. Based on the Q output waveforms you obtained in (a) and (b) name two interesting applications of the circuit shown.



5. A D flip-flop application, similar to the one in problem 4 is shown below. Here instead of the of the Clock level sensitive D flip-flop used in problem 4, a +ve edge triggered D flip-flop is used.

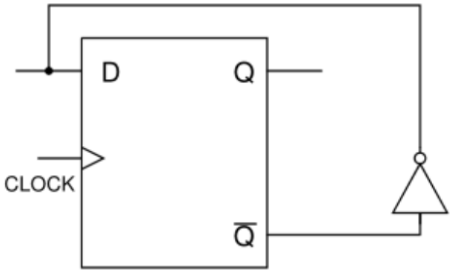
a) Sketch the Q output with respect to the Clock for at least eight clock periods. Assume that initially Q = '0'. What is the frequency of the waveform at the Q output?

b) Assume that the Clock signal is now changed to a waveform of 1 kHz, but with Clock High = 0.25 msec, Clock Low = 0.75 msec. Sketch the Q output with respect to the Clock for at least eight clock periods. Once again assume that initially Q = '0'.

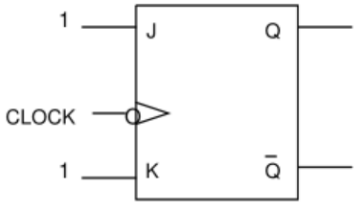
c) Is there any difference in the waveforms you got in this problem compared to the ones you got for problem 4? Justify your answer.

d) If instead of the +ve edge triggered flip-flop shown, if a -ve edge triggered D flip-flop is used for the cases 5(a) and 5(b), what will be the difference in the Q output waveforms compared to the +ve edge triggered case?

e) Refer to the reference material uploaded on Moodle and find out what is the advantage in using edge-triggered flip-flops instead of level sensitive flip-flops.



6. A JK flip-flop circuit is shown below where J = 1, K =1 and the given JK flip-flop is a negative edge-triggered flip flop. Assume that the Clock input is a 10 kHz square wave signal. Sketch the Q output with respect to the Clock for at least eight clock periods. Assume that initially Q = '0'. What is the frequency of the waveform at the Q output?

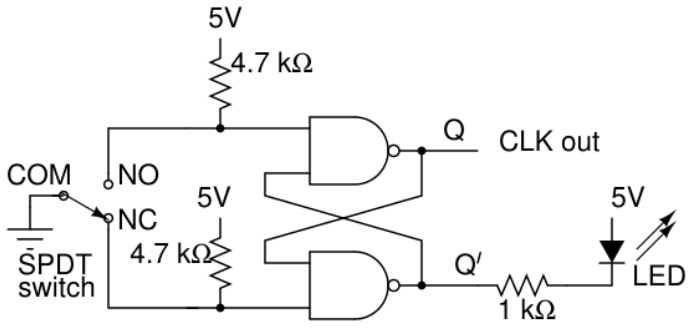


7 C) A latch circuit commonly used for generating manual clock is shown below, where a spring-loaded single-pole double-throw (SPDT) switch is used. This switch has three contacts, viz. Common (COM), Normally-Open (NO), and Normally-closed (NC).

i) In the switch position is as shown in the figure, what will be the Q output and the state of the LED (ON or OFF)?

ii) In the switch position as shown, what will be the currents flowing into the Std TTL NAND gate inputs connected to NO and NC? Std TTL gate current specifications: I_{OH} = 400 µA, I_{OL} = 16 mA, I_{IH} = 40 µA, I_{IL} = 1.6 mA.

iii) Why is such a latch circuit required for generating clock manually with each press; instead why not just use the switch (with connections to +5V) for generating clock pulse with each press?



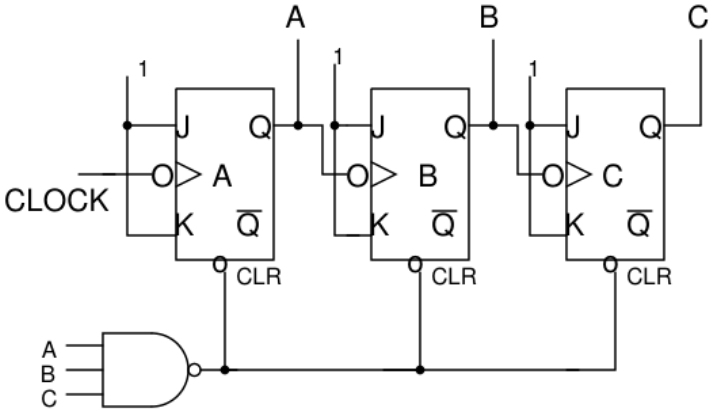
Part B – Ripple Counters (Asynchronous Counters)

8. The circuit diagram of a Ripple Counter is shown below. It uses –ve edge-triggered JK flip-flops. The JK flip-flops have active-low asynchronous clear inputs (i.e. irrespective of the Clock, when CLR = '0' the flip-flop is reset).

a) Analyze the circuit and write the stable sequence of states (CBA), where C is the MSB and A is the LSB.

b) Based on your answer in (a) classify the counter as a Mod-N UP counter or a Mod-N DOWN counter.

c) Sketch the A, B and C outputs of the counter with respect to the Clock for at least 8 Clock periods.



9. Design a modulo-5 Ripple UP counter using –ve edge triggered JK flip flops and one extra gate (any type of one gate with any number of inputs). Assume that each JK flip-flop has both Q and Q' outputs and also an active-low asynchronous Clear input (i.e. when the Clear input = '0', the Q output will be '0' irrespective of the Clock). Draw a clear circuit diagram and sketch the timing diagram showing the CBA outputs (C is the MSB) with respect to the Clock for at least eight Clock periods.

Part C – Synchronous Counters

10. Design a modulo-3 synchronous UP counter using +ve edge triggered JK flip-flops, with the sequence of states (BA): 01, 10, 11, 01, …. If the unused state 00 comes, the next state should be 01. Give all the design steps, i.e. the table of present states, next states, the required JK inputs for the next state, and the K map minimizations for the J and K inputs of the flip-flops. Draw the final circuit diagram.

11. Design a modulo-6 synchronous DOWN counter using +ve edge triggered JK flip-flops, with the following sequence of states (CBA): 111, 110, 101, 100, 011, 010, 111, …. If any of the unused states, i.e. if states (CBA): 001 or 000 comes, the next state should be 111.

    Give all the design steps, i.e. the table of present states, next states, and the required JK inputs for the next state, and the K map minimizations for the J and K inputs of the flip-flops. No need to draw the final circuit diagram.

12. a) Design a mod-7 synchronous counter having the sequence of states (CBA): 000, 001, 010, 011, 100, 101, 110, 000,… using -ve edge triggered JK flip-flops. If the unused state (CBA): 111 appears at the start, the next state should be 000.

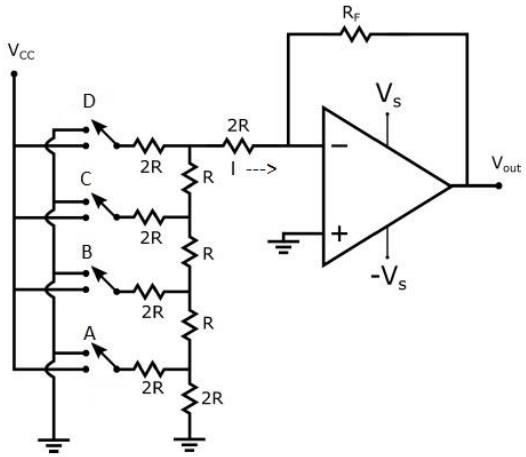
    Give all the design steps, i.e. the table of present states, next states, and the required JK inputs for the next state, and the K map minimizations for the J and K inputs of the flip-flops. No need to draw the final circuit diagram.

Part D – R-2R ladder, DAC and ADC

13. Circuit diagram of a Digital-to-Analog Converter is shown below. Assume that switches A, B and D are in the 'GND' position, while switch C is in the 'V_{cc}' position.

    a) Obtain an expression for the current I in terms of V_{cc} and R.

    b) If V_{cc} = 6 Volts and R_F = R, calculate V_{out} (for the switch positions as mentioned above).



14. Circuit diagram of a Digital-to-Analog Converter is shown below.

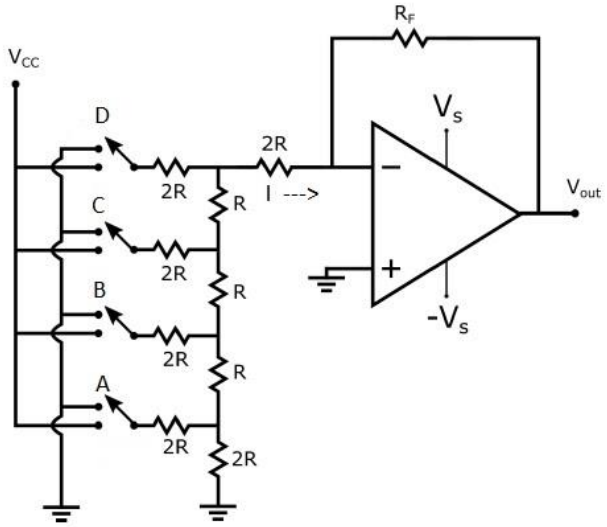
a) Assuming that switches D, C and B are in the 'GND' position, while switch A is in the 'V_{cc}' position, write current I (as indicated in the figure) in terms of V_{cc} and R.

b) Assuming that switches D, C and A are in the 'GND' position, while switch B is in the 'V_{cc}' position, write current I (as indicated in the figure) in terms of V_{cc} and R.

c) Based on the expressions you obtained in (a) and (b) above, write I (as indicated in the figure) in terms of V_{cc} and R assuming switches D and C are in the 'GND' position, while switches B and A are in the 'V_{cc}' position.

d) For case (c) calculate V_{out} assuming V_{cc} = 5 V and R_F = 2R.

e) What is the 'step-size' or 'resolution' (in Volts) of the given DAC?

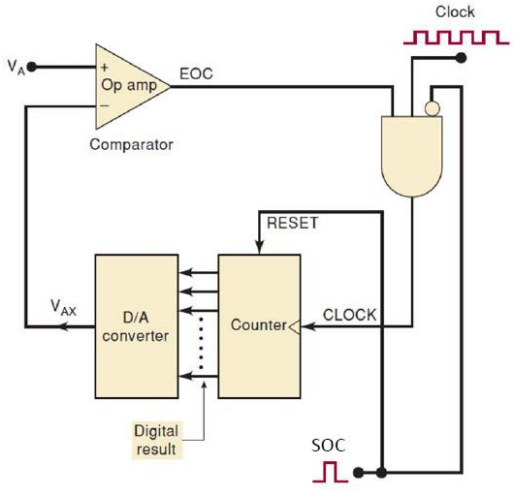


15. Block diagram of a simple analog-to-digital converter (ADC) is given below. Assume that the ADC is 4-bit with digital outputs D, C, B and A, where D is the MSB and A the LSB. The Opamp comparator output EOC gives '1' when $V_A > V_{AX}$, else '0'. The digital-to-analog converter (DAC) output V_{AX} is given by:

$$V_{AX} = V_{REF} [D(1/2) + C(1/4) + B(1/8) + A(1/16)]$$

It is assumed that, each time a valid input voltage V_A is applied to the ADC input, a short SOC pulse is applied to the circuit as shown, which resets the Binary counter and starts the ADC operation, giving a 4-bit digital value corresponding to the given analog input V_A. Assume V_{REF} = 5V and the Clock frequency is 20 kHz.

a) What is the step-size (or resolution) of this ADC in Volts?
b) What range of V_A values can be digitized by this ADC?
c) For V_A = 3 V, what will be the digital output (DCBA)?
d) What will be the time taken (in µsec, i.e. micro seconds) to get the digital output for the ADC operation in (c). You may neglect the delays caused by the Opamp comparator, DAC and the AND gate.
e) What will be the maximum time taken (in µsec) to digitize the highest V_A value?


Clock
V_A
+
Op amp
−
EOC
Comparator
RESET
V_{AX}
D/A
converter
Counter
CLOCK
Digital
result
SOC