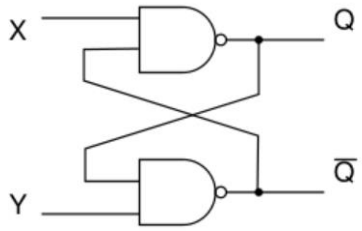
EE 103 – Intro to Electrical Enggineering 2022-23/I

Problem Sheet: Digital Electronics

Topics: Sequential Circuits – NAND latch, SR Flip-flop, JK flip-flop, D-flip-flop

Part A– Latches and Flip-flops

1. The circuit diagram of a NAND latch is shown below.



a) Assume that initially $Q = 1$ and $\bar{Q} = 0$. Analyze the NAND latch and verify that if the inputs are $X = 0\ and\ Y = 1$, then the outputs will continue to be at the same states.

b) Verify again that if now the inputs are made $X = 1\ and\ Y = 1$, then also the outputs $Q\ and\ \bar{Q}$ will remain at the same state as before.

c) Now change input conditions to $X = 1\ and\ Y = 0$. Analyze the circuit and determine the outputs $Q\ and\ \bar{Q}$.

d) Verify again that if now the inputs are made $X = 1\ and\ Y = 1$, then the outputs $Q\ and\ \bar{Q}$ will remain at the same state as before.

e) Now change input conditions to $X = 0\ and\ Y = 0$. Analyze the circuit and determine the outputs $Q\ and\ \bar{Q}$.

f) Find out what will happen if now the inputs are made $X = 1\ and\ Y = 1$. (If you analyse the circuit now to determine $Q\ and\ \bar{Q}$, you will see that you get two valid sets of results, i.e. $Q = 1$ and $\bar{Q} = 0$ or $Q = 0$ and $\bar{Q} = 1$).

Note: The above inconsistent result is one of the main reasons for not allowing the input condition $X = 0\ and\ Y = 0$. In actual practice, when the condition mentioned in (e) is followed by (f), then NAND gate with the shorter propagation delay would force its output to be '0'. Accordingly, the second NAND gate output would become '1'.

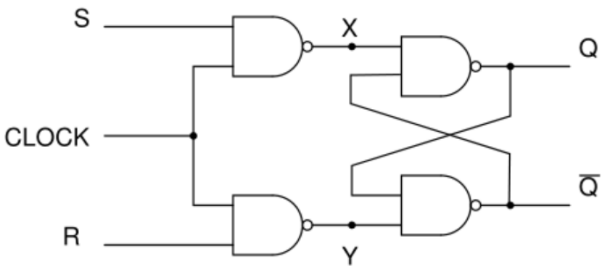
The second reason why the input condition $X = 0\ and\ Y = 0$ is not allowed is that for other except this input condition the outputs of the NAND latch are complimentary. In sequential circuits this property of the outputs being complementary is very useful.

For the above two reasons, we write the input condition $X = 0\ and\ Y = 0$ as 'Not allowed'.

2. The schematic diagram of an SR flip-flop is shown below. Analyse the circuit and write the truth table for the same (Inputs: S, R and CLOCK; Outputs Q *and* $\bar{Q}$).

a) For which input condition do you find inconsistency in the Q *and* $\bar{Q}$ outputs?

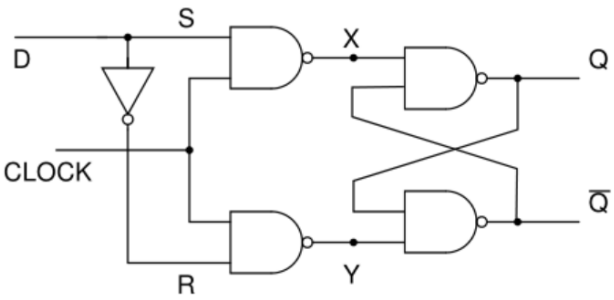
b) Based on the above truth table define what is the role of the Clock input, also for what condition of the Clock (i.e. High, Low or +ve or -ve edge) the flip-flop is able to operate normally.



3. An SR flip-flop modified to give is a D flip-flop shown below.

a) Write the truth table for this flip-flop.

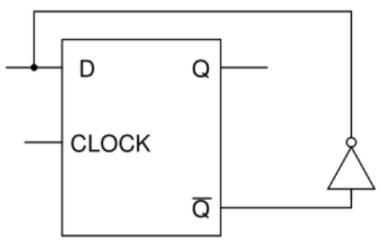
b) What is the utility of this flip-flop? A common question/confusion by students is that since in a D flip-flop, output is the same as the input, why do we use this flip-flop? Go through the reference material uploaded on Moodle and find at least two major applications of the D flip-flop.



4.An interesting application of the D flip-flop is shown below. Assume that the input Clock signal is a square wave of 1 kHz (i.e. Clock High = Clock Low = 0.5 msec). Assume that the D flip-flop used here is the same as used in problem 3.

a) Sketch the Q output with respect to the Clock for at least eight clock periods. Assume that initially Q = '0'. What is the frequency of the waveform at the Q output?

b) Assume that the Clock signal is now changed to a waveform of 1 kHz, but with Clock High = 0.25 msec, Clock Low = 0.75 msec. Sketch the Q output with respect to the Clock for at least eight clock periods. Assume that initially Q = '0'. Based on the Q output waveforms you obtained in (a) and (b) name two interesting applications of the circuit shown.



5. A D flip-flop application, similar to the one in problem 4 is shown below. Here instead of the of the Clock level sensitive D flip-flop used in problem 4, a +ve edge triggered D flip-flop is used.

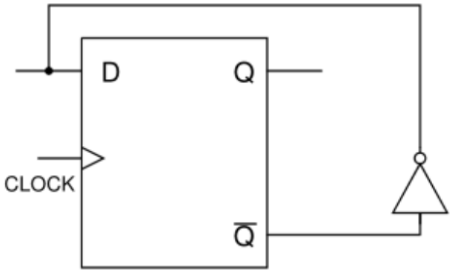
a) Sketch the Q output with respect to the Clock for at least eight clock periods. Assume that initially Q = '0'. What is the frequency of the waveform at the Q output?

b) Assume that the Clock signal is now changed to a waveform of 1 kHz, but with Clock High = 0.25 msec, Clock Low = 0.75 msec. Sketch the Q output with respect to the Clock for at least eight clock periods. Once again assume that initially Q = '0'.

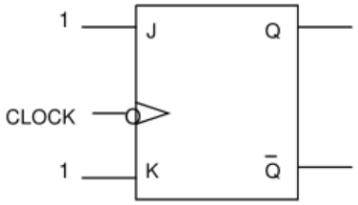
c) Is there any difference in the waveforms you got in this problem compared to the ones you got for problem 4? Justify your answer.

d) If instead of the +ve edge triggered flip-flop shown, if a -ve edge triggered D flip-flop is used for the cases 5(a) and 5(b), what will be the difference in the Q output waveforms compared to the +ve edge triggered case?

e) Refer to the reference material uploaded on Moodle and find out what is the advantage in using edge-triggered flip-flops instead of level sensitive flip-flops.



6. A JK flip-flop circuit is shown below where J = 1, K =1 and the given JK flip-flop is a negative edge-triggered flip flop. Assume that the Clock input is a 10 kHz square wave signal. Sketch the Q output with respect to the Clock for at least eight clock periods. Assume that initially Q = '0'. What is the frequency of the waveform at the Q output?



7 C) A latch circuit commonly used for generating manual clock is shown below, where a spring-loaded single-pole double-throw (SPDT) switch is used. This switch has three contacts, viz. Common (COM), Normally-Open (NO), and Normally-closed (NC).

i) In the switch position is as shown in the figure, what will be the Q output and the state of the LED (ON or OFF)?

ii) In the switch position as shown, what will be the currents flowing into the Std TTL NAND gate inputs connected to NO and NC? Std TTL gate current specifications: I_{OH} = 400 μA, I_{OL} = 16 mA, I_{IH} = 40 μA, I_{IL} = 1.6 mA.

iii) Why is such a latch circuit required for generating clock manually with each press; instead why not just use the switch (with connections to +5V) for generating clock pulse with each press?