EE 103 – Intro to Electrical Engg : 2023-24/I - Autumn

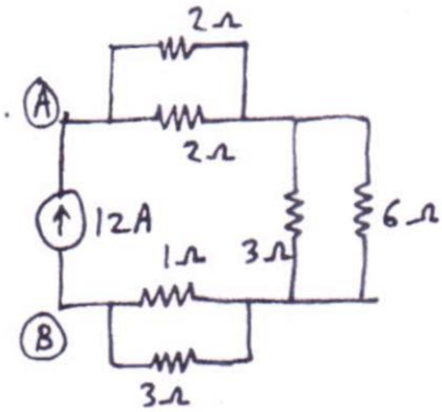
Analog Electronics - Practice Problems (with numerical answers)

Sep 2, 2023

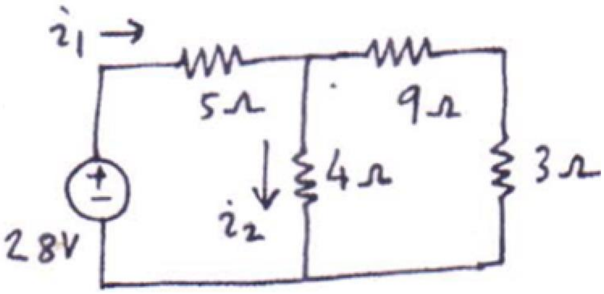
Part A : Circuit Theory

Mesh Analysis

1. Find the voltage V_{AB}, i.e. the voltage across A and B nodes.
   (Answer: V_{AB} = 45 V)

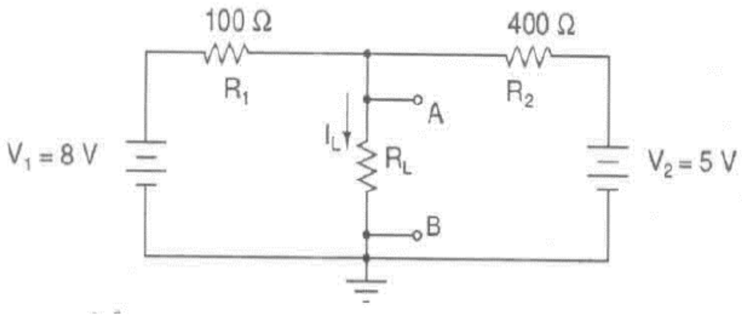


2. Find i_1 and i_2 using mesh analysis. (Ans: i_1 = 3.5 A, i_2 = 2.625 A)



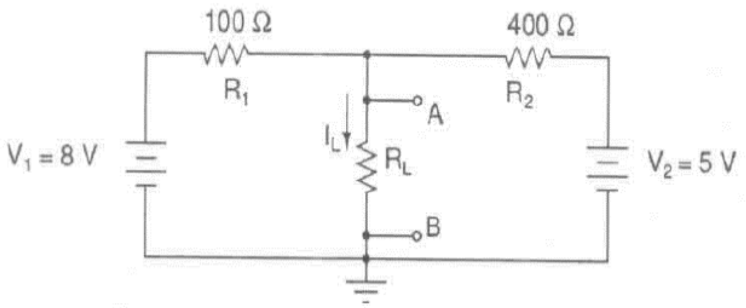
<u>Node Voltage Method</u>

3. In the circuit shown below, using the node voltage method, determine I_L for R_L = 200 ohms. (Ans: I_L = 26.43 mA)



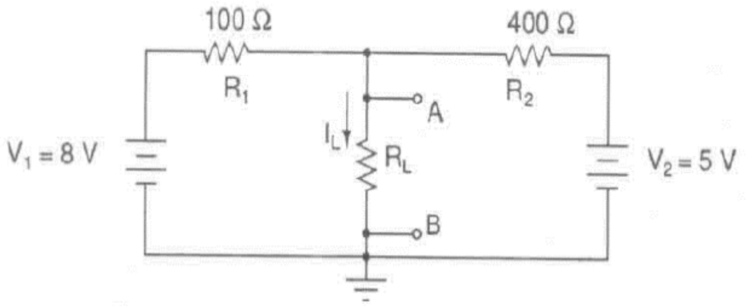
Thevenin's theorem

4. For the circuit shown in the figure,
   i) Find the Thevenin's equivalent circuit across the terminals A and B.
   ii) Using Thevenin's equivalent circuit find I_L for: a) $R_L = 100\ \Omega$ and b) $R_L = 80\ \Omega$.
   (Ans: (i) $V_{Th} = 7.4$ V, $R_{Th} = 80\ \Omega$; (ii) a) 41.11 mA b) 46.25 mA)



Superposition Theorem

5. In the circuit shown below, using superposition theorem determine I_L for $R_L = 400\ \Omega$.
   (Ans: I_{L1} (with V_2=0) = 13.33 mA, I_{L2} (with V_1 =0) = 2.08 mA; $I_L = I_{L1} + I_{L2}$ = 15.4 mA)



Part B - Transient Response of RC Circuits

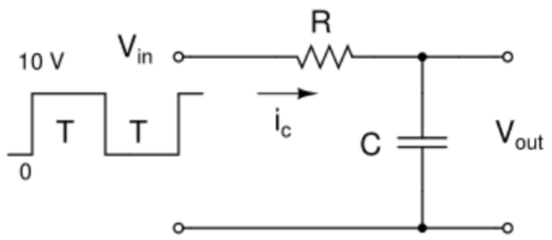
RC Integrator circuits

1. An RC integrator circuit is shown below. R = 10 kΩ, C = 0.1 μF. Evaluate and sketch the voltage (V_{out}) and current (i_c) waveforms for the following RC integrator circuit for the following cases:

a) T = 5 msec
b) T = 1 msec

The input (V_{in}) is a square-wave signal (with equal high and low time intervals T), with a low-level amplitude of 0 volts and high-level amplitude 10 V.

Hints:
i) In an RC circuit steady state voltage and current are reached when $T = 5\tau$. For cases with $T < 5\tau$, it has to be computed iteratively or analytically.
ii) Use the capacitor equation to solve RC time response circuits.
$V_c = V_f + (V_i - V_f) \exp(-t/RC)$, where V_c = capacitor voltage being evaluated, V_i = initial voltage, V_f = final voltage
iii) Voltage across a capacitor cannot change instantaneously, but current can.



Answer:
Case a (T = 5 msec) : τ = 1 msec. Steady state is reached in each half cycle. Hence V_{out} = 10 V (end of +ve half cycle), and V_{out} = 0 V (end of the 2nd half cycle)

Case a (T = 1 msec) : τ = 1 msec. Steady state is not reached in each half cycle. The steady state values can be analytically arrived at or evaluated numerically in an iterative fashion using the equation for the voltage across a capacitor.
Iteratively, V_{out} = 6.32 V (end of first +ve half cycle), V_{out} = 2.33 V (end of the 2nd half cycle), V_{out} = 7.18 V (end of the 3rd half cycle), V_{out} = 2.64 V (end of the 4th half cycle), etc

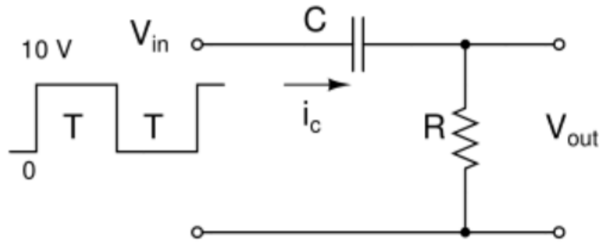
RC Differentiator circuits

2. An RC differentiator circuit is shown below. R = 10 kΩ, C = 0.1 μF. Evaluate and sketch the voltage (V_{out}) and current (i_c) waveforms for the following RC integrator circuit for the following cases:

a) T = 5 msec
b) T = 10 msec

The input (V_{in}) is a square-wave signal (with equal high and low time intervals T), with a low-level amplitude of 0 volts and high level amplitude 10 V.

Hint: In an RC circuit steady state voltage and current are reached when T = 5τ. For cases with T < 5 τ, it has to be computed iteratively or analytically.



Answer:
Case a (T = 5 msec) : τ = 1 msec. Steady state is reached in each half cycle. Hence V_{out} = 10 V (at t = t_{0+} which decays to 0 V at the end of the 1st half cycle), and V_{out} = -10 V (at t = $(t_0 + T)_+$ which charges to 0 V at the end of the 2nd half cycle, and the cycle repeats).

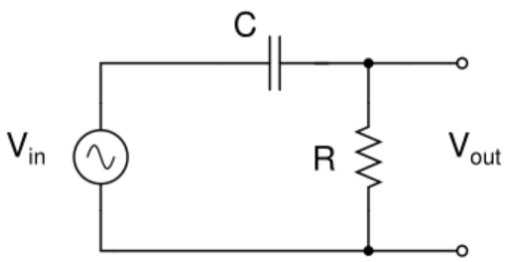
Case a (T = 1 msec) : τ = 1 msec. Steady state is not reached in each half cycle. The steady state values can be analytically arrived at or evaluated numerically in an iterative fashion using the equation for the voltage across a capacitor.
At the transitions of V_{in}, there will be a 10 V jump (+ve jump or -ve jump for +ve going and -ve going edges respectively). After the jump, the capacitor charges or discharges as the case may be.
Iteratively, V_{out} = 10 V (at t = t_{0+} which decays to 3.68 V at the end of the 1st half cycle), and

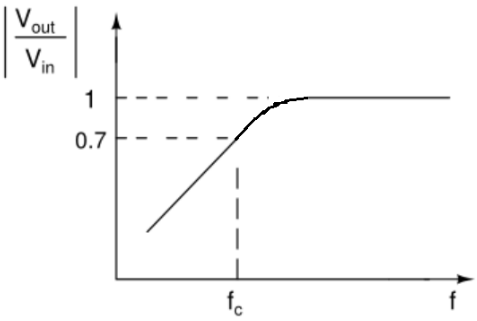
V_{out} = (3.68-10) = -6.32 V (at t = (t_0 +T)$_+$ which charges to -2.33 V at the end of the 2nd half cycle, and V_{out} = (-2.33 +10) = 7.67 V (at t = (t_0 +2T)$_+$ which discharges to 2.82 V at the end of the 3rd half cycle, etc.

Part C – Frequency Response of RC Circuits

1. The circuit diagram of an RC high-pass filter is given below. For a sinusoidal input voltage, sketch the magnitude plot of V_{out}/V_{in} as a function of frequency. The cut-off frequency of the filter is $f_c = 1/(2\pi RC)$. The component values are: C = 0.2 μF, R = 2 kΩ.

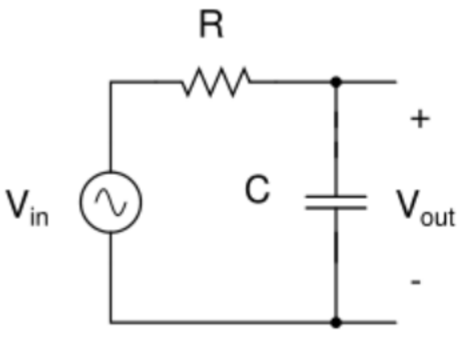
(Ans: f_c = 397.89 Hz. Magnitude of (V_{out}/V_{in}) will be 0.707 at f_c, and 1 for f >> f_c. For f < f_c, the magnitude drops below 0.707 and approaches 0 at very low frequencies).

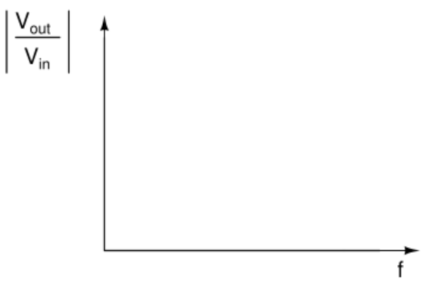




2. The circuit diagram of an RC low-pass filter is given below. For a sinusoidal input voltage, sketch the magnitude plot of V_{out}/V_{in} as a function of frequency. The cut-off frequency of the filter is $f_c = 1/(2\pi RC)$. The component values are: C = 0.1 μF, R = 10 kΩ.

(Ans: f_c = 159.15 Hz. Magnitude of (V_{out}/V_{in}) will be 0.707 at f_c, and 1 for f << f_c. For f > f_c, the magnitude drops below 0.707 and approaches 0 at very high frequencies).

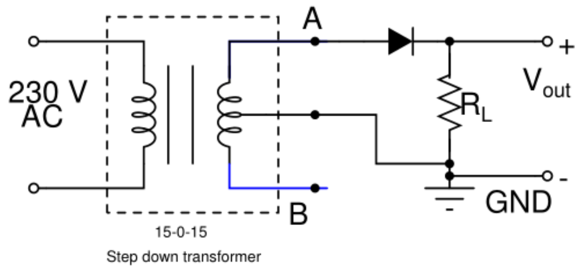




Part D – Unregulated DC Power Supply

Half-wave and Full-wave Rectifier Circuits

1. Sketch the V_A and V_{out} waveforms. Evaluate the average value of V_{out}.
   (Ans: $V_{out\,(avg)} = 15 \times sqrt(2)/\pi = 6.75$ V)



2. In the Bridge rectifier circuit shown below, sketch the V_{AB} and V_{out} waveforms. Evaluate the average value of V_{out}.

(Ans: $V_{out\,(avg)} = 2 \times 15 \times sqrt(2)/\pi = 13.50$ V)

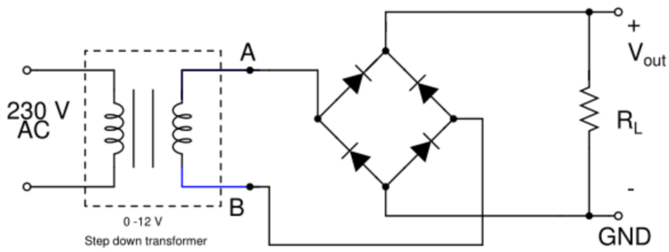


Fig D.2

3. Sketch the likely V_{out} waveforms of the full-wave rectifier circuit shown in Fig.D.3, for the following cases:

a) C is a large value (say 1000 μF), and R_L open circuit

b) C is a large value (say 1000 μF), and R_L = large value (say 10 kΩ)

c) C is a large value (say 1000 μF), and R_L = small value (say 100 Ω)

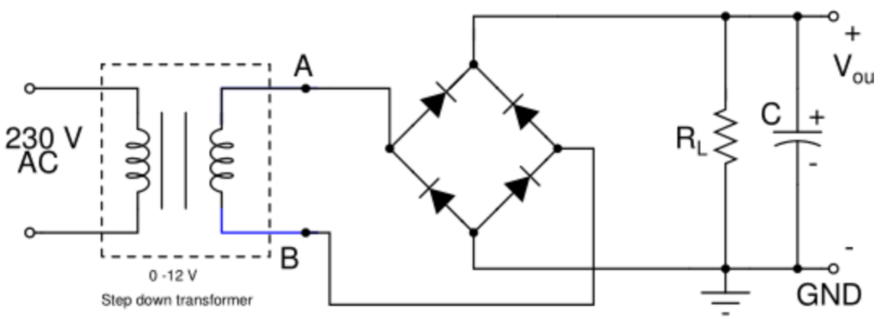


Fig D.3

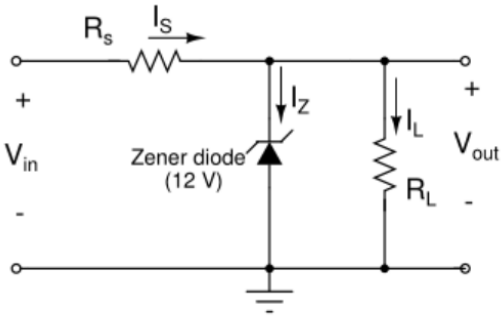
Part E – Regulated DC Power Supply (using Zener Regulator)

1. A Zener regulator circuit is shown below that uses a 12 V Zener diode. It has a resistance (R_Z) of 125 Ω in the Zener region. Other parameters are: Vin = 20 V, R_S = 470 Ω,

a) Evaluate V_{out}, I_S, I_Z, and I_L for $R_L = 1$ k Ω.

b) Evaluate V_{out}, I_S, I_Z, and I_L for $R_L = 4$ k Ω.

<u>Hint</u>: Find the Thevenin's equivalent across R_L and use it to evaluate the currents and voltages. For finding the Thevenin equivalent, replace the Zener diode with a battery of 12 V in series with 125 Ω (the resistance in the Zener region).



(Ans: V_{Th} = 13.68 V , R_{Th} = 98.74 Ω

R_L = 1 k Ω : V_{out} = 12.45 V ; I_S = 16.05 mA; I_Z = 3.6 mA and I_L = 12.45 mA

R_L = 4 k Ω : V_{out} = 13.35 V ; I_S = 14.15 mA; I_Z = 10.8 mA and I_L = 3.34 mA)

Part F – BJT DC Circuits

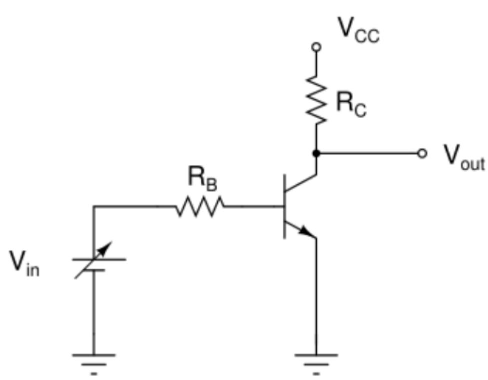
1. A BJT inverter circuit is shown below. Circuit values and BJT parameters are:

Circuit values: Vcc = 5 V, R_B = 20 kΩ, R_C = 1 kΩ

BJT parameters: β = 40, V_{BE} = 0.7 V, V_{CEsat} = 0.2 V

Analyse the circuit and sketch the VTC (voltage-transfer characteristic, i.e. V_{out} vs V_{in}) of the BJT inverter when V_{in} is varied from 0 to 5 V.

(Ans: V_{IL} = 0.7 V, V_{IH} = 3.1 V, V_{OL} = 0.2 V, V_{OH} = 5 V)



2. In the BJT inverter if the resistances R_C and R_B are changed to $R_C = 500\ \Omega$ and $R_B = 10\ k\Omega$, while keeping all the other parameters the same, once again sketch the VTC of the modified BJT inverter.

(Ans: $V_{IL} = 0.7$ V, $V_{IH} = 3.1$ V, $V_{OL} = 0.2$ V, $V_{OH} = 5$ V)

3. A BJT circuit is shown below in Fig.P3. Determine the currents I_C, I_B and I_E and the node voltages V_C and V_B. Circuit and BJT parameters are: Vcc = 12 V, $R_C = 1\ k\Omega$, $R_B = 50\ k\Omega$, $\beta = 40$, $V_{BE} = 0.7$ V, $V_{CEsat} = 0.2$ V. Comment on the mode of operation of the BJT.

<u>Hint</u>: Note in Fig.P3. $I \neq I_C$, but actually $I = I_E$
(Answers: $I_B = 124.18\ \mu A$; $I_C = 4.97$ mA ; $I_E = 5.09$ mA; $V_C = 6.91$ V; $V_B = 0.7$ V).

b) In the above circuit if R_C is now changed to 10 kΩ, while keeping all other circuit values and BJT parameters as earlier, determine once again the currents I_C, I_B and I_E and the node voltage V_C. Comment on the mode of operation of the BJT. What is the special feature of this circuit (from the point of view of biasing and the BJT mode).

(Answers: $I_B = 24.57\ \mu A$; $I_C = 0.98$ mA ; $I_E = 1.01$ mA; $V_C = 1.93$ V; $V_B = 0.7$ V).

4. A modified version of the circuit of Fig.P3 is shown in Fig.P4. Determine the currents I_C, I_B and I_E and the node voltage V_C and V_E. Circuit and BJT parameters are: Vcc = 12 V, $R_C = 1\ k\Omega$, $R_B = 50\ k\Omega$, $R_E = 2\ k\Omega$, $\beta = 40$, $V_{BE} = 0.7$ V, $V_{CEsat} = 0.2$ V. Comment on the mode of operation of the BJT.

(Answers: $I_B = 65.32\ \mu A$; $I_C = 2.61$ mA ; $I_E = 2.68$ mA; $V_C = 9.32$ V; $V_B = 6.06$ V ; $V_E = 5.36$ V).

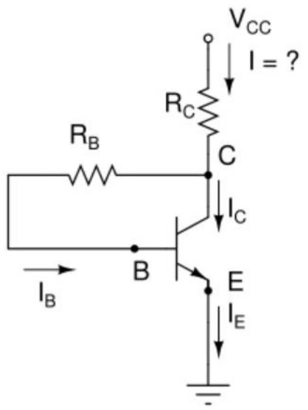


Fig. P3

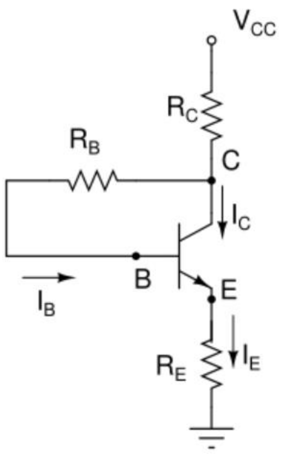


Fig. P4

Part G – Opamp Amplifier Circuits – Linear Applications

1. The circuit diagram of an Opamp inverting amplifier is shown below in Fig.P1. The circuit values are: +Vcc = +12 V, -Vcc = -12 V. R_1 = 5 kΩ, R_F = 50 kΩ. The input signal is V_{in} = 0.2 sin ωt V. Sketch the V_{in} and V_{out} waveforms. Assume that the maximum possible Opamp output levels possible are +/- Vcc.
   (Ans: Voltage gain Av = -10).

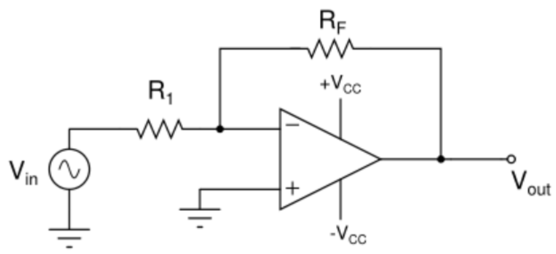


Fig. P1

2. For the circuit shown in Fig.P1, if now R_F is now increased to 500 kΩ, while keeping R_1 = 5 kΩ and Vin the same as in problem 5, sketch V_{in} and V_{out} waveforms. Explain the V_{out} sketch (as to why it is abnormal). Once again assume that the maximum possible Op amp output levels possible are +/- Vcc.
   (Ans: Voltage gain Av = -100; the positive and negative peaks as per calculation would be +20 and =20 respectively. Since Vout output levels cannot exceed +/- Vcc (+/- 12 V), Vout will get clipped beyond +/- 12 V).

3. Once again consider the inverting amplifier of problem 1, i.e. R_1 = 5 kΩ, R_F = 50 kΩ. However, for this case, the V_{in} signal is from a sensor, which has a Thevenin equivalent Voltage, V_{Th} = 0.1 V, and the Thevenin equivalent resistance, R_{Th} = 3 kΩ. What would be the Op amp output V_{out} for this case.
   (Ans: This would result in a voltage gain of $-[R_F/(R_1 + R_{Th})] = -[50/(5+3)] = -6.25$. Hence V_{out} will have less amplitude).

4. For the problem statement of 3, if a non-inverting amplifier is used (with the same voltage gain magnitude as of the original inverting amplifier) what would be V_{out}. Comment as to which amplifier, the inverting or the non-inverting amplifier is a better choice as a voltage amplifier.
   (Ans: The input resistance (= V_{in}/i_{in}) of an inverting amplifier equals the resistance connected to the input (=R_1 for problem 3). In the case of a non-inverting amplifier (assuming no resistance connected parallel to the input voltage Vin), the input resistance (= V_{in}/i_{in}) is ideally infinite, practically also very high. For a voltage amplifier, the input resistance should be as high as possible. Hence non-inverting amplifier is a better voltage amplifier in comparison to the inverting amplifier).

Part H – Op amp Circuits – Non-Linear Applications

1. An op amp comparator circuit is shown below.

Given: +Vcc = +12 V, -Vcc = - 12 V. Assume that the op amp is ideal. Also assume that the maximum and minimum V_{OUT} levels are +Vcc and -Vcc respectively.

For the given V_{IN} waveform sketch the V_{OUT} waveform by superimposing V_{OUT} on V_{IN}.