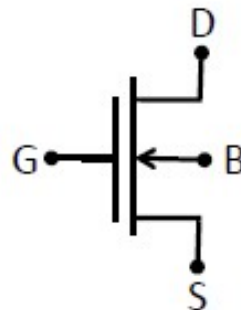
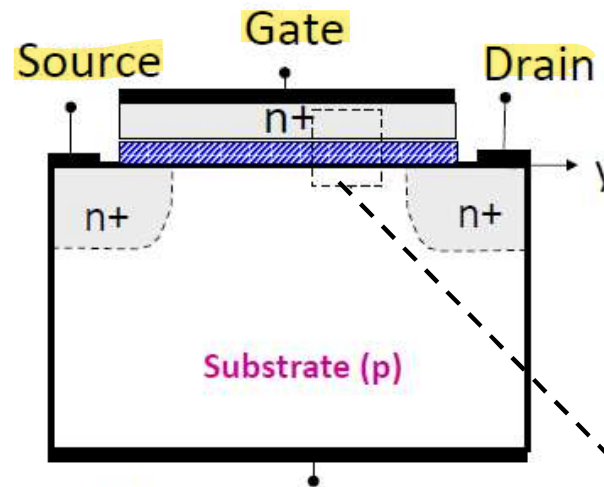
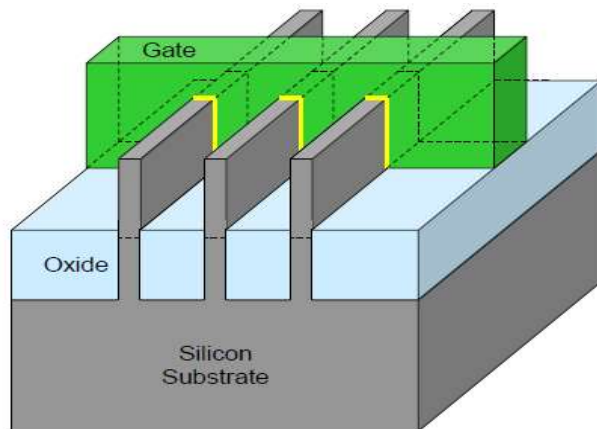
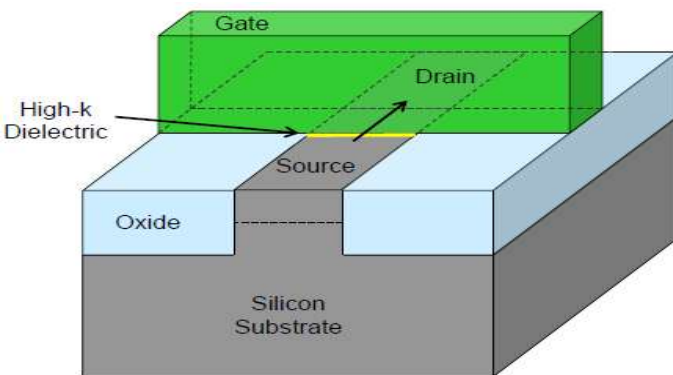


# MOS Field-Effect Transistor (MOSFET)

MOS-based devices (MOSFET, FinFET, Power-MOSFET...)

Low-power, integration

Digital logic/memory, analog, RF, power...

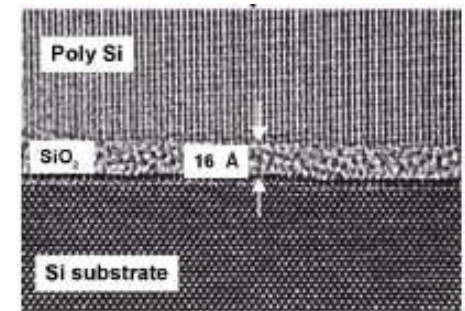


NMOSFET

PMOSFET?

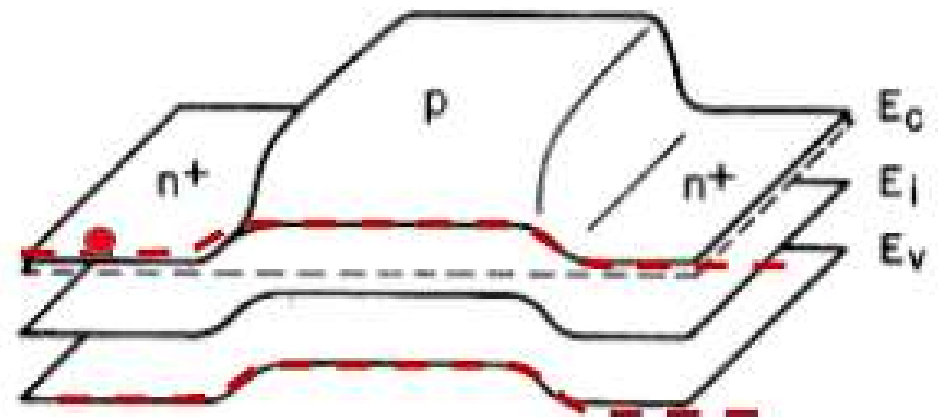
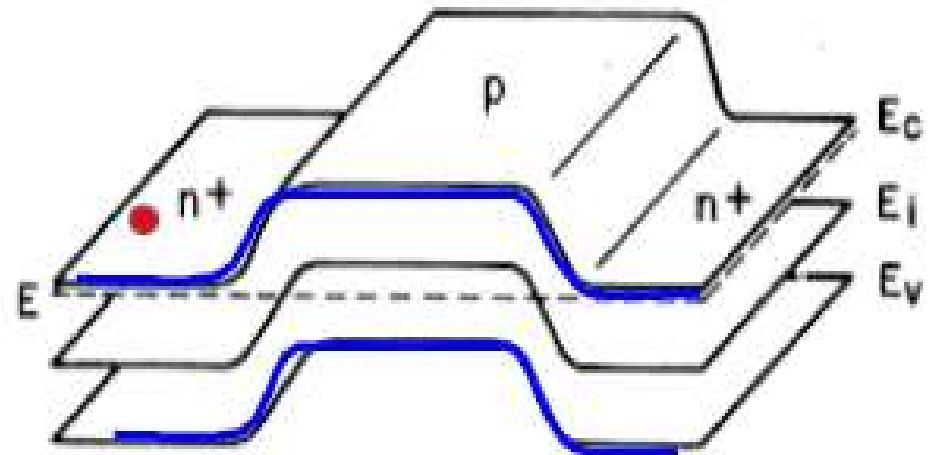
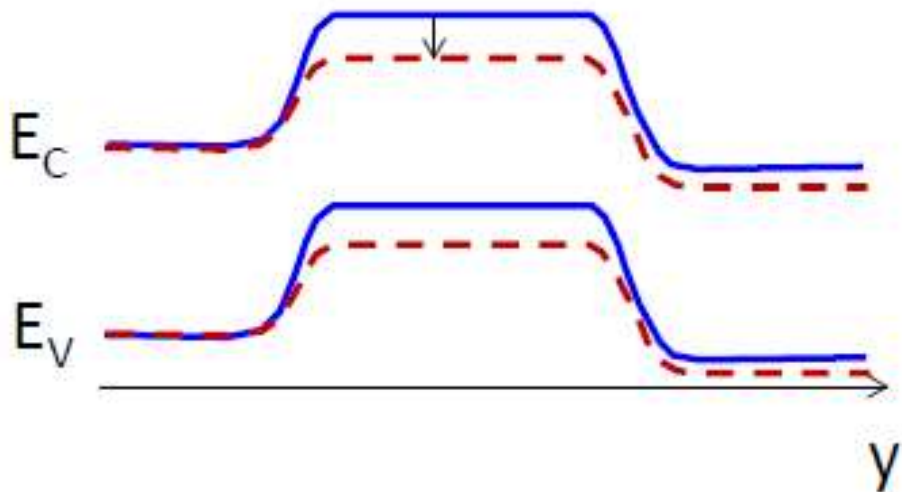
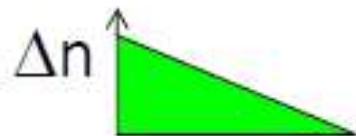
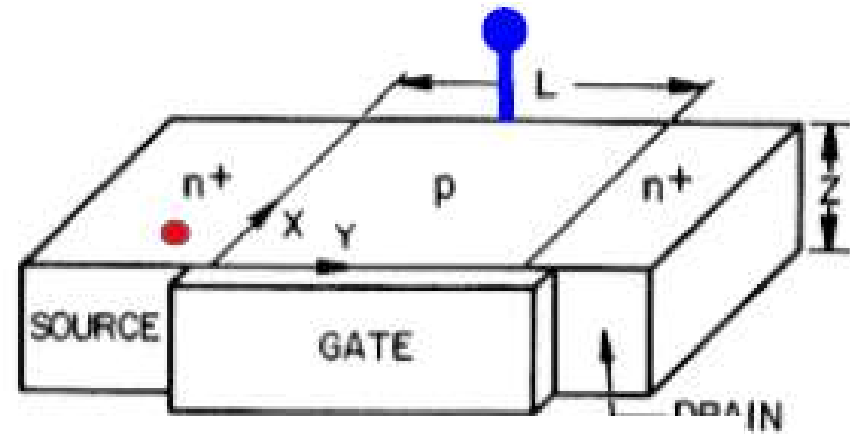
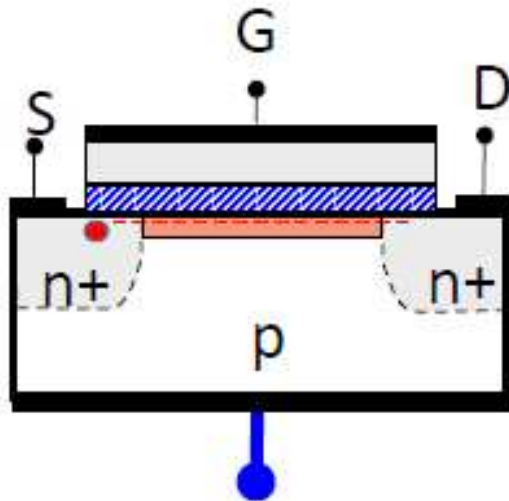
Charge-control

$$J = (Q) \otimes v$$

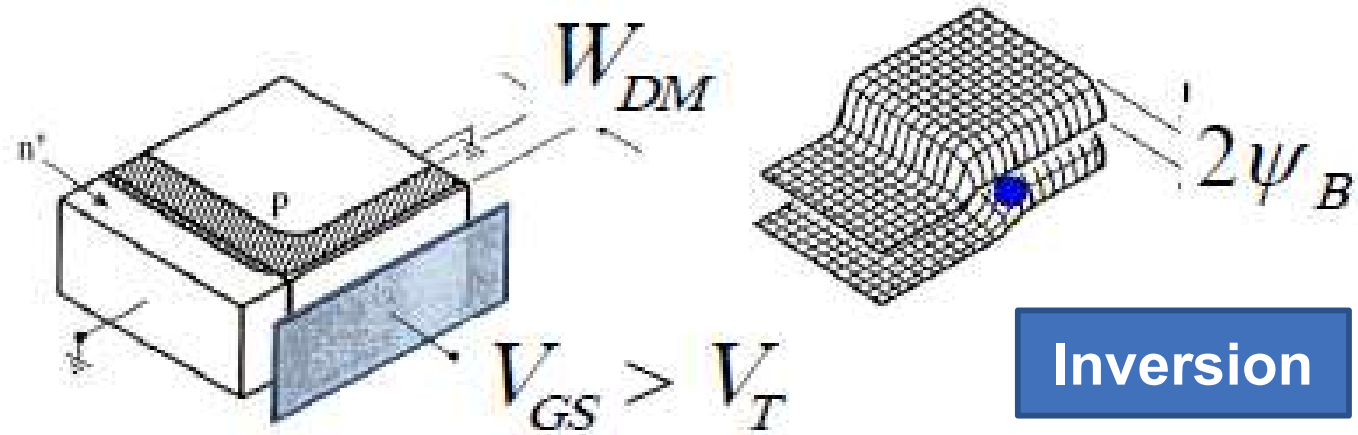
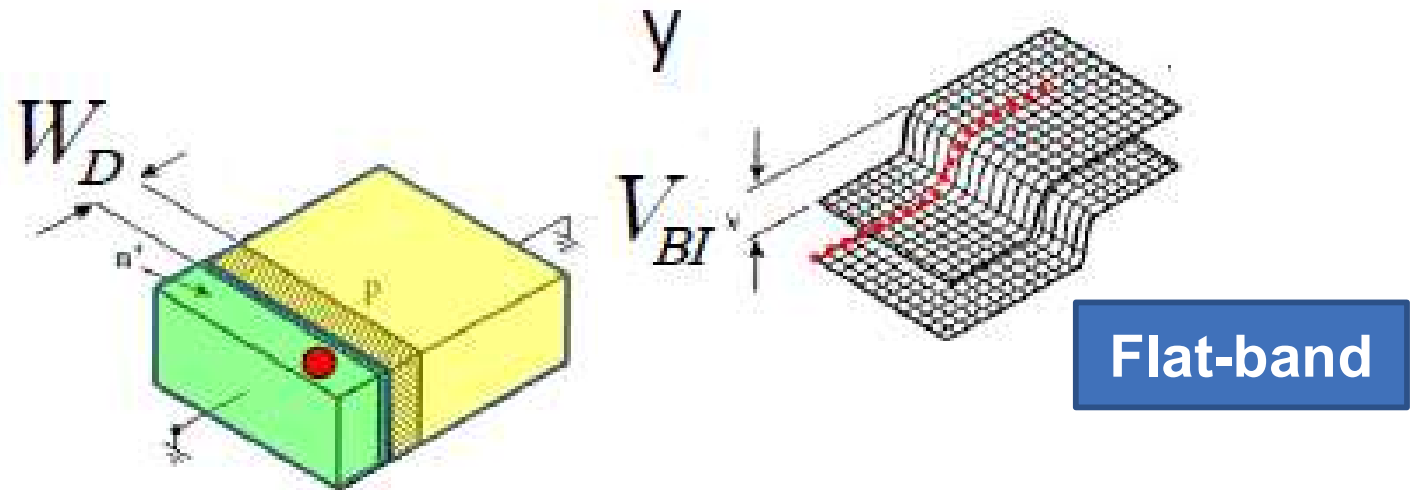
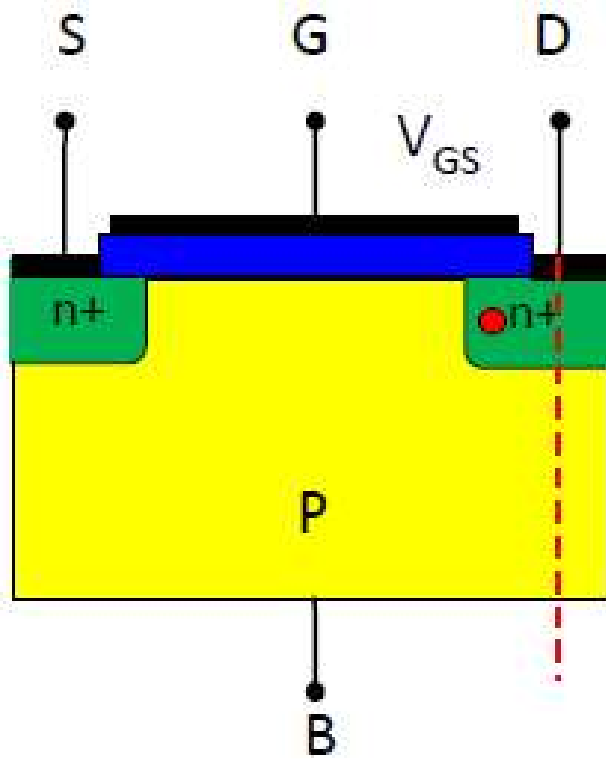


MOSCAP

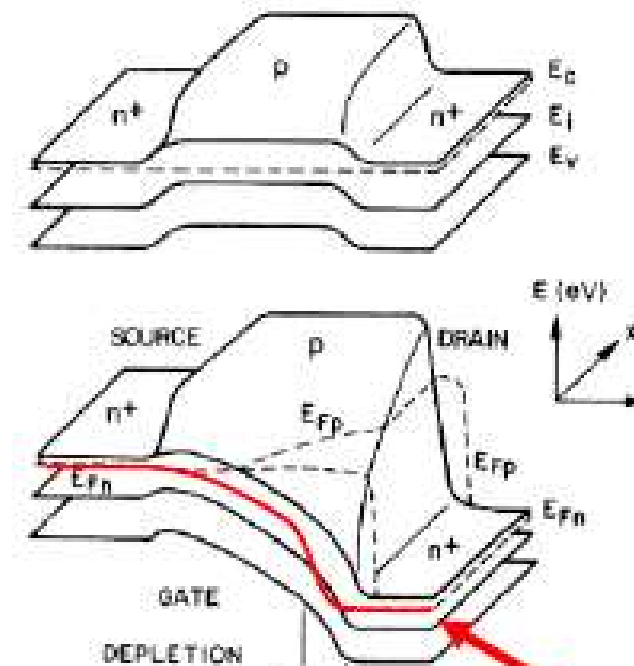
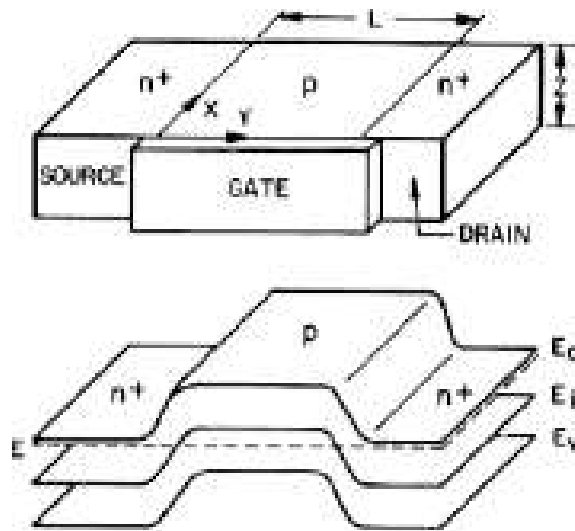
# Effect of bias



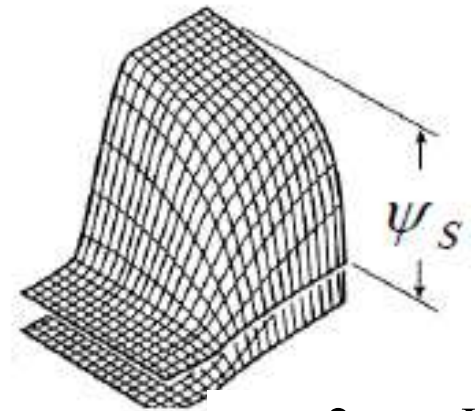
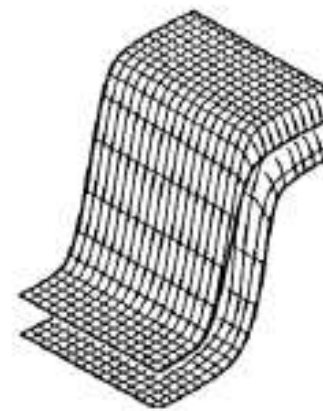
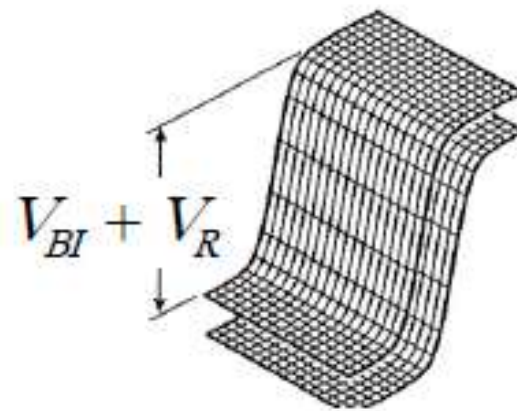
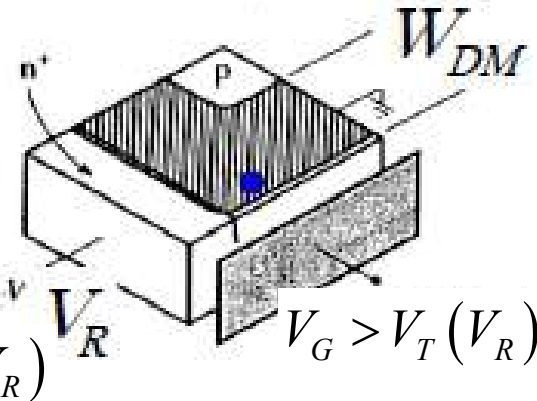
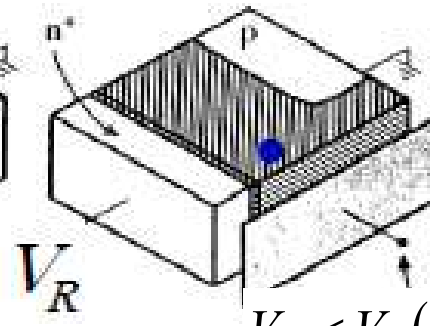
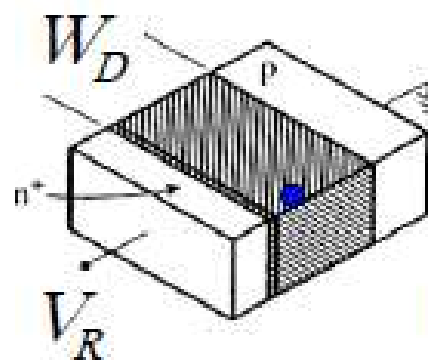
# Effect of gate-bias



# Effect of drain-bias



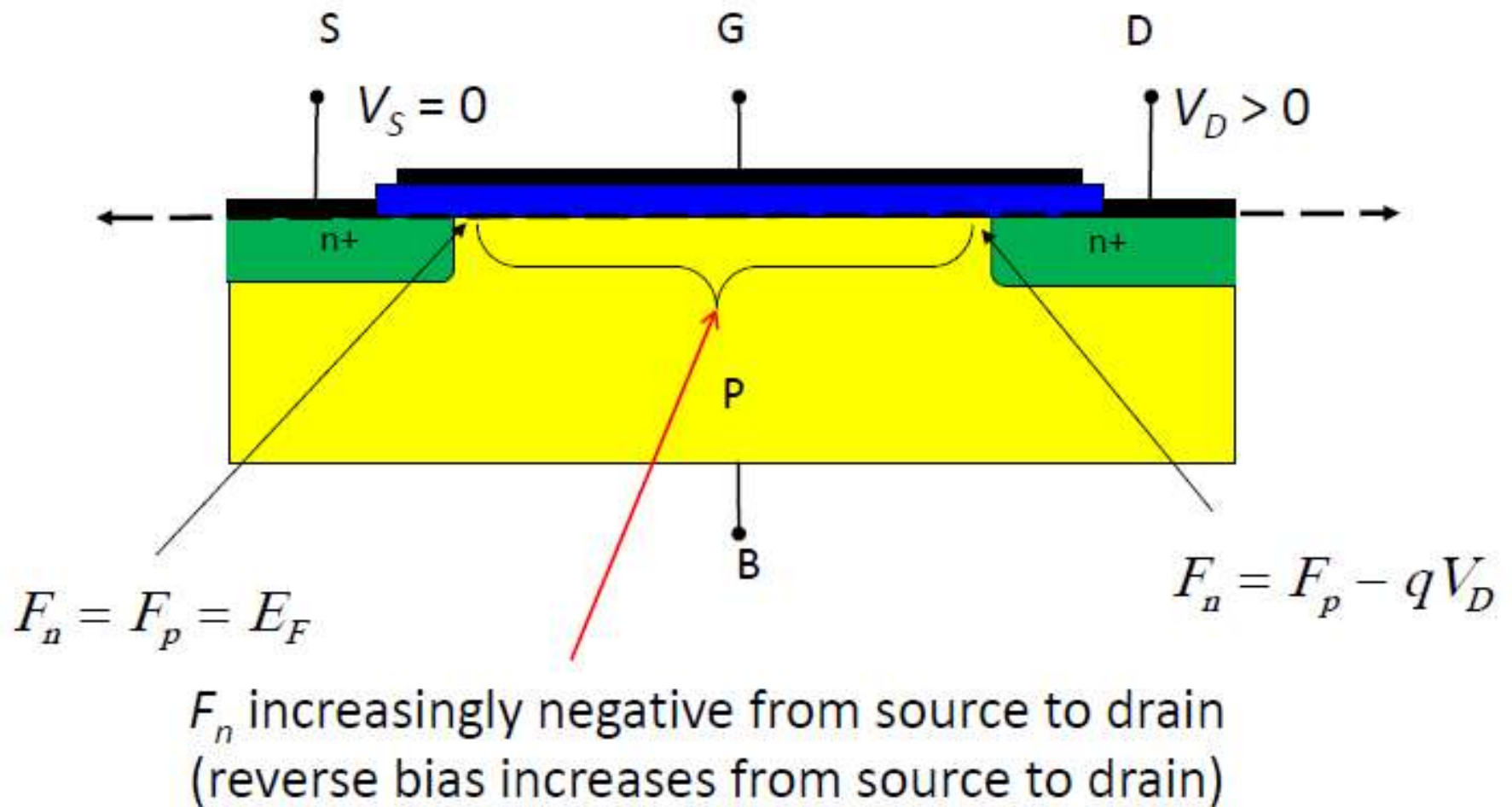
$$V_D > 0$$



$$\psi_S > 2\psi_B + V_R$$

$F_N$

# MOSFET I – V



# Depth-integrated current density

$$J_1 = Q_1 \mu \mathcal{E}_1 = Q_1 \mu \left. \frac{dV}{dy} \right|_1$$

$$J_2 = Q_2 \mu \mathcal{E}_2 = Q_2 \mu \left. \frac{dV}{dy} \right|_2$$

$$J_3 = Q_3 \mu \mathcal{E}_3 = Q_3 \mu \left. \frac{dV}{dy} \right|_3$$

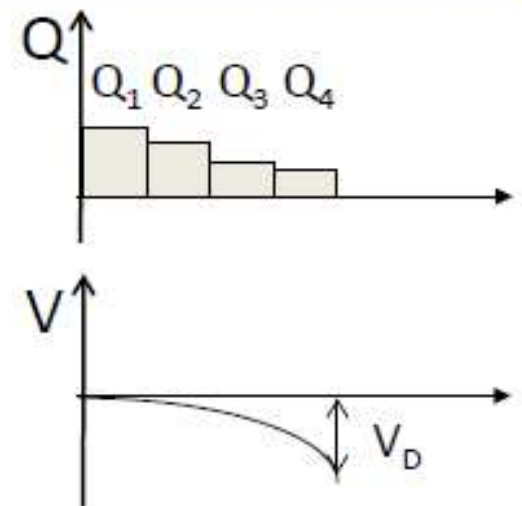
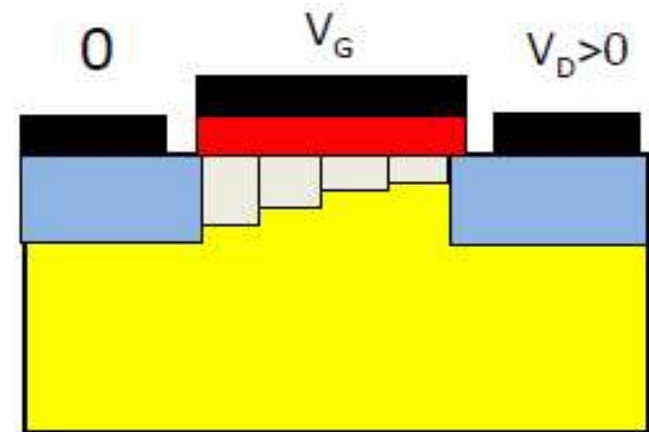
$$J_4 = Q_4 \mu \mathcal{E}_4 = Q_4 \mu \left. \frac{dV}{dy} \right|_4$$

$$\sum_{i=1,N} \frac{J_i dy}{\mu} = \sum_{i=1,N} Q_i dV$$

Gradual Channel

$$\frac{J_D}{\mu} \sum_{i=1,N} dy = \int_0^{V_D} C_{ox} (V_G - V_{th} - mV) dV$$

$$J_D = \frac{\mu C_{ox}}{L_{ch}} \left[ (V_G - V_{th}) V_D - m \frac{V_D^2}{2} \right]$$

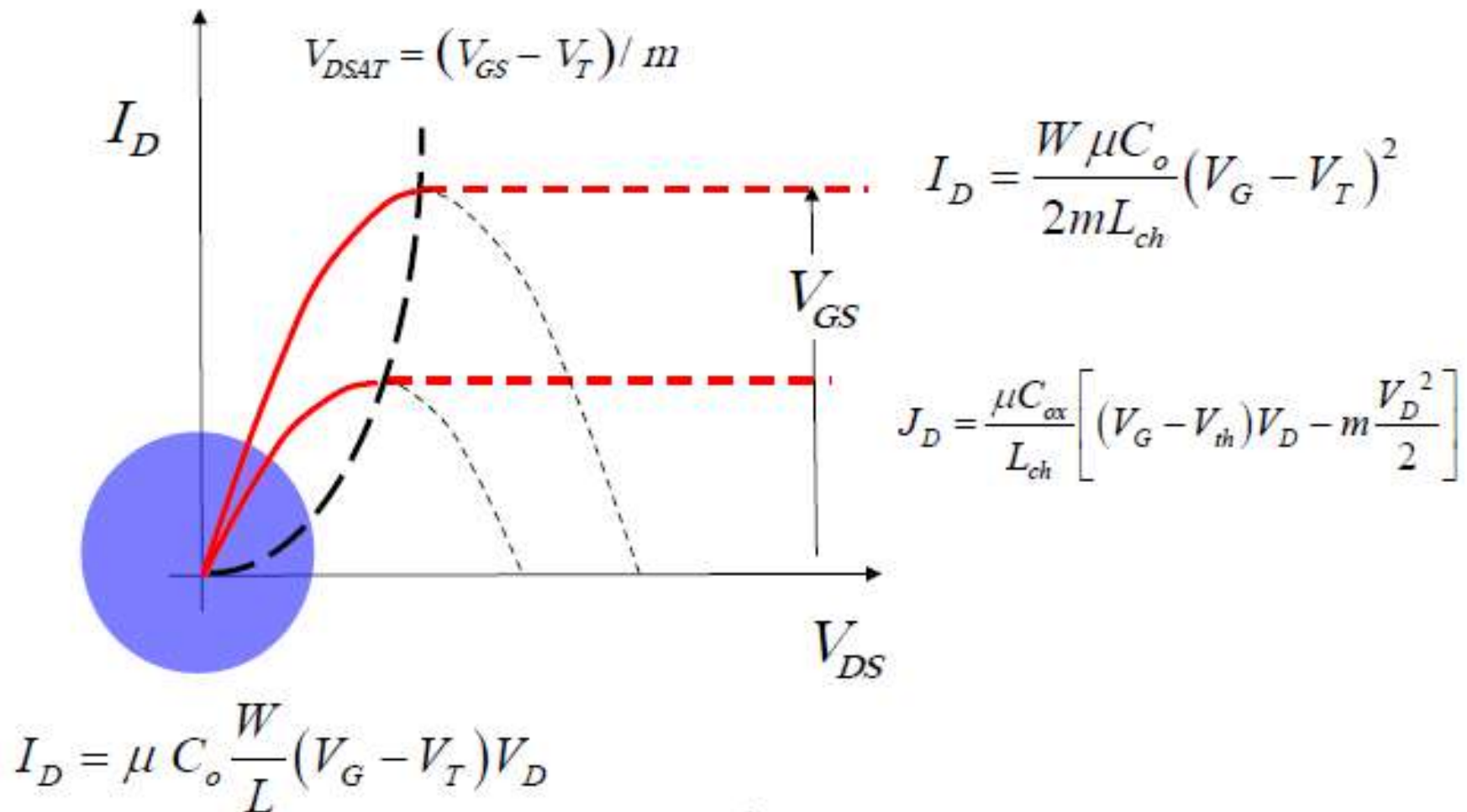




# Square-law I-V

$$I_D = W \frac{\mu C_{ox}}{L_{ch}} \left[ (V_G - V_{th}) V_D - m \frac{V_D^2}{2} \right]$$

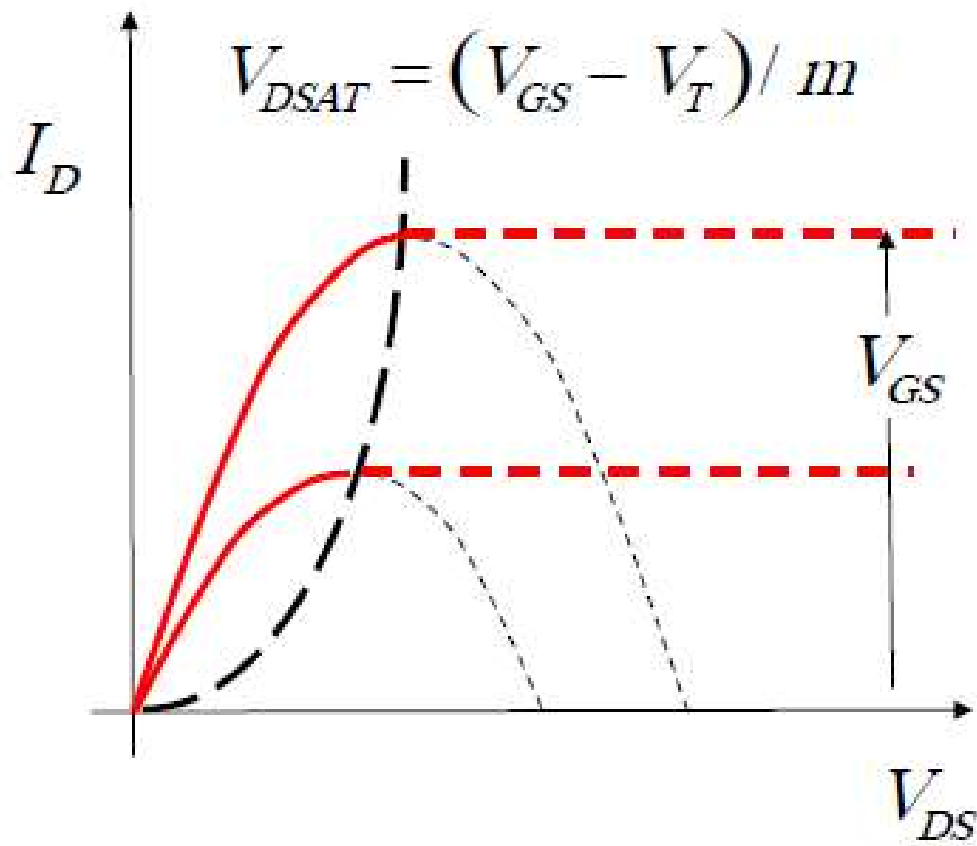
$$\frac{dI_D}{dV} = 0 = (V_G - V_{th}) - m V_D \Rightarrow V_{D,sat} = (V_G^* - V_{th}) / m$$



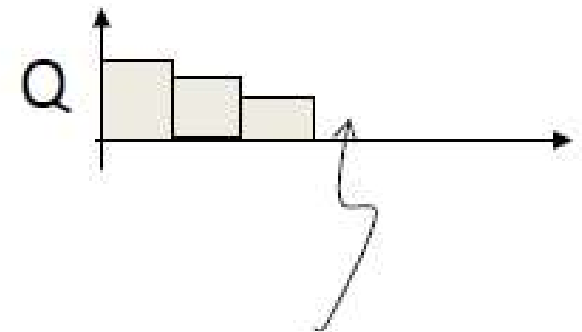
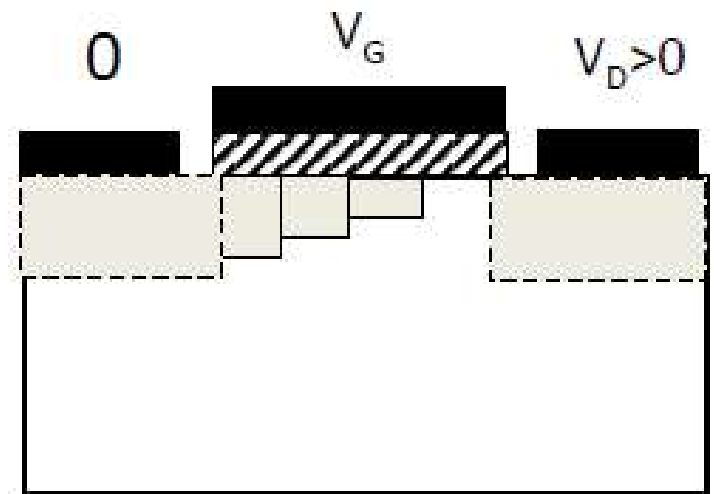
# Saturation and pinch-off

$$I_D = \frac{W \mu C_o}{2mL_{ch}} (V_G - V_T)^2$$

$$V_{DSAT} = (V_{GS} - V_T) / m$$



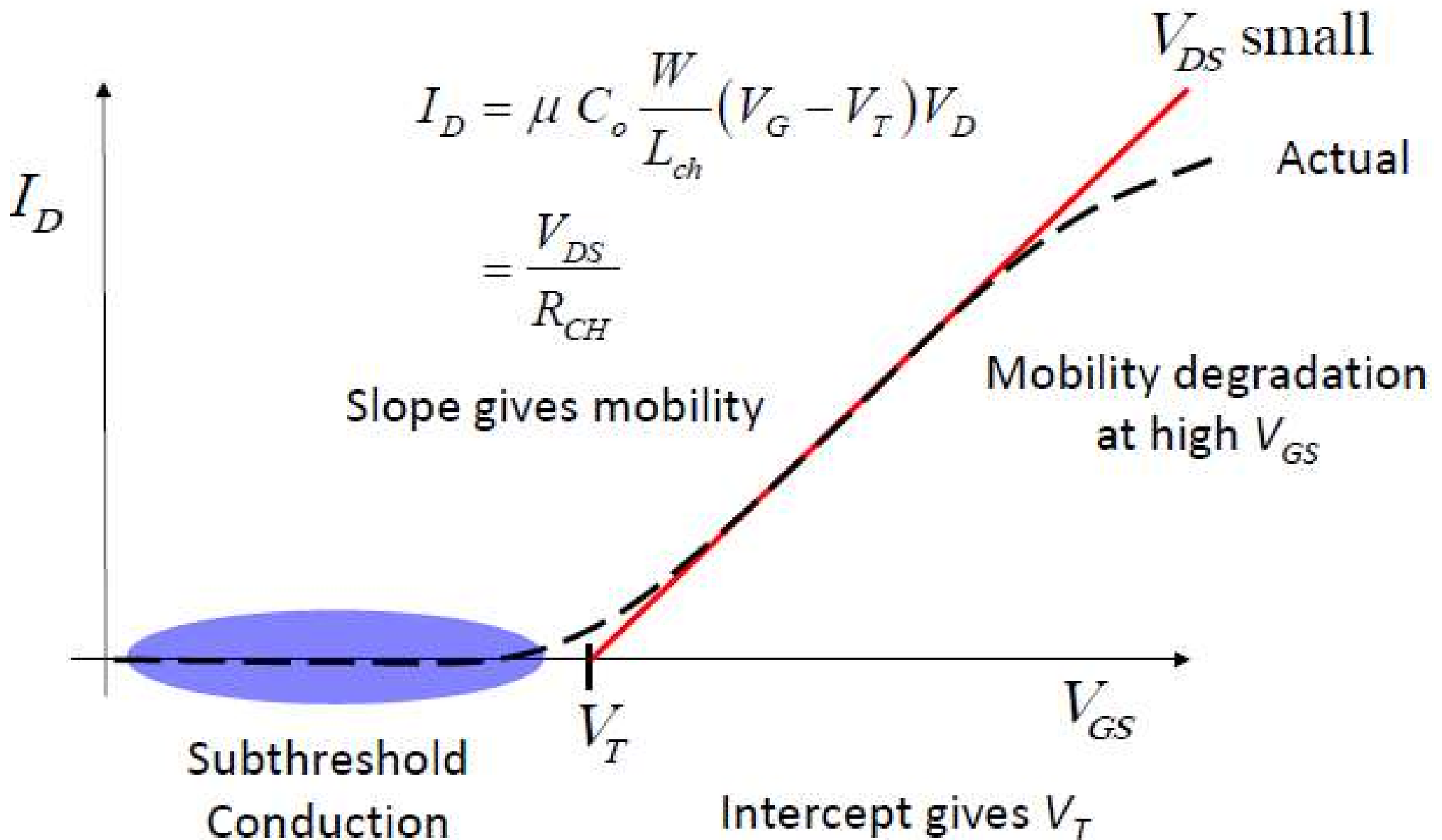
$$Q_i \approx -C_{ox} (V_G - V_{th} - mV)$$



loss of inversion



## Linear region (low $V_{DS}$ )



# Finis

## Sources:

1. Prof. M.A. Alam
2. [www.nature.com](http://www.nature.com)