EE 207 EXAM-II Solutions 09th Apr, 2025

(Time allowed is 120min. 1 single-sided A4 sized handwritten formula sheet is allowed.)

1. This problem is about designing a silicon p/i/n diode to withstand a reverse bias voltage of $V_R = 20V$. The design parameters are: N, the doping level in the n and p regions (assumed to be uniform and equal); and, W, the thickness of the i-region.

(a) Sketch the equilibrium band diagram for this device. [2]

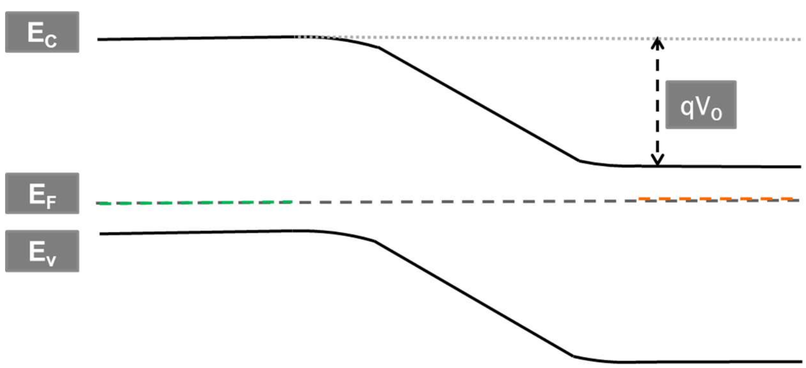
(b) Provide the values of N, W, and the maximum electric field in your design. Please keep in mind the following constraints. [8]

i. N should be in the range of $10^{16} cm^{-3} - 10^{18} cm^{-3}$.

ii. N should be as large as possible to minimize series resistance.

iii. N should not be so large that the maximum electric field in the device gets anywhere close to the critical electric field in silicon, viz. $3.10^5\ V.cm^{-1}$.

(a) The equilibrium band diagram is as follows. [2]



The corresponding electric field profile is as follows.

(b) To start with, we note that the built-in potential is $V_0 = \frac{kT}{q} ln\left(\frac{N}{n_i}\right) - \frac{kT}{q} ln\left(\frac{n_i}{N}\right) = \frac{2kT}{q} ln\left(\frac{N}{n_i}\right) = 0.84\ V$.

Here is one way to design the device. [8]

First, let us start by putting a cap on the maximum electric field. Suppose we aim to design the device so the field does not exceed $6.10^4\ V.cm^{-1} = E_m = 6.10^6\ V.m^{-1}$, the maximum electric field.

Second, let us say that we will use the mid-level doping allowed, viz. $N = 10^{17}\ cm^{-3} = 10^{23}\ m^{-3}$, so that I do not have to deal with the problem of degenerate doping.

Then, $E_m = qNX/\epsilon \Longrightarrow X = \epsilon E_m/qN = 39nm$

The voltage drop in the doped semiconductors is $V_{pn} = qNX^2/\epsilon = 0.23\,V$. As expected, the voltage drop is almost entirely in the i-region. Thus, $E_m W \approx V_R \Longrightarrow W = 20/(6.10^6)\ m = 3.3\ \mu m$.

Thus, in this design: $E_m = 6.10^4\ V.cm^{-1}; N = 10^{17}\ cm^{-3}; W = 3.3\ \mu m$

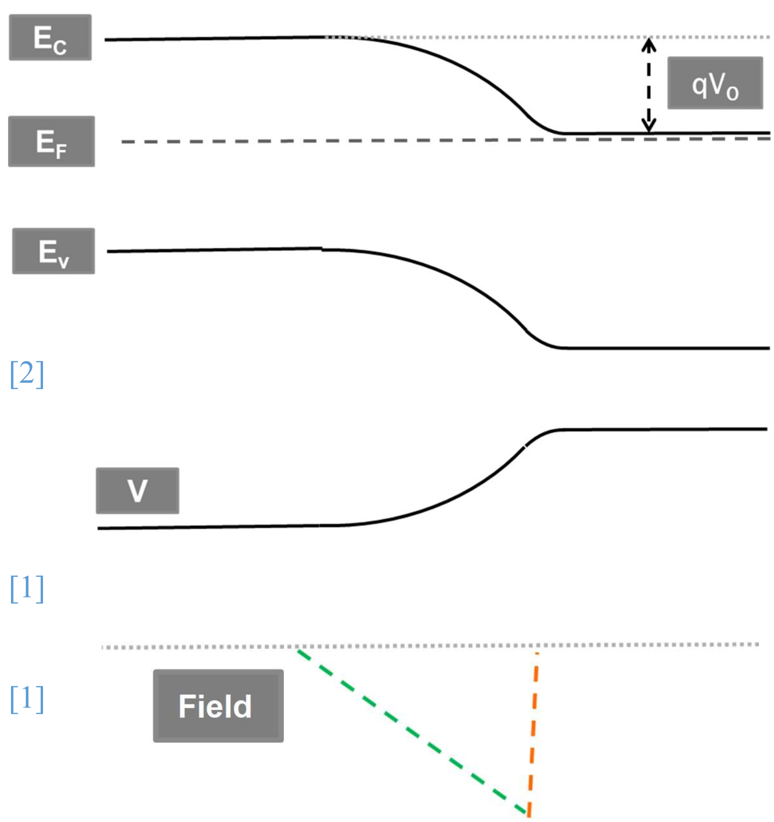
2. Consider an n$^+$/i homojunction in a semiconductor with bandgap $E_g = 1.6eV$, electron affinity $\chi_s = 4eV$, relative permittivity $\kappa_s = 12$, and intrinsic carrier concentration $n_i = 10^8 cm^{-3}$. Assume that the Fermi level in the bulk of the n$^+$ region coincides with the conduction band-edge there. Assume equal electron and hole effective mass in the semiconductor. Also, assume *equilibrium* for all parts of this question. For part (b) provide a numerical answer. $\varepsilon_0 = 8.854 \times 10^{-12}\, Fm^{-1}$

(a) Sketch the band-diagram, including the vacuum level. Also show the profiles of the potential and electric field in the semiconductor. [4]

(b) What is the built-in potential? [2]

(c) Write down the Poisson equation for the i-region. Eliminate the position variable in order to express it in terms of the electric field and potential. [4]

(a) The band diagram, potential, and field are as follows.



(b) The Fermi level on the n$^+$ side, before junction formation is: $E_{Fn} = E_C$

The Fermi level on the i-side, before junction formation is: $E_{Fi} = E_C - E_G/2$

Therefore, the built-in potential is given by: $V_0 = E_{Fn} - E_{Fi} = E_G/2 = 0.8eV$ [1+1]

(c) The Poisson equation in the i-region is $\frac{d^2V}{dx^2} = -\frac{q(p-n)}{\varepsilon}$

where the symbols have their usual meaning. Note that because it is not a doped material, there is no depletion charge; we can only have accumulation of carriers – electrons and/or holes, depending on the potential. [1+1]

Now, the position variable may be eliminated as follows:

$$\frac{dE}{dx} = \frac{q(p-n)}{\varepsilon}$$

$$\frac{dE}{dV}\frac{dV}{dx} = \frac{q\left(p_0e^{-qV/kT} - n_0e^{+qV/kT}\right)}{\varepsilon}$$ [1+1]

$$-E\frac{dE}{dV} = \frac{q\left(p_0e^{-qV/kT} - n_0e^{+qV/kT}\right)}{\varepsilon}$$

3. Consider metal-oxide-semiconductor (MOS) capacitors on n-type substrates that are ideal, meaning the workfunction of the metal and semiconductor are equal. Also assume no charge inside the oxide or at the interfaces.

(a) Suppose the semiconductor substrate is silicon, with doping of $N_d = 10^{17} cm^{-3}$; and the oxide is SiO_2, with $\varepsilon_r(SiO_2) = 4$, and thickness $t = 20nm$. Calculate the threshold voltage, and sketch the band diagram at threshold. [4]

(b) At threshold, what are the electric fields in the oxide, and at the semiconductor surface? [3]

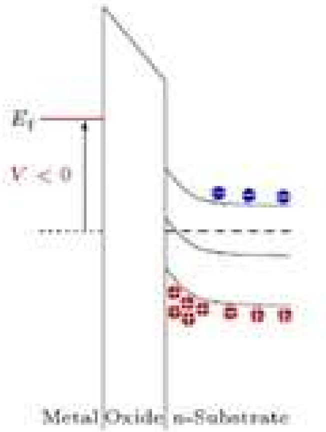
(c) What is the high-frequency small-signal capacitance above threshold? [3]

(a) The threshold voltage in this ideal case is given by: $V_T = -2\varphi_F - \frac{\sqrt{2\varepsilon_S q N_d |2\phi_F|}}{C_{ox}}$ [1]

$\lfloor\varphi_F\rfloor = \left(\frac{kT}{q}\right) ln\left(\frac{N_d}{n_i}\right) = 0.42V$

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = 1.77 \times 10^{-3}\ Fm^{-2}$$

$$\therefore V_T = -0.84\ V - \frac{\sqrt{2\varepsilon_S q N_d |2\phi_F|}}{C_{ox}} = -0.84\ V - 0.94\ V = -1.78\ V$$ [2]



[1]

(b) The electric field in the oxide is calculated as follows.

At threshold,

$$V_{ox} = \frac{\sqrt{2\varepsilon_s q N_d |2\phi_F|}}{C_{ox}} = 0.94\ V = E_{ox} t_{ox}$$ [1]

$$\therefore E_{ox} = \frac{V_{ox}}{t_{ox}} = \frac{0.94\ V}{20\times10^{-9} m} = \ 4.7 \times 10^7\ Vm^{-1} = 4.7 \times 10^5\ Vcm^{-1}$$ [1]

The semiconductor surface field is given by: $\epsilon_s E_s = \epsilon_{ox} E_{ox}$

$$\therefore E_s = \frac{\epsilon_{ox} E_{ox}}{\epsilon_s} = \frac{4E_{ox}}{11.7} = \ 1.6 \times 10^7\ Vm^{-1} = 1.6 \times 10^5\ Vcm^{-1}$$ [1]

(c) The high-frequency capacitance above threshold is given by:

$$C_{min} = \frac{C_{ox} C_s}{C_{ox} + C_s}$$ [1]

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = 1.77\ \times 10^{-3}\ Fm^{-2}$$

Now, $C_s = \frac{\epsilon_s}{W_m}$ where is the maximum depletion width.

$$W_m = \sqrt{\frac{2\varepsilon_s |2\phi_F|}{q N_d}} = 10^{-7}\ m \Longrightarrow C_s = \frac{\epsilon_s}{W_m} = 10^{-3}\ Fm^{-2}$$ [1]

$$C_{min} = 6.4\ \times 10^{-4}\ Fm^{-2}$$ [1]