EE 207 [Spring 24-25] ***HW-7***

1. Consider a long-channel silicon PMOSFET with a body doping of $10^{17} cm^{-3}$. The insulator is complex: it comprises 1nm of SiO_2 grown on the Si, and 4nm of a high-k dielectric XO_2 deposited on top of the SiO_2. Atop that, we have a metal (cobalt) gate, with a workfunction $\varphi_m = 5.0eV$. Assume no charge inside the oxide layers.

Si: electron affinity $\chi_{Si} = 4.05eV$, bandgap $E_g = 1.1eV$, permittivity $\in_{Si} = 11.8$, intrinsic carrier concentration $n_i = 1.5 \times 10^{10} cm^{-3}$, assume equal electron and hole effective mass

SiO_2: permittivity $\in_{SiO_2} = 3.9$, band-offsets with Si – $\Delta E_C = 3eV$, $\Delta E_V = 5eV$

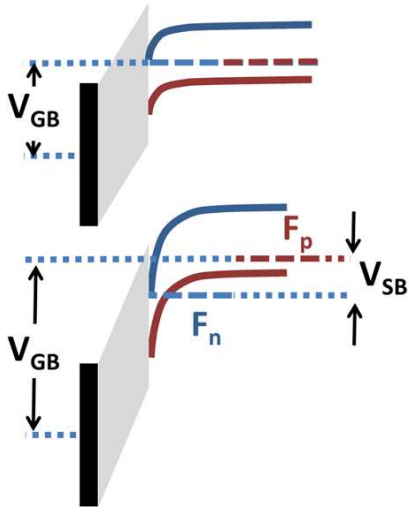
XO_2: permittivity $\in_{XO_2} = 7.8$, everything else same as SiO_2, no band-offsets with SiO_2

Free space permittivity $\in_0 = 8.85 \times 10^{-12} Fm^{-1}$

[You may use Boltzmann statistics for all calculations. Assume all interfaces are ideal.]

Calculate the flat-band voltage V_{FB} and threshold voltage V_T. Sketch the equilibrium band-diagram.

2. In order to control leakage in my CMOS based circuit, I use a body-biasing scheme, wherein a voltage is applied to the substrate (body) with respect to the grounded source, so as to increase the threshold voltage. This effect is illustrated with the band diagrams below.



First, explain the effect of body bias on theshold voltage intuitively through these band diagrams. Second, calculate the threshold voltage V_T, with and without the body bias.

The following parameters may be useful:

Parameter	Values
V_{FB}(V)	0
$\|2\varphi_F\|$ (mV)	200
$V_{ox}(\psi_s = \|2\varphi_F\|)$ (mV)	100
$\|V_{SB}\|$ (V)	1.6