EE 230 - Analog Lab
Wadhwani Electronics Laboratory
Electrical Engineering IIT Bombay

Lab: 10.a

Instructions:

- Use the model file uploaded on moodle along with this handout.
- Write down all your observations in your notebook.

Objectives:

- To design a basic Differential amplifier for given specifications
- To understand the working and design of an Operational Differential Amplifier
- Using Simulations to support analytical analysis.

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1. **Differential Amplifier with Resistive Load**

   (a) **Theory**
   Fig.[1] is a basic differential amplifier with a resistive load. M_1, and M_2 are input NMOS differential pair. R_2, R_3 are resistive loads to this differential pair. M_3 realizes the tail current source. R_1, M_3 and M_4 together realizes a current mirror. $V_{DD} = 10V$. A_1, A_2, and A_3 are ammeters used to measure respective branch currents (No need to connect ammeter explicitly in LTspice simulation). They don't play any role in differential amplifiers apart from measurement purposes.
   Required specifications:
   $Gain > 12dB$
   $V_{in,cm(min)} = 3.5V$
   $5V < V_{out,cm} < 7V$
   Follow the below design steps

   i. Minimum input common mode voltage is defined as the minimum voltage at which all the MOSFETs are in desired operating regions. In our case, saturation region. Let current from M_3 be I_{tail}. Thus $V_{in,cm(min)}$ can be written as

   $$V_{in,cm(min)} = V_{GS1} + V_{dsat3} \tag{1}$$

   $$V_{in,cm(min)} = V_{TH1} + \sqrt{\frac{I_{tail}}{K_{n1}}} + \sqrt{\frac{2I_{tail}}{K_{n3}}} \tag{2}$$

   Calculate the required I_{tail} to achieve the minimum input common mode specification. As a safety of margin, $V_{in,cm}$ will be greater than the calculated $V_{in,cm(min)}$ value.

   ii. Gain of differential amplifier, A_v can be written as

   $$A_v = gm1 * R_2 \tag{3}$$

   $$A_v = \sqrt{I_{tail}K_{n1}} * R_2 \tag{4}$$

   Calculate R_2 required to meet gain specification.

   iii. Output common mode voltage ($V_{out,cm}$) can be written as

   $$V_{out,cm} = V_{DD} - \frac{I_{tail}R_2}{2} \tag{5}$$

   Evaluate the $V_{out,cm}$ value. If it does not meet the specifications then redesign certain parameters to meet the specification. For example, if you have designed for a very high gain then you will probably get V_{outcm} lesser than the acceptable minimum value. This can risk M_1 and M_2 to be driven in the triode region. In this case, you can reduce the gain to increase V_{outcm}. It is common to get trade-offs between different specifications.

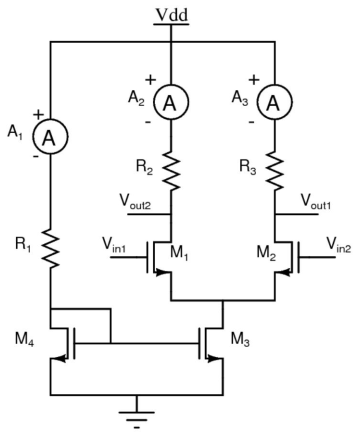

Figure 1: Basic Differential Amplifier

iv. Let the current through M_4 be I_{ref}. Calculate the value of R_1 to achieve desired I_{ref} value.

(b) **Simulation**

i. Draw a schematic for Differential Amplifier with resistive load circuit [1] in LT-Spcie. Apply $V_{in1} = V_{in2} = 4.5V, V_{dd} = 10V$. Ensure all the MOSFETs are in the saturation region. Each MOSFET should satisfy $V_{DS} > V_{GS} - V_{TH}$ condition to be in the saturation region. If any one of the MOSFET fails the condition then redesign the circuit.

ii. Tabulate all the node voltages, branch currents and operating region of MOSFETs. **[2 Marks]**

iii. Characterize the large signal behaviour of designed differential amplifier. Fix $V_{in2} = 4.5V$ and sweep V_{in1} from 0 V to 10 V. Plot the $(V_{out1} - V_{out2})$ vs $(V_{in1} - V_{in2})$ transfer characteristics curve. How should ideally transfer characteristics curve look like? **[2 Marks]**

iv. Apply 10 mV_{pp}, 1 KHz,sinusoidal differential input with 4.5 V common mode input voltage. Use 5 mV_{pp}, 1 KHz sinusoidal signal, with 4.5 V dc offset and apply it to V_{in1} and similarly apply 5 mV_{pp}, 1 KHz, 180 deg phase shifted sinusoidal signal, with 4.5 V dc offset to V_{in2}.

v. Plot the output V_{out1} and V_{out2} together. Observe the phase shift between two signals. Measure the differential gain. Compare with your hand calculations. **[2 Marks]**

2. **Differential Amplifier with active load**

(a) **Theory**

Differential amplifier with current mirror load [2] is also called a Five Transistor OTA (5T-OTA). It is a very useful topology to build an Operational Amplifier (Op-amp). M_1, M_2 are NMOS Differential pair. M_3, M_4 are the current mirror load. M_0 is a tail current source and M_5 mirrors the current to M_0. Tail current (I_0) is decided by the value of R_D.

i. **Gain**

Gain of 5T-OTA is given as $-g_{m1}(r_{o2}||r_{o4})$. r_o is defined as $\frac{1}{\lambda * I_d}$. This gain is highly dependent on channel length modulation coeffecient. You can get the values from the model file.

ii. **Output Common Mode Voltage ($V_{out_{dc}}$)**

Due to the negative feedback caused by the differential pair and current mirror, V_{out}, will be the same as V_{g3} in equilibrium condition (i.e. when $V_{in1} = V_{in2}$ and M_1, M_2 and M_3, M_4 are identical). V_{g3} can be expressed as $V_{DD} - V_{sg3}$. $V_{sg3} = \sqrt{\frac{I_0}{K_{n3}}} + V_{th3}$, where I_0 is the tail current source. Thus finally $V_{g3} = V_{out_{dc}} = V_{DD} - \sqrt{\frac{I_0}{K_{n3}}} - V_{th3}$

iii. **Input Common Mode Voltage**

Input common mode voltage (V_{incm}) should be such that all transistors should be in the saturation region. $V_{incm_{min}} = \sqrt{\frac{2I_0}{K_{n0}}} + \sqrt{\frac{I_0}{K_{n1}}} + V_{th1}$ and $V_{incm_{max}} = V_{out_{dc}} + V_{th1}$. Thus V_{incm} should be choosen in between these two limits.

(b) **Simulation**

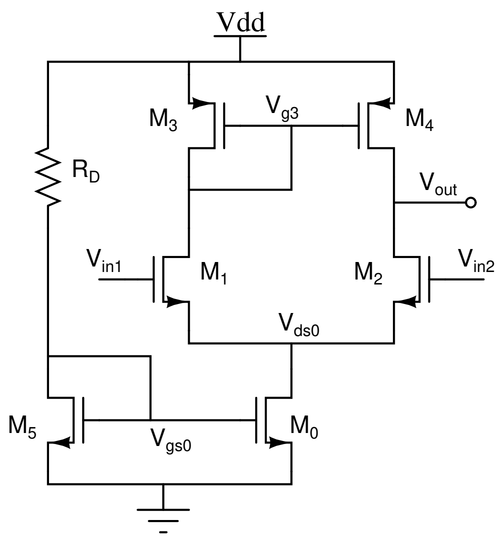

Figure 2: Five Transistor-OTA

i. Design this amplifier for $V_{out_{dc}} = 6V$, $V_{dd} = 10V$.
(Hint: Refer to the equations in the theory part for $V_{out_{dc}}$. From this calculate the tail current source (I_0). Then calculate the limits of V_{incm} and chose V_{incm} accordingly (Don't choose very near to the extreme values). Since I_0 is known, calculate R_D). **[3 Marks]**

ii. Apply $V_{in1} = V_{in2} = V_{incm}$ and run DC analysis. Tabulate all the node voltages, branch currents and operating region of MOSFETs. **[2 Marks]**

iii. Apply V_{in1} as sine wave of 5 mV_{pp}, 1 KHz and V_{in2} as sine wave of 5 mV_{pp}, 1 KHz and 180 deg phase shifted (w.r.t to V_{in1}). Offset/DC value of these two waveforms should be V_{incm}. Plot the V_{out} and $V_{in1} - V_{in2}$ and report the gain. Compare with the hand calculated gain. **[2 Marks]**

iv. Perform AC analysis. Determine the DC gain and compare it with the transient analysis gain.
- **[2 Marks]**

v. Measure the common mode gain of the OTA. You have to short V_{in1} and V_{in2} and apply V_{in} as sine wave of 100 mV_{pp}, 1 KHz and dc offset should be V_{incm} that you have calculated earlier. Plot the output waveform and mention the common mode gain of the OTA. **[2 Marks]**

3. **Some Application design around Five Transistor OTA**

(a) **Unity Gain Amplifier**

i. Design the unity gain buffer circuit as shown in the figure [3].

ii. Determine the transfer characteristics by performing DC sweep analysis. Sweep voltage input V_{in1} from 0 to 10 V in a step of 0.1V, $V_{dd} = 10V$. Plot V_{out} and V_{in1} with respect to V_{in1}.
- **[2 Marks]**

iii. Perform transient analysis. Apply V_{in1} as 100 mVpp, 1 KHz and V_{incm} (as calculated earlier) as DC offset. **[1 Marks]**

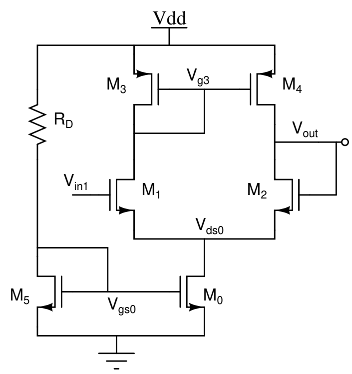

Figure 3: Unity amplifier

(b) **Inverting Amplifier**

i. The Inverting amplifier circuit designed using five-transistor OTA is shown in Figure [4]. Apply V_{bias} as V_{incm} at the gate of M_1 that you have calculated when you were designing five transistor OTA. Take Resistor value R_2 =10R_1=10MΩ, $V_{dd} = 10V$. What is the need to have resistance values in MΩ? **[1 Marks]**

ii. Apply $V_{bias} + vd$ at the one terminal of R_1, vd is the sinusoidal voltage input with 100 mVpp, 1KHz frequency. Plot V_{out} and $V_{bias} + vd$ and tabulate the theoretical and measured value of the amplifier gain and the phase shift. **[2 Marks]**

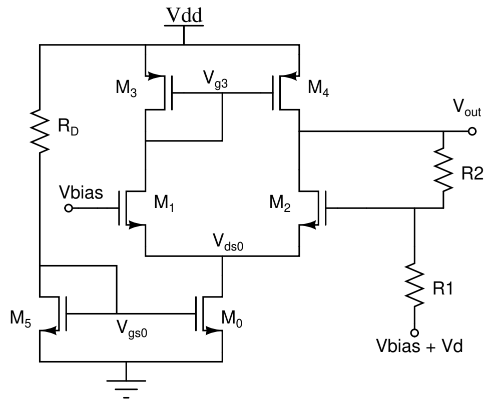

Figure 4: Inverting amplifier

(c) **Differentiator Circuit (BONUS)**

i. By observing unity gain and inverting amplifier now you have to connect the five transistor OTA as Differentiator in negative feedback configuration.You can refer the previous experiment of Opamp based Differentiator. Apply Vin as trinagular waveform of 100 mVpp, 1 KHz frequency and Plot input and output waveform. **[2 Marks]**