

Lab: 8

### Instructions:

- Write down all your observations in notebook.
- Verify your calculations with your respective TA.

### Objectives:

- To extract mosfet parameters.
- To design CS amplifier for given specifications.
- To understand the working and design of basic current mirror.
- Using Simulations to support analytical analysis.

#### 1. MOSFET Characterization

In this section, an [Excel File](#) is provided which contains experimental  $I_d$  values for corresponding  $V_{gs}$  values (0 to 5 V) for a constant  $V_{ds}$  of 5 V and  $V_{bs}$  of 0 V.

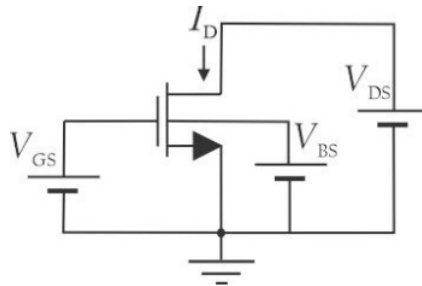


Figure 1: Testbench to extract Mosfet Parameters

The expression for  $I_d$  is given by

$$I_d = \frac{k_n}{2} (V_{gs} - V_{th})^2$$

where  $k_n$  is the transistor transconductance (in  $\mu A/V^2$ ) and  $V_{th}$  is the threshold voltage (in Volts). Using the data,

- Plot  $I_d$  v/s  $V_{gs}$  from the given data
- Extract  $K_n$  and  $V_{th}$  referring to the [Video](#) and tabulate them. [2 Marks]
- Include these parameters ( $k_n$  and  $V_{th}$ ) into the model file and then simulate (DC Sweep on  $V_{gs}$  from 0 to 5 V,  $V_{ds} = 5$  V,  $V_{bs} = 0$  V) the schematic in Ltspice as shown in Fig[1] and plot  $I_d$  v/s  $V_{gs}$ . [2 Marks]
- Extract the simulation data ( $I_d$  and  $V_{gs}$  values) from LtSpice and plot in Excel with the experimental data provided on the same plot. These plots should coincide with each other. [1 Mark]

In the subsequent sections, You will use these parameters to design a Common Source Amplifier and Current Mirror using Ltspice. Assume  $V_{th}$  and  $K_p$  to be 0.5 V and 200 (in  $\mu A/V^2$ ) respectively for PMOS.

## 2. Common Source (CS) Amplifier with Resistive Load

### (a) Theory

#### i. Introduction:

MOSFET-based Common Source (CS) Amplifier with resistive load is as shown in the figure [2].  $M_1$  is an NMOS with  $R_D$  resistor as load. Input,  $V_{in}$  is applied at the gate of  $M_1$ .  $V_{in}$  consists of DC bias voltage of  $V_{bias}$  and ac signal  $v_{in}$  (i.e.  $V_{in} = V_{bias} + v_{in}$ ).  $V_{bias}$  is responsible for biasing  $M_1$  in proper **operating region**. Output is observed at the drain of  $M_1$ . This circuit is called a common source amplifier with a resistive load.

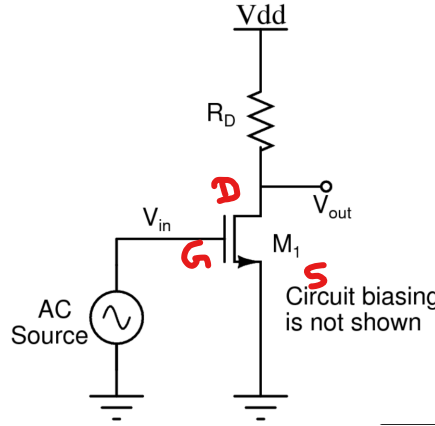


Figure 2: CS amplifier with Resistive Load

#### ii. Small signal gain ( $A_v$ ):

is  $g_m = kn?$

Fig[3] is a small signal model of CS amplifier with resistive load.  $v_{in}$  is small signal applied between gate and source where source is grounded. This  $v_{in}$  causes change in current flowing from drain to source. This change is given by  $g_m v_{in}$  where  **$g_m$  is transconductance of  $M_1$  mosfet**.  $g_m v_{in}$  flows from parallel combination of  $R_D$  and  $r_o$  (i.e.  $R_D || r_o$ ) generating voltage change at drain ( $v_{out}$ ) of  $-g_m(R_D || r_o)v_{in}$ . Thus, change of  $v_{in}$  voltage at gate causes  $-g_m(R_D || r_o)v_{in}$  change in drain voltage. Gain ( $A_v$ ) of CS amplifier is defined as  $v_{out}/v_{in}$ . Thus,  **$A_v = -g_m(R_D || r_o)$** . For simplicity  $r_o$  is assumed infinite (Practically it is a high value). Thus small signal gain is simplified to  $A_v = -g_m R_D$ .

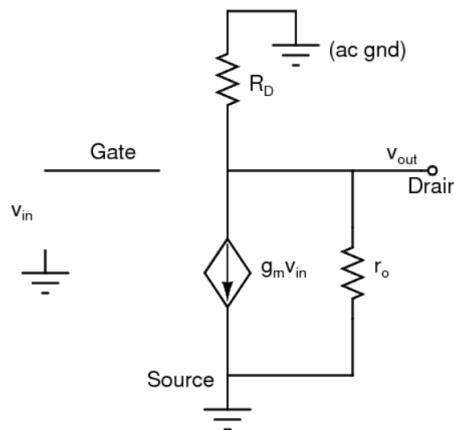


Figure 3: Small signal model of CS amplifier with resistive load

#### iii. Biasing $M_1$ in saturation region

$M_1$  should be biased in saturation region for amplifier to work. For this,  **$V_{ds1} > V_{gs1} - V_{th1}$** . As a safety margin let us consider  $V_{ds1}$  is  $V_m$  voltage higher than  $V_{gs1} - V_{th1}$ . In our case  $V_{ds1} = V_{out}$  and  $V_{gs1} = V_{in} - V_{th}$ . Let  $I_D$  be the current flowing through  $M_1$ . Thus,  $V_{out}$  can be expressed as  $V_{dd} - I_D R_D$ . Thus the constraint to keep  $M_1$  in saturation is  **$V_{dd} - I_D R_D = V_{in} - V_{th} + V_m$** .  $I_D$  in saturation region is given as  $\frac{K_n}{2}(V_{in} - V_{th})^2$  and transconductance,  **$g_m = K_n(V_{in} - V_{th})$** . Thus

?  $I_D R_D$  can be expressed as  $\frac{A_v(V_{in} - V_{th})}{2}$ . Substituting this in above inequality and rearranging terms to get  $V_{in}$  we get  $V_{in} = \frac{V_{dd} - V_m}{1 + \frac{A_v}{2}} + V_{th}$ . This  $V_{in}$  is the DC bias voltage ( $V_{bias}$ ).

(b) **Simulation**

Design a CS amplifier with resistive load for a small signal gain  $A_v > 18$  dB.

- Perform hand calculations to meet gain specifications. Use the extracted parameter values for  $K_n$  and  $V_{th}$  and tabulate DC bias Voltage ( $V_{bias}$ ), Drain resistance ( $R_D$ ) and DC output voltage ( $V_{out_{dc}}$ ). [3 Marks]
- Draw Schematic in LtSpice and use the same model file (containing parameters you extracted from the data provided). Select the standard value of  $R_D$ , available in the lab, as shown in Fig.[ 8] and is close to the value calculated previously. Run Transient Simulation by applying  $V_{in}$  of 10 mV<sub>pp</sub>, 1 KHz sinusoidal signal with DC voltage offset of  $V_{bias}$  and  $V_{dd} = 5V$ . Plot  $V_{out}$  and  $V_{in}$ . [1 Mark]
- Determine the gain  $A_v$ . If gain specification is not meet then make appropriate changes in the circuit parameters to meet the specs. Tabulate the final values of all parameters. [1 Mark]
- Tabulate the DC Operating point( $V_{gs}, V_{ds}, I_d$  and  $g_m$ ) and region of operation of transistor. [2 Marks]

### 3. Common Source (CS) Amplifier with Diode Connected Load

(a) **Theory**

i. **Introduction**

MOSFET-based Common Source (CS) Amplifier with diode connected load is as shown in the figure [ 4].  $M_1$  is a NMOS with  $M_2$  as a diode load. Input,  $V_{in}$  is applied at the gate of  $M_1$ .  $V_{in}$  consists of dc bias voltage of  $V_{bias}$  and ac signal  $v_{in}$  ( $V_{in} = V_{bias} + v_{in}$ ).  $V_{bias}$  is responsible for biasing  $M_1$  in proper operating region. Output is observed at the drain of  $M_1$ . Thus this circuit is called as a common source amplifier with diode connected load.

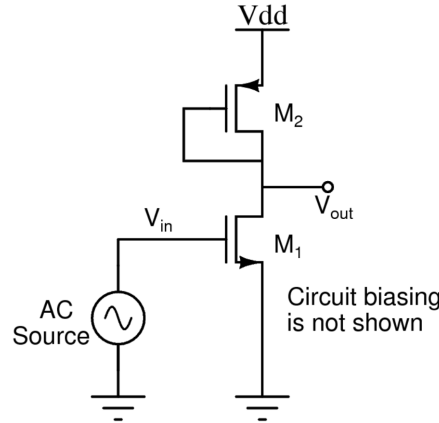


Figure 4: CS amplifier with diode connected load

ii. **Small signal gain ( $A_v$ )**

Small signal model of CS amplifier with diode connected load is shown in Fig.[ 5]. For simplicity let us consider  $r_{o1}$  and  $r_{o2}$  be infinite (In practical cases both these resistances are very high but not infinite). Thus there is no current flowing through these resistances. Writing KCL at node  $v_{out}$  we get  $g_{m2}v_{sg2} = g_{m1}v_{gs1}$ . Where  $v_{gs1} = v_{in}$  and  $v_{sg2} = -v_{out}$ .  $g_{m1}$  can be expressed as  $\sqrt{2I_{d1}K_{n1}}$  similarly  $g_{m2}$  can be expressed as  $\sqrt{2I_{d2}K_{p2}}$ . Thus  $A_v = \frac{v_{out}}{v_{in}} = \frac{-g_{m1}}{g_{m2}} = -\sqrt{\frac{K_{n1}}{K_{p1}}}$

iii. **Biasing  $M_1$ ,  $M_2$  in saturation region**

Drain and Gate of  $M_2$  are connected to each other. Thus  $M_2$  if on then will always be biased in saturation region.(prove why?).  $M_1$  will remain in saturation as long as  $V_{out} > V_{in} - V_{th1}$ . Thus,  $V_{out} = V_{in} - V_{th1} + V_m$ . Current from  $M_2$  and  $M_1$  are same. Thus,  $K_{n1}(V_{in} - V_{th1})^2 = K_{p2}(V_{dd} - V_{out} - V_{th2})^2$ . Input voltage can be expressed as  $V_{in} = \sqrt{\frac{K_{p2}}{K_{n1}}}(V_{dd} - V_{out} - V_{th2}) + V_{th1}$ . Let  $V_m$  be the margin voltage by which  $V_{out}$  is greater than  $V_{in} - V_{th1}$ . Substituting this in  $V_{in}$  equation we can solve for  $V_{in}$ . This value will be the bias voltage ( $V_{bias}$ ) of  $M_1$ .

(b) **Simulation**

Design a CS amplifier with diode load

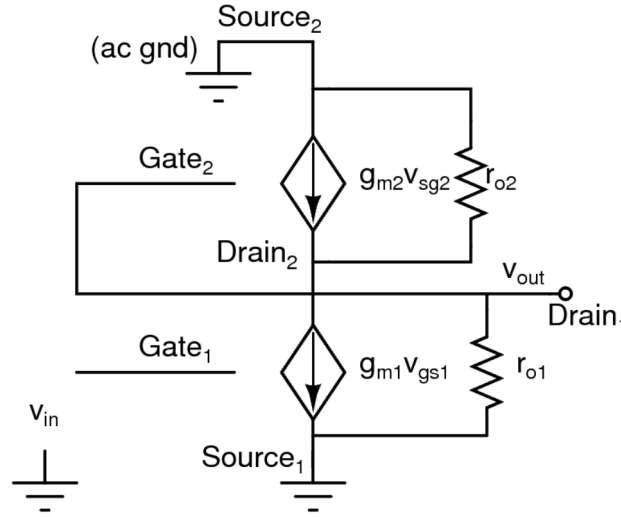


Figure 5: Small signal model of CS amplifier with diode connected load

- i. Perform hand calculations. Use the extracted parameter values for  $K_n$  and  $V_{th}$  (assume  $K_p$  and  $V_{th}$  for PMOS as given in question 1). Tabulate DC bias Voltage ( $V_{bias}$ ), DC output voltage ( $V_{out_{dc}}$ ) and small signal gain ( $A_v$ ). [3 Marks]
- ii. Draw Schematic in LtSpice. Use the same model file as earlier.  
Run transient simulation by applying  $V_{in}$  of 10 mV<sub>pp</sub>, 1 KHz sinusoidal signal with DC voltage offset of  $V_{bias}$  and  $V_{dd} = 5V$ . Plot  $V_{out}$  and  $V_{in}$ . [1 Marks]
- iii. Determine the gain  $A_v$ . Compare with the hand-calculated gain value. [1 Marks]
- iv. Tabulate the DC Operating point and region of operation for both the transistors. [4 Marks]

#### 4. Current Mirror (CM) Design

##### (a) Introduction

Current mirror is an analog circuit which senses the reference current and mirrors it to the load. It is widely used in modern ICs. Most common applications are amplifiers, D/A converters, Delay elements, Bias circuits etc.

##### (b) Basic Design Concepts

Basic idea is to generate a reference voltage ( $V_{GS1}$ ) by pushing current ( $I_{REF}$ ) into the diode connected MOSFET ( $M_1$ ) as shown in Fig.[ 6] and use this voltage to bias another MOSFET ( $M_2$ ) such that the another MOSFET acts as a current source providing same current ( $I_{copy}$ ) as reference current ( $I_{REF}$ ). Let's derive the equation for  $I_{COPY}$  in terms of  $I_{REF}$  and device parameters.

The current equation of a MOSFET, ignoring channel length modulation and biased in saturation region is

$$I_{DS} = \frac{1}{2} \mu C_{OX} \frac{W}{L} (V_{GS} - V_{TH})^2 \quad (1)$$

Above equation can be rearranged to get

$$V_{GS} = \sqrt{\frac{2I_{ds}}{\mu C_{OX} \frac{W}{L}}} + V_{TH} \quad (2)$$

Referring to Fig.[ ??] and Eqn.[ 2] we can write  $V_{GS1}$  as

$$V_{GS1} - V_{TH1} = \sqrt{\frac{2I_{REF}}{\mu C_{OX} \frac{W_1}{L_1}}} \quad (3)$$

Since  $V_{GS1} = V_{GS2}$  and assuming  $V_{TH1} = V_{TH2}$  we can write  $I_{COPY}$  as

$$I_{COPY} = \frac{1}{2} \mu C_{OX} \frac{W_2}{L_2} (V_{GS1} - V_{TH1})^2 \quad (4)$$

$$I_{COPY} = \frac{W_2}{L_2} \frac{I_{REF}}{\frac{W_1}{L_1}} \quad (5)$$

generally written as

$$\frac{I_{COPY}}{\frac{W_2}{L_2}} = \frac{I_{REF}}{\frac{W_1}{L_1}} \quad (6)$$

In many applications we may require to copy more current from reference. This is simply achieved by connecting current source MOSFETs in parallel and with appropriate sizing.

Note that all the above equations are derived by ignoring channel length modulation effect thus if this effect is considered there may be error in copying current, usually length of devices are chosen high to minimize the error and  $V_{DS1}$ ,  $V_{DS2}$  are made equal. Both the MOSFETs (M1 and M2) are in saturation region. Since, M1 is in diode connected it will always be in saturation region given enough overdrive is provided but there is a possibility of M2 going in triode region due to inadequate drain to source voltage across it. Thus, if M2 is biased in triode then current mirroring will not happen. The derived equation is valid for older technology models where MOSFET obeys the square law behaviour. In small scale devices this is not true but however it will still be able to mirror the current but will follow different equation as opposed to Eqn.[ 6]

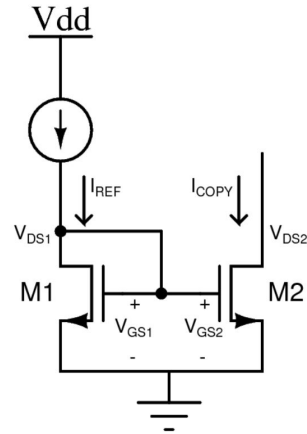


Figure 6: Basic NMOS current mirror circuit

(c) **Simulation**

Fig.[ 6] is an equivalent model of Fig. 7 simplified for simulation purposes.

- Perform hand calculations to calculate value of  $R_1$  such that  $I_{REF} = 2$  mA. What is the value of  $V_{GS1}$ ? Use  $V_{DD} = 8$  V. [2 Marks]
- Draw LtSpice Schematic for Fig.[ 7] circuit. Set the value of  $R_1$  and perform DC simulation to find  $I_{REF}$ . Tweak value of  $R_1$  (if required) until  $I_{REF}$  is 2 mA. [1 Marks]
- Sweep  $V_{DS2}$  from 0 V to 8 V. Plot  $I_{COPY}$  vs  $V_{DS2}$ . Determine value of  $V_{DS2}$  at which  $I_{COPY} = I_{REF}$ . What is the relationship between this  $V_{DS2}$  and  $V_{DS1}$ . [3 Marks]

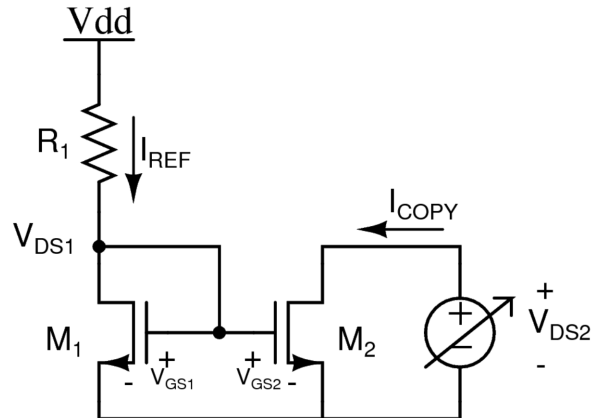


Figure 7: NMOS current mirror circuit setup for simulation

| Value        | Value       | Value        | Value          | Value         | Value          | Value          |
|--------------|-------------|--------------|----------------|---------------|----------------|----------------|
| 1 $\Omega$   | 10 $\Omega$ | 100 $\Omega$ | 1 k $\Omega$   | 10 k $\Omega$ | 100 k $\Omega$ | 1 M $\Omega$   |
| 1.2 $\Omega$ | 12 $\Omega$ | 120 $\Omega$ | 1.2 k $\Omega$ | 12 k $\Omega$ | 120 k $\Omega$ | 1.2 M $\Omega$ |
| 1.5 $\Omega$ | 15 $\Omega$ | 150 $\Omega$ | 1.5 k $\Omega$ | 15 k $\Omega$ | 150 k $\Omega$ | 1.5 M $\Omega$ |
| 1.8 $\Omega$ | 18 $\Omega$ | 180 $\Omega$ | 1.8 k $\Omega$ | 18 k $\Omega$ | 180 k $\Omega$ | 1.8 M $\Omega$ |
| 2.2 $\Omega$ | 22 $\Omega$ | 220 $\Omega$ | 2.2 k $\Omega$ | 22 k $\Omega$ | 220 k $\Omega$ | 2.2 M $\Omega$ |
| 2.7 $\Omega$ | 27 $\Omega$ | 270 $\Omega$ | 2.7 k $\Omega$ | 27 k $\Omega$ | 270 k $\Omega$ | 2.7 M $\Omega$ |
| 3.3 $\Omega$ | 33 $\Omega$ | 330 $\Omega$ | 3.3 k $\Omega$ | 33 k $\Omega$ | 330 k $\Omega$ | 3.3 M $\Omega$ |
| 3.9 $\Omega$ | 39 $\Omega$ | 390 $\Omega$ | 3.9 k $\Omega$ | 39 k $\Omega$ | 390 k $\Omega$ | 3.9 M $\Omega$ |
| 4.7 $\Omega$ | 47 $\Omega$ | 470 $\Omega$ | 4.7 k $\Omega$ | 47 k $\Omega$ | 470 k $\Omega$ | 4.7 M $\Omega$ |
| 5.6 $\Omega$ | 56 $\Omega$ | 560 $\Omega$ | 5.6 k $\Omega$ | 56 k $\Omega$ | 560 k $\Omega$ | 5.6 M $\Omega$ |
| 6.8 $\Omega$ | 68 $\Omega$ | 680 $\Omega$ | 6.8 k $\Omega$ | 68 k $\Omega$ | 680 k $\Omega$ | 6.8 M $\Omega$ |
| 8.2 $\Omega$ | 82 $\Omega$ | 820 $\Omega$ | 8.2 k $\Omega$ | 82 k $\Omega$ | 820 k $\Omega$ | 8.2 M $\Omega$ |

Figure 8: Standard Resistors values with a tolerance of  $\pm 10\%$