Indian Institute of Technology Bombay

Analog Circuits Lab
EE 230

Lab 4
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Mridul Choudhary
23B3933

Contents

1 Log and Anti-Log Amplifier

1.1 Aim of the experiment

1. **Understand and Implement Log and Anti-Log Amplifiers:** Design and analyze circuits that compute the logarithm and antilogarithm of an input signal.
2. **Develop a Square Root Amplifier:** Use logarithm and antilogarithm principles to construct a circuit that outputs the square root of the input voltage.
3. **Analyze the Behavior of Diodes in Logarithmic and Antilogarithmic Circuits:** Study the diode's voltage-current characteristics and its role in logarithmic computations.
4. **Simulate the Square Root Amplifier Circuit:** Validate circuit performance through SPICE simulations, comparing theoretical and simulated results.

1.2 Design of the Circuit

The experiment uses op-amps and diodes to implement logarithmic, anti-logarithmic, and square root functions.

1. **Logarithmic Amplifier Design**
   - Uses a diode and an op-amp in an inverting amplifier configuration.
   - Key Equation:
   $$I_D = I_s(e^{\frac{V_D}{nV_T}} - 1) \tag{1}$$
   - If $V_D >> nV_T$, approximation holds :
   $$I_D = I_S e^{\frac{V_D}{nV_T}} \tag{2}$$
   - Applying to the circuit:
   $$I_D = \frac{V_{in}}{R} \tag{3}$$
   - Resulting in:
   $$V_{out1} = -nV_T ln(V_{in}) + a_2 \tag{4}$$
   - This circuit transforms input voltage into a logarithmic signal.
2. **Offset Removal Block**
   - A subtraction circuit removes the offset term a_2.
   - After subtraction:
   $$V_{out2} = a_1 ln(V_{in}) \tag{5}$$
3. **Scaling Block**
   - The log output is scaled by 1/2 using an amplifier with gain $\beta = \frac{1}{2}$

- Output:

$$V_{out3} = \frac{-a_1}{2} ln(V_{in}) \tag{6}$$

4. **Antilogarithmic Amplifier**

- Uses a second diode to exponentiate the scaled output.
- Applying the exponential equation:

$$V_{out} = R_3 I_s e^{\frac{V_{b2}}{n_2 V_T}} V_{in}^{\frac{1}{2}} + V_{b2} \tag{7}$$

- Final square-root result:

$$V_{out} = b_1 V_{in}^{\frac{1}{2}} \tag{8}$$

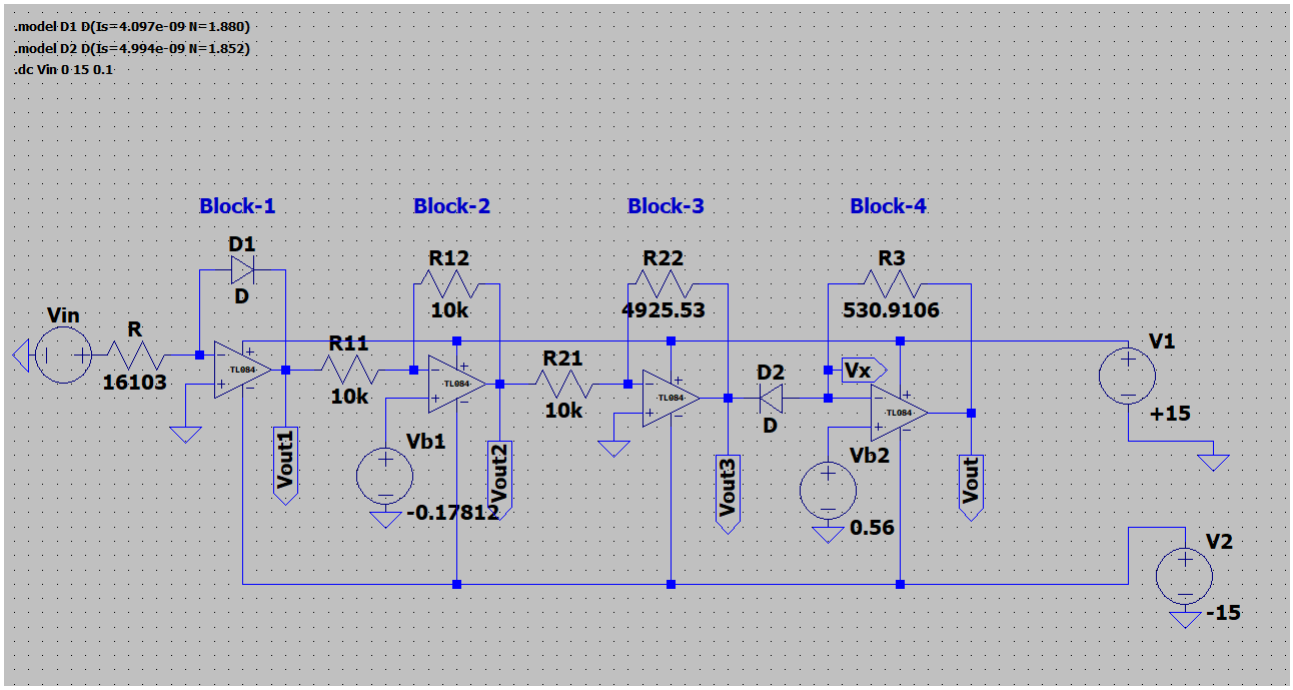

Figure 1: Log Anti-Log Circuit Diagram

1.3 Experimental Results

Sr. No.	Parameter	Value
1	n_1	1.880
2	n_2	1.852
3	I_{s1}	$4.097e^{-09}$ A
4	I_{s2}	$4.994e^{-09}$ A
5	(V_{d1}, I_{d1}) (D1)	(0.5 V, $1.192e^{-04}$ A)

6	(V_{d2}, I_{d2}) (D1)	(0.6 V, $9.315e^{-04}$ A)
7	(V_{d1}, I_{d1}) (D2)	(0.5 V, $1.698e^{-04}$ A)
8	(V_{d2}, I_{d2}) (D2)	(0.6 V, $1.368e^{-03}$ A)
9	R	16103 Ω
10	a_1	0.048645
11	a_2	-0.35625967791100094
12	R_1	10 kΩ
13	V_{b1}	-0.178129838 V
14	β	0.492553
15	R_{21}	10 kΩ
16	R_{22}	4925.53 Ω
17	V_{b2}	0.56 V
18	R_3	530.9106 Ω

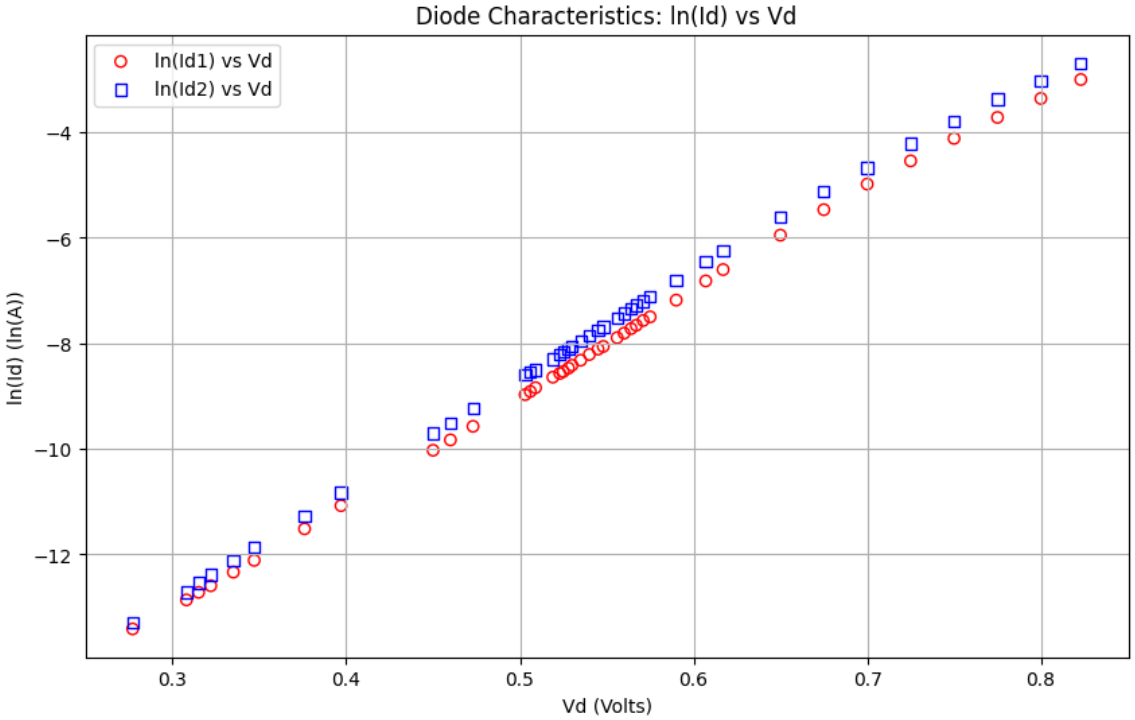

Figure 2: V_D v/s I_D of D1 and D2

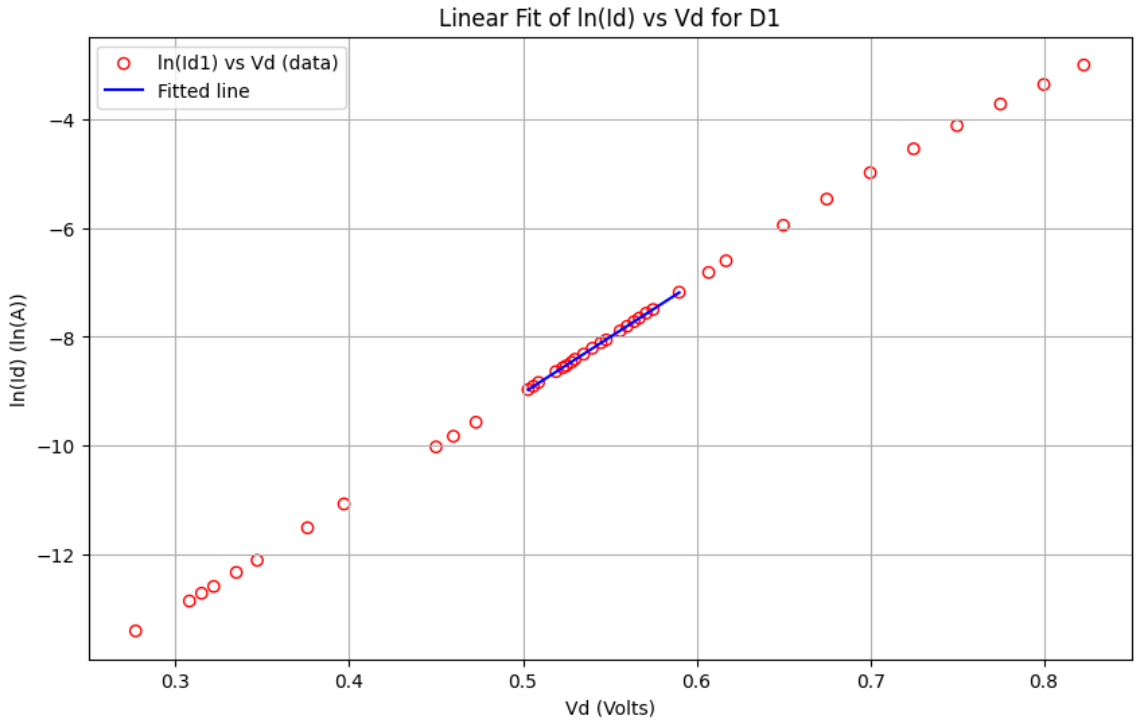

Figure 3: Fitted line on V_D v/s I_D of D1

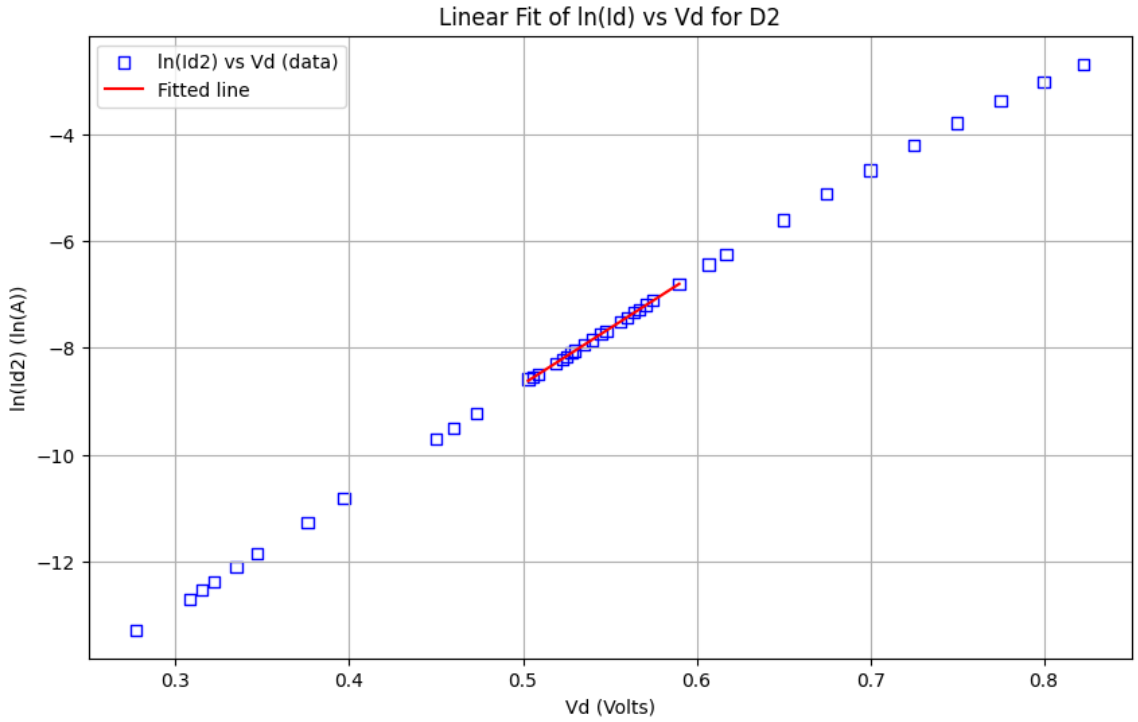

Figure 4: Fitted line on V_D v/s I_D of D2

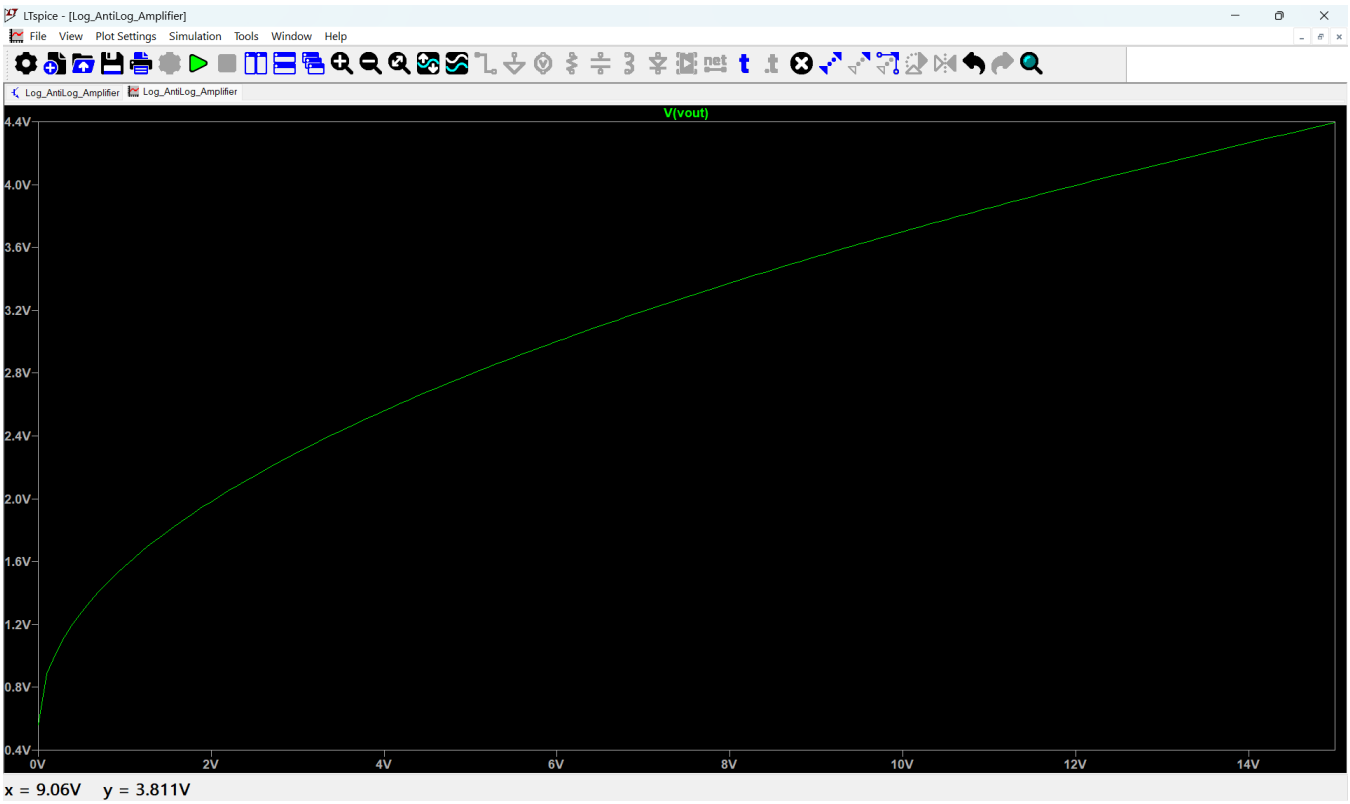

Figure 5: V_{out} of the Log Anti-Log Amplifier

1.4 Conclusion and Inference

1. **How to select the diode for log amplification?**
   - Choose a diode with a linear $ln(I_D)$ vs V_D relationship over a suitable current range.
   - Avoid diodes with multiple linear regions (e.g., D4 in the graph in handout).
2. **How to select the input voltage range?**
   - Determine the range where $ln(I_D)$ vs V_D is linear.
   - Use $V_{in1} = I_{D1}/R$ and $V_{in2} = I_{D2}/R$.
3. **How to extract diode model parameters?**
   - The saturation current I_S is obtained from the y-intercept of the $ln(I_D)$ vs V_D plot.
   - The ideality factor n is extracted from the slope.
4. **Which op-amp to choose?**
   - Choose a low-bias current op-amp like TL084, since high bias currents can distort low-current diode operation.
5. **Simulation Steps:**

- Plot $ln(I_D)$ vs V_D for provided diodes.
- Identify the linear range and determine I_S and n.
- Implement the SPICE model for these diodes.
- Verify circuit behavior with expected $ln(V_{out})$ vs $ln(V_{in})$.

1.5 Experiment Completion Status

The complete experiment was performed in front of the TA in the lab itself.