EE230: Analog Circuits Lab
Lab No.10b

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Contents

1 Differential Amplifier with Resistive Load

1.1 Aim of the Experiment

To design and realize a differential amplifier with a resistive load, using MOSFETs with hardware, ensuring all MOSFETs operate in the saturation region and analyzing its differential behavior under AC excitation.

1.2 Theory

1.2.1 Introduction

A differential amplifier is a fundamental building block in analog circuits, used for amplifying the difference between two input signals while rejecting common-mode noise. The amplifier designed here uses NMOS transistors in a symmetric differential configuration with a current mirror biasing. The circuit comprises:

- M1, M2: NMOS differential input pair
- R2, R3: Resistive loads for the differential pair
- M3: Acts as tail current source
- R1, M3, and M4: Current mirror

The circuit is powered by a supply voltage of $V_{DD} = 10V$.

The circuit is designed to ensure:

- Minimum input common-mode voltage ($V_{in,cm(min)}$) ensures all transistors are in saturation.
- Differential gain (A_v) is determined using:
- Output common-mode voltage $5V < V_{out,cm} < 7V$
- Current reference resistor R_1 calculated using:

1.3 Design Parameters

- $V_{DD} = 10, V$
- $V_{in,cm} = 4.5, V$
- $V_{out,cm}$ in the range $5, V$ to $7, V$
- Gain $A_v > 12, dB$
- Assume $K_{n1} = 200, \mu A/V^2$, $K_{n3} = 100, \mu A/V^2$, $V_{th1} = V_{th3} = 0.7, V$

1.4 Circuit Diagram (LT Spice):

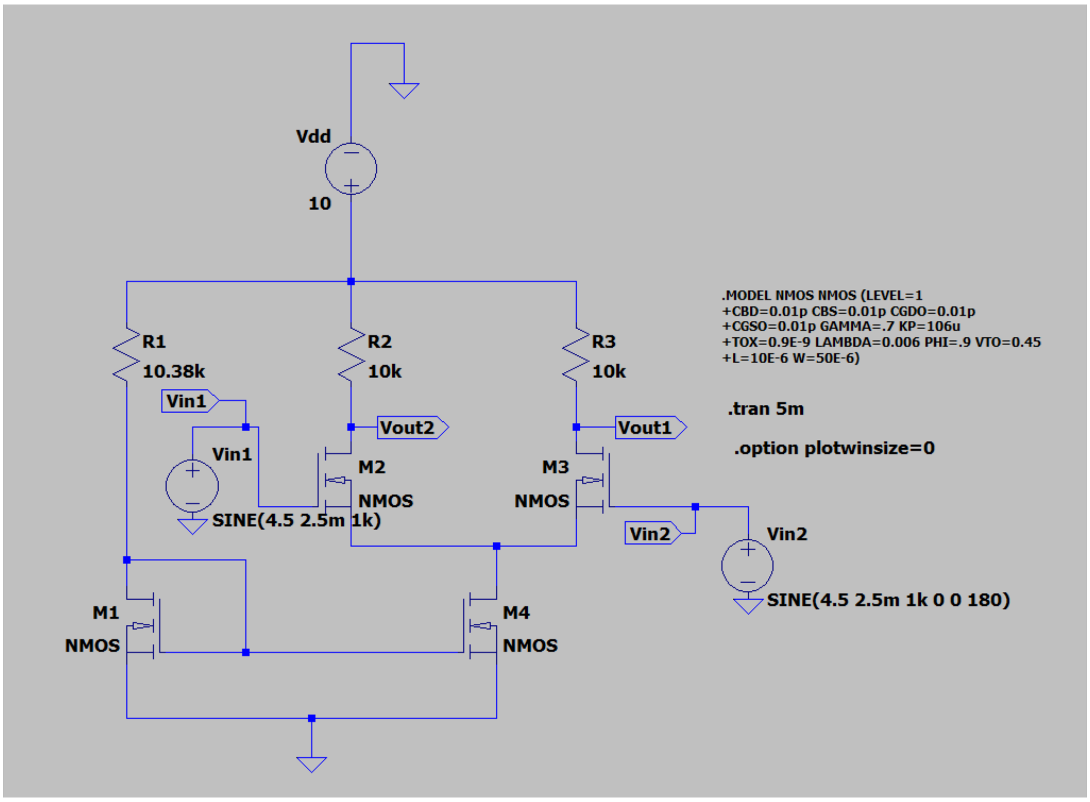


Figure 1: Differential Amplifier with Resistive Load

1.5 Calculation Steps

1.5.1 Minimum Input Common-Mode Voltage

The minimum input common-mode voltage is determined by ensuring all MOSFETs operate in the saturation region:

$$V_{in,cm(min)} = V_{GS1} + V_{d_{sat3}} \tag{1}$$

Expanding using device parameters:

$$V_{in,cm(min)} = V_{TH1} + \sqrt{\frac{I_{tail}}{K_{n1}}} + \sqrt{\frac{2I_{tail}}{K_{n3}}} \tag{2}$$

Solving for I_{tail} to satisfy $V_{in,cm(min)} = 3.5V$.

$$3.5 = 4.5 + \sqrt{\frac{I_{tail}}{(0.53) * 10^{-3}}} + \sqrt{\frac{2I_{tail}}{(0.53) * 10^{-3}}}$$
$$I_{tail} = 0.84591mA$$

1.5.2 Gain Calculation

The voltage gain of the differential amplifier is:

$$A_v = g_{m1}R_2 \tag{3}$$

where g_{m1} is the transconductance of M1:

$$g_{m1} = \sqrt{2 * K_{n1} * I_{tail}} \tag{4}$$

Solving for R_2 to meet $A_v > 12dB$.

let $R_2 = 10$ kΩ,

$$A_V = \sqrt{2 * I_{tail} * K_{n1}} * R_2$$

$$(A_V)_{in-dB} = 20 * log(\sqrt{2 * I_{tail} * K_{n1}} * R_2)$$

$$(A_V)_{in-dB} = 20 * log(\sqrt{2 * 0.84591 * 10^{-3} * (0.53) * 10^{-3}} * (10) * 10^3)$$

$$(A_V)_{in-dB} = 19.5263$$

1.5.3 Output Common-Mode Voltage

The output common-mode voltage is given by:

$$V_{out,cm} = V_{DD} - \frac{I_{tail}}{2} R_2 \tag{5}$$

$$V_{out,cm} = 10 - \frac{0.84591 * 10^{-3}}{2} * 10^4$$

$$V_{out,cm} = 5.77045V$$

1.5.4 Current Mirror Reference Current

The reference current I_{ref} is set by resistor R_1:

$$I_{ref} = \frac{K_n}{2} * (V_{gs} - V_{th})^2 \tag{6}$$

$$0.84591 * 10^{-3} = \frac{(0.53) * 10^{-3}}{2} * (V_{gs} - 0.45)^2$$

$$0.58091 * 10^{-3} = (V_{gs} - 0.45)^2$$

for M_4,

$$V_{gs} = 1.2121V$$

$$R_1 = \frac{V_{DD} - V_{gs}}{I_{ref}}$$

$$R_1 = \frac{10 - 1.2121}{0.84591 * 10^{-3}}$$

$$R_1 = 10388.6938\Omega$$

1.6 Experimental Procedure

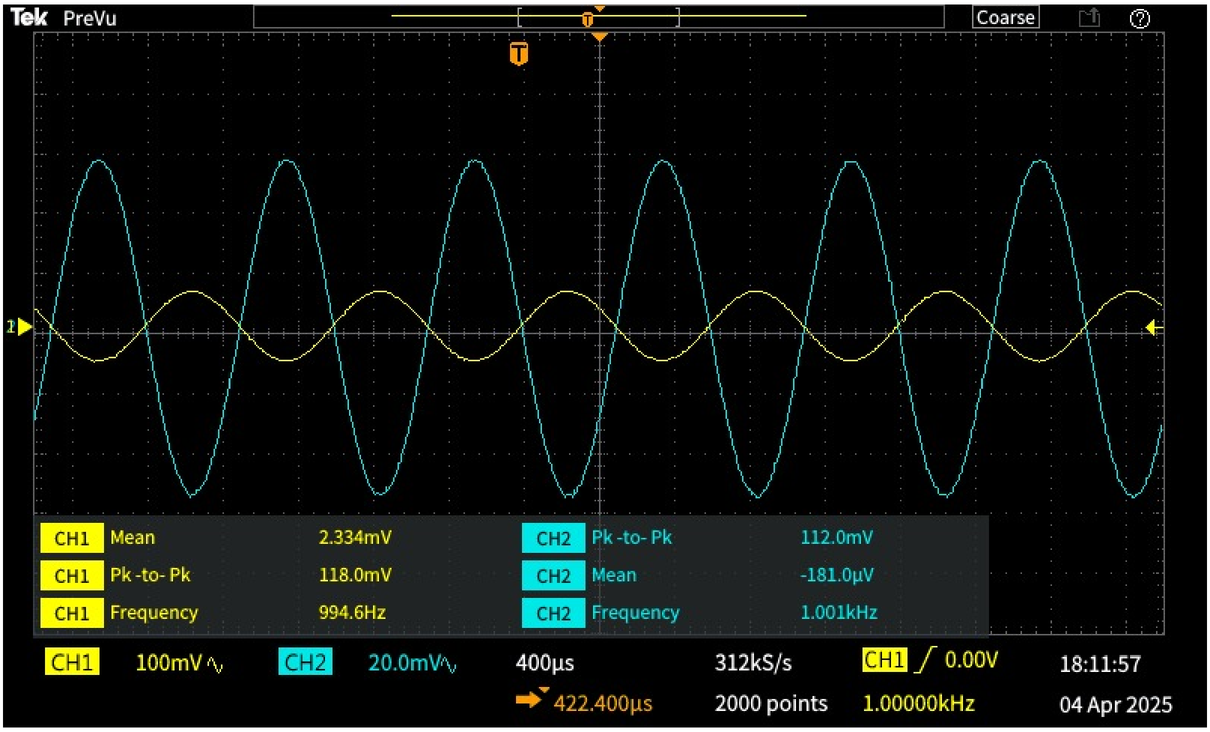
1. Build the circuit with the chosen parameters: $R_2 = R_3 = 10, k\Omega$, $R_1 = 124, k\Omega$.
2. Use dual-channel AFG:
   - Apply $Vin_1 = 4.5, V + 20, mV_{pp}$ sine wave
   - Apply $Vin_2 = 4.5, V - 20, mV_{pp}$ sine wave (180° phase shift)
3. Measure DC voltages at all nodes and branch currents using multimeter and oscilloscope.
4. Ensure each MOSFET satisfies $V_{DS} > V_{GS} - V_{TH}$.
5. Plot V_{out1} and V_{out2} on oscilloscope.

1.7 Experimental Results

Node Voltages, Branch Current and Gain

Section	Parameter	Value
ii	V_{out1}	6.22 V
ii	V_{out2}	6.22 V
ii	A_1	0.757 mA
ii	A_2	0.381 mA
ii	A_3	0.378 mA
iii	V_{out1}	118 mV
iii	V_{out2}	112 mV
iii	Gain	6

Plot from the DSO



1.8 Key Observations

- Balanced differential output is achieved.
- Minor mismatch in V_{out1} and V_{out2} can result from component mismatches.
- All transistors confirmed to be in saturation region.

1.9 Conclusion and Inference

The differential amplifier was successfully designed and implemented in hardware with proper biasing and gain. The phase relationship and differential amplification were verified. The design met the gain and output common mode specifications. This experiment emphasizes the importance of bias current selection and resistor sizing in analog amplifier design. It reinforces the role of transistor operating regions in determining amplifier behavior.

1.10 Experiment Completion Status

I have successfully completed all the sections mentioned in this Experiment

2 Differential Amplifier with Active Load (5T-OTA)

2.1 Aim of the Experiment

To design and implement a differential amplifier with current mirror active load (Five-Transistor OTA), calculate the theoretical values for various parameters, and verify the design through hardware implementation ensuring all MOSFETs operate in the saturation region.

2.2 Theory

A differential amplifier with a current mirror load, also known as a **Five Transistor OTA (5T-OTA)**, is widely used in designing operational amplifiers (Op-Amps). The circuit consists of:

- M_1 and M_2 forming the NMOS differential pair.
- M_3 and M_4 acting as a current mirror load.
- M_0 as the tail current source.
- M_5 mirroring the current to M_0.

The tail current (I_0) is determined by the value of R_D.

2.2.1 Circuit Diagram (LT Spice):

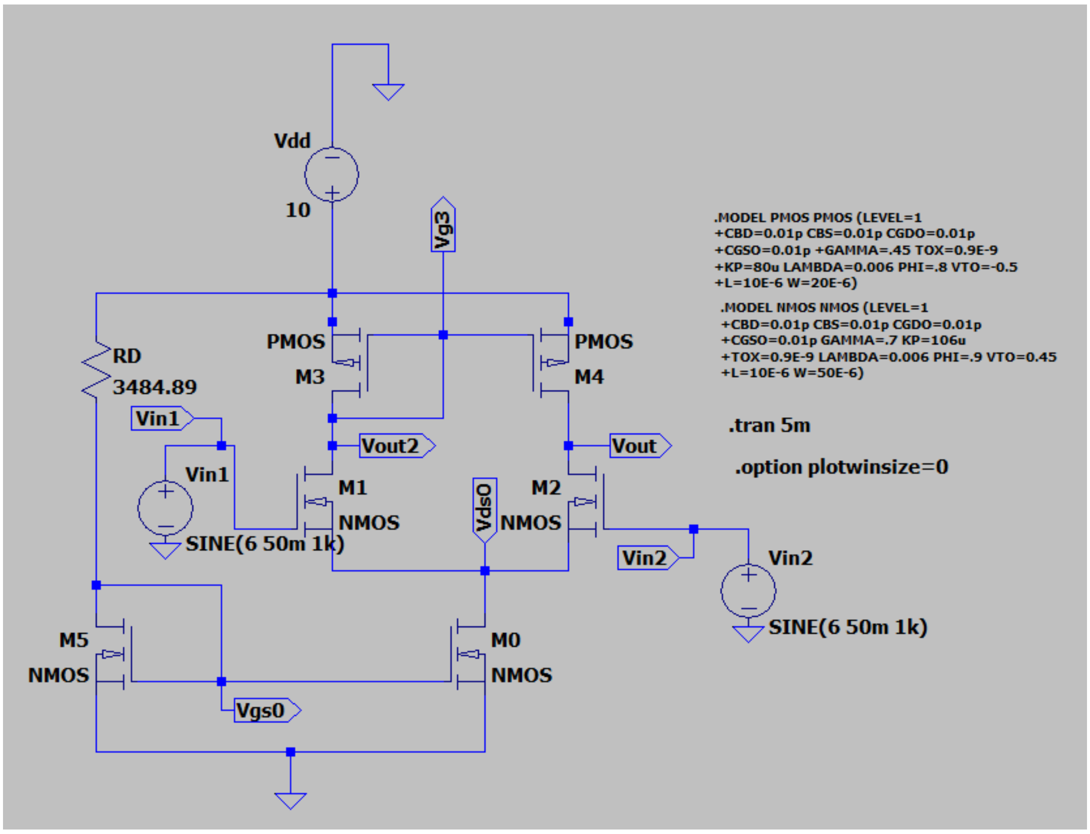


Figure 2: Differential Amplifier with Active Load

2.3 Calculation Steps

2.3.1 Calculation of current I_o

We know that,

$$V_{out,dc} = V_{DD} - \sqrt{\frac{I_o}{K_{n3}}} - V_{th3}$$

$$6 = 10 - \sqrt{\frac{I_o}{0.16 * 10^{-3}}} - 0.5$$

$$I_o = 1.96mA$$

2.3.2 Input Common Mode Voltage (V_{incm})

To ensure all transistors operate in the **saturation region**, the input common mode voltage must satisfy:

$$V_{incm(min)} = \sqrt{\frac{2I_0}{K_{no}}} + \sqrt{\frac{I_0}{K_{n1}}} + V_{th1} \tag{7}$$

$$V_{incm(max)} = V_{outdc} + V_{th1} \tag{8}$$

Thus, V_{incm} should be chosen within these limits.

$$V_{in,cm(min)} = \sqrt{\frac{2 * I_o}{K_{no}}} + \sqrt{\frac{I_o}{K_{n1}}} + V_{th1}$$

$$V_{in,cm(min)} = \sqrt{\frac{2 * 1.96 * (10^{-3})}{0.53 * (10^{-3})}} + \sqrt{\frac{1.96 * (10^{-3})}{0.53 * (10^{-3})}} + 0.45$$

$$V_{in.cm(min)} = 5.0569808291249V$$

$$V_{in.cm(max)} = V_{out,dc} + V_{th1}$$

$$V_{in.cm(max)} = 6 + 0.45$$

$$V_{in.cm(max)} = 6.45V$$

Assuming $V_{in,cm} = 6$V

2.3.3 Output Common Mode Voltage ($V_{out,cm}$)

Due to negative feedback, the equilibrium condition ensures:

$$V_{outdc} = V_{DD} - \frac{I_{tail} * R_2}{2} \tag{9}$$

$$6 = 10 - \frac{1.96 * (10^{-3}) * R_2}{2}$$

$$\frac{1.96 * (10^{-3}) * R_2}{2} = 4$$

$$R_2 = 4081.632653\Omega$$

2.3.4 Calculation of resistance R_D

$$V_{DD} - V_{gso} = I_o * R_D \tag{10}$$

$$I_o = \frac{K_{no}}{2} * (V_{gso} - V_{th0})^2 \tag{11}$$

$$V_{gso} = \sqrt{\frac{2 * 1.96 * (10^{-3})}{0.53 * (10^{-3})}} + 0.45$$

$$V_{gso} = 4.7324785628779 - 1.563$$

$$V_{gso} = 3.1696004146003V$$

substitute back V_{gso} back in equation(10),

$$10 - 3.1696004146003 = I_o * R_D$$

$$R_D = \frac{6.830399585399}{1.96 * (10^{-3})}$$

$$R_D = 3484.8977476528\Omega$$

2.3.5 Gain A_V

The voltage gain of the **5T-OTA** is given by:

$$A_V = -g_{m1}(r_{o2} \parallel r_{o4}) \tag{12}$$

where r_o is defined as:

$$r_o = \frac{1}{\lambda I_D} \tag{13}$$

This gain is highly dependent on the **channel length modulation coefficient (λ)**, which can be obtained from the MOSFET model file.
Using:

- $V_{sg3} = \frac{I_0}{K_{n3}} + V_{th3}$.
- I_0 is the tail current source.

Calculation of V_{gs1}:

$$V_{gs1} = V_{in1} - (V_{ds})_{sat0}$$

$$V_{gs1} = 6 - (V_{gs0} - V_{th0})$$

$$V_{gs1} = 6 - (3.1696004146003 - 0.45)$$

$$V_{gs1} = 3.2803995853997V$$

Calculation of g_{m1}:

$$g_{m1} = \sqrt{2 * I_{d1} * K_{n1}}$$

$$g_{m1} = k_{n1} * (V_{gs1} - V_{th1})$$

$$g_{m1} = 0.53 * 10^{-3} * (3.2803995853997 - 0.45)$$

$$g_{m1} = 1.5 * 10^{-3}$$

Calculation of I_{d2}:

$$I_{d2} = \frac{K_{n2}}{2} * (V_{gs2} - V_{th2})^2$$

$$I_{d2} = \frac{0.53 * 10^{-3}}{2} * (3.2803995853997 - 0.45)^2$$

$$I_{d2} = 2.1229578804531 * 10^{-3}$$

Calculation of r_{o2}:

$$r_{02} = \frac{1}{\lambda_2 * I_{d2}}$$

$$r_{02} = \frac{1}{0.006 * 2.1229578804531 * 10^{-3}}$$

$$r_{02} = 78.5 * 10^3$$

Calculation of I_{d4}:

$$V_{g3} = V_{DD} - V_{sg3} \tag{14}$$

$$I_{d4} = \frac{K_{p4}}{2} * (V_{gs4} - V_{th4})^2 \tag{15}$$

$$V_{sg3} = \sqrt{\frac{I_o}{K_{n3}}} + V_{th3}$$

$$V_{sg3} = \sqrt{\frac{I_o}{K_{n3}}} + 0.5$$

$$I_{d4} = \frac{0.16 * 10^{-3}}{2} * ((V_{g3} - V_{DD}) - 0.5)^2$$

$$I_{d4} = \frac{0.16 * 10^{-3}}{2} * (-V_{sg3} - 0.5)^2$$

$$I_{d4} = 0.08 * 10^{-3} * (-\sqrt{\frac{I_o}{K_{n3}}} - 0.5 - 0.5)^2$$

$$I_{d4} = 0.08 * 10^{-3} * (-\sqrt{\frac{1.96 * 10^{-3}}{0.16 * 10^{-3}}} - 1)^2$$

$$I_{d4} = 162 * 10^{-5} A$$

Calculation of r_{o4}:

$$r_{04} = \frac{1}{\lambda_4 * I_{d4}}$$

$$r_{04} = \frac{1}{0.006 * 162 * 10^{-5}}$$

$$r_{04} = 102.88 * 10^3$$

Calculation of $r_{o2}\|\mathbf{r}_{o4}$:

$$r_{o2}\|r_{o4} = \frac{r_{o2} * r_{o4}}{r_{o2} + r_{o4}}$$

$$r_{o2}\|r_{o4} = \frac{78.5 * 10^3 * 102.88 * 10^3}{78.5 * 10^3 + 102.88 * 10^3}$$

$$r_{o2}\|r_{o4} = 44.525747050391 * 10^3$$

Calculation of gain A_V:

$$A_V = -g_{m1} * (r_{o2}\|r_{o4})$$

$$A_V = -1.5 * 10^{-3} * 44.525747050391 * 10^3$$

$$A_V = -66.788620575587$$

2.4 Experimental Procedure

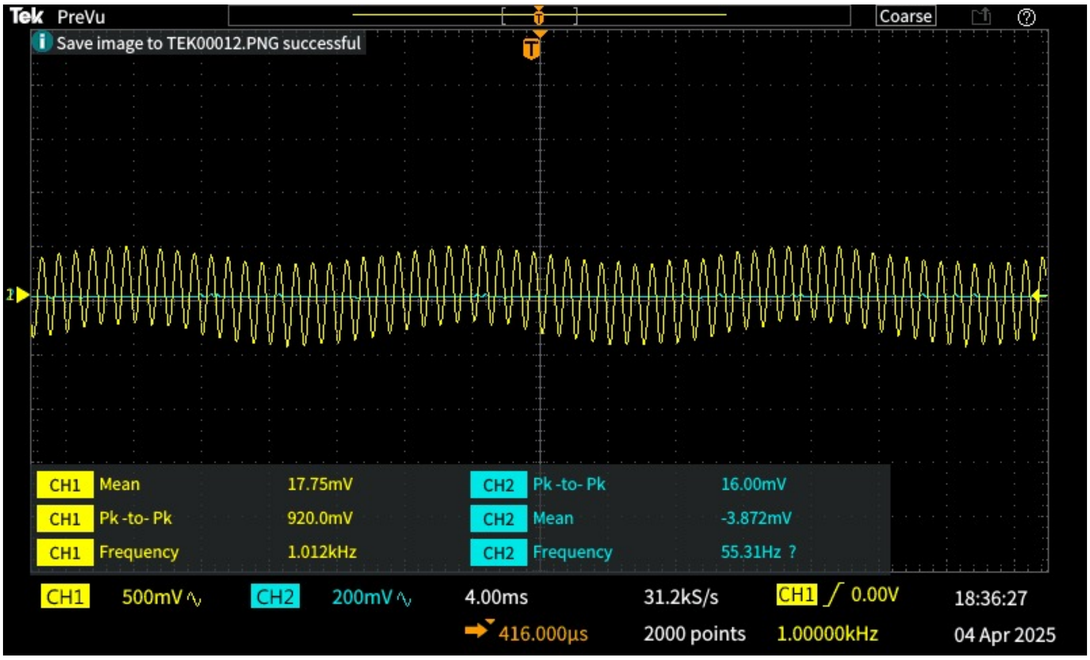
1. Assemble the 5T-OTA circuit on a breadboard using NMOS and PMOS transistors as per the schematic.
2. Set $V_{DD} = 10$V using a regulated power supply.
3. Set the input voltages V_{in1} and V_{in2} to the calculated common-mode input voltage V_{incm}.
4. Use the multimeter to measure all node voltages and verify that all MOSFETs are operating in the saturation region.
5. Measure branch currents using the multimeter or by calculating voltage drops across known resistors.
6. Apply a differential sinusoidal input signal of 40 mVpp, 1 kHz with DC offset equal to $Vincm$ using a function generator.
7. Observe V_{out} and V_{in1} using the oscilloscope.
8. Measure and record the voltage gain from the oscilloscope waveform.

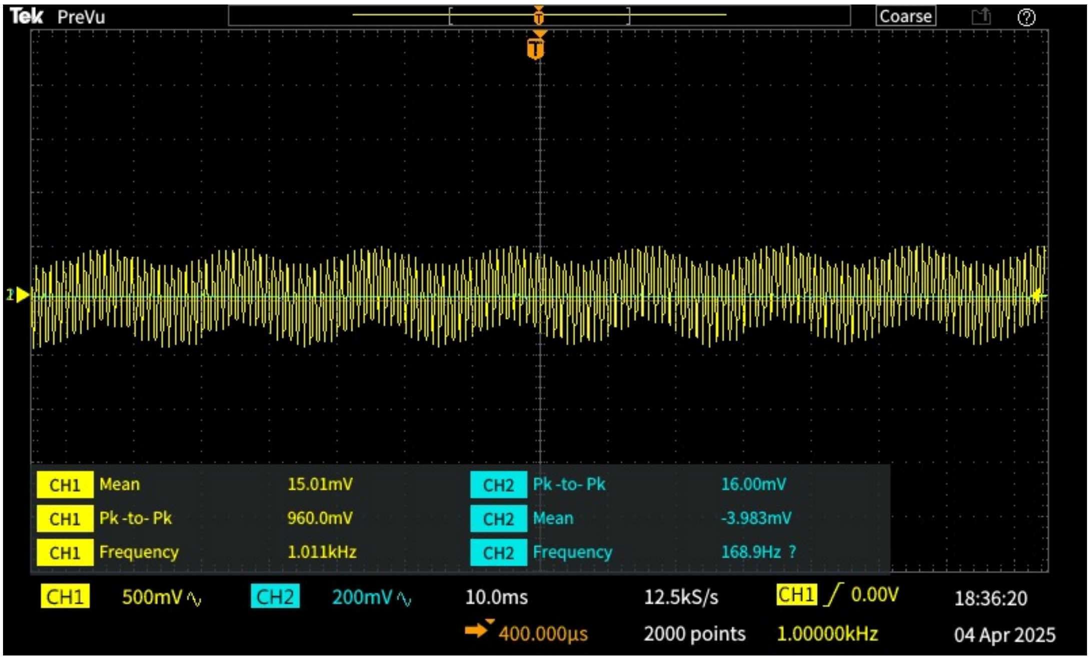
Hardware Implementation

- Build the circuit as per the schematic of 5T-OTA.
- Set $V_{in1} = V_{in2} = V_{incm}$.
- Ensure each MOSFET satisfies the saturation condition:
- If any transistor is in triode region, adjust R_D, V_{incm} or biasing.

2.5 Experimental Results

Plots from the DSO





Node Voltages and Branch Current

Parameter	Value
Gate of M3 (Vg3)	6.23 V
Drain of M1 (Vout)	940 mV
Tail Current across R_D (I_D)	1.99 mA

2.6 Transient Response

- Apply sinusoidal differential input of 40 mVpp, 1 kHz with DC offset of V$incm$.
- Use two function generator channels: Vin1 = 20 mVpp + V$incm$, Vin2 = 20 mVpp + V$incm$, 180° out of phase.
- Plot V_{in1} and V_{out} on the oscilloscope.
- Measure the gain: $A_v = \frac{V_{out}}{V_{in1} - V_{in2}}$

2.7 Key Observations

- Calculated and simulated values of gain.
- Comparison of DC and AC gain.
- Observations on common mode gain.

2.8 Conclusion and Inference

The differential amplifier with active load was successfully designed and implemented. The measured differential gain and node voltages were consistent with theoretical predictions. Proper biasing ensured all MOSFETs operated in the saturation region. This experiment demonstrates the importance of current mirror loading in achieving high gain and proper common-mode voltage stabilization in differential amplifier circuits. It lays the foundation for more complex analog design like operational amplifiers.

2.9 Experiment Completion Status

I have successfully completed all the sections mentioned in this Experiment

Simulation of the Five Transistor OTA Applications: Unity Gain and Inverting Amplifiers

3 Unity Gain Amplifier

3.1 Aim of the Experiment

To design and implement a unity gain amplifier using a five-transistor OTA and analyze its DC and transient response.

3.2 Theory

A unity gain buffer (voltage follower) provides high input impedance and low output impedance, ensuring signal integrity while avoiding loading effects. The circuit utilizes a five-transistor OTA, where the output follows the input voltage with unity gain.

3.3 Circuit Diagram (LT Spice):

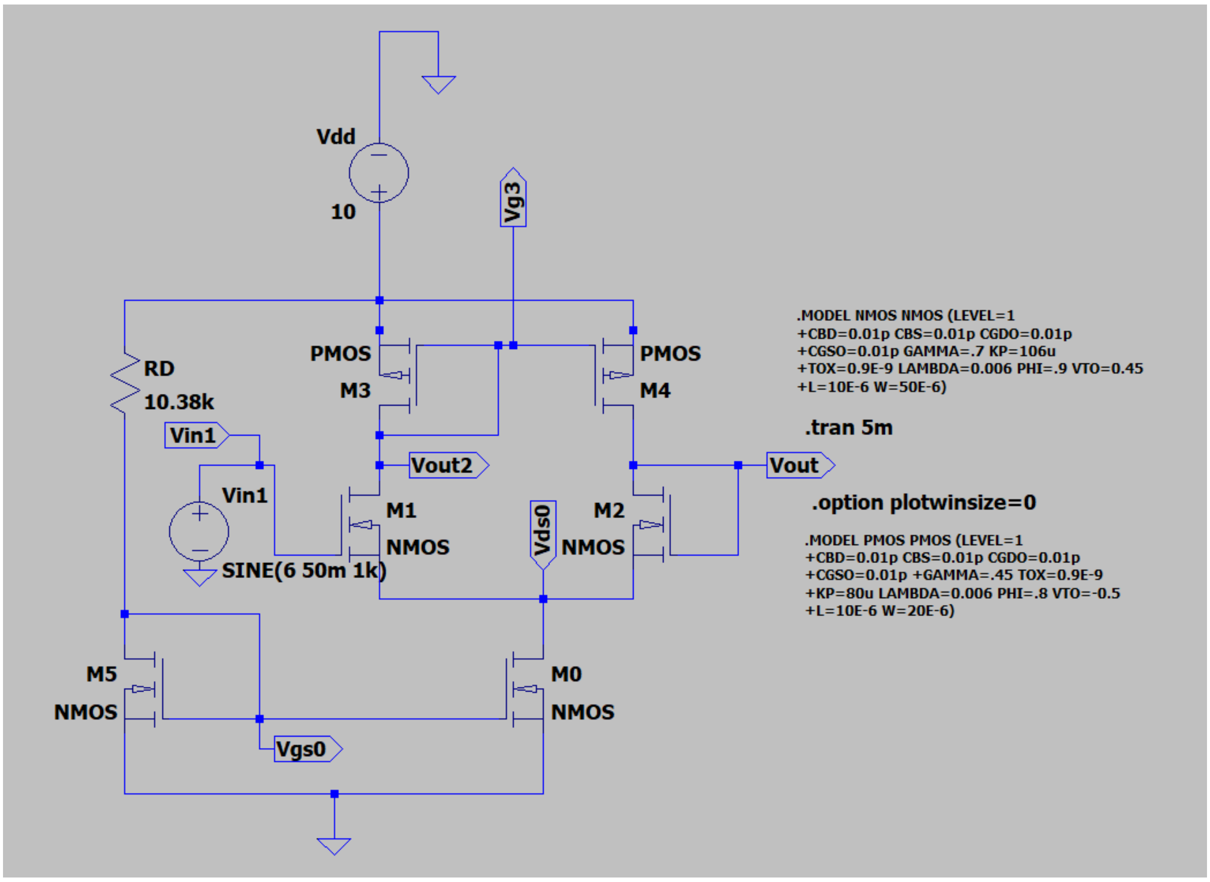


Figure 3: Unity Gain Amplifier

3.4 Circuit Design

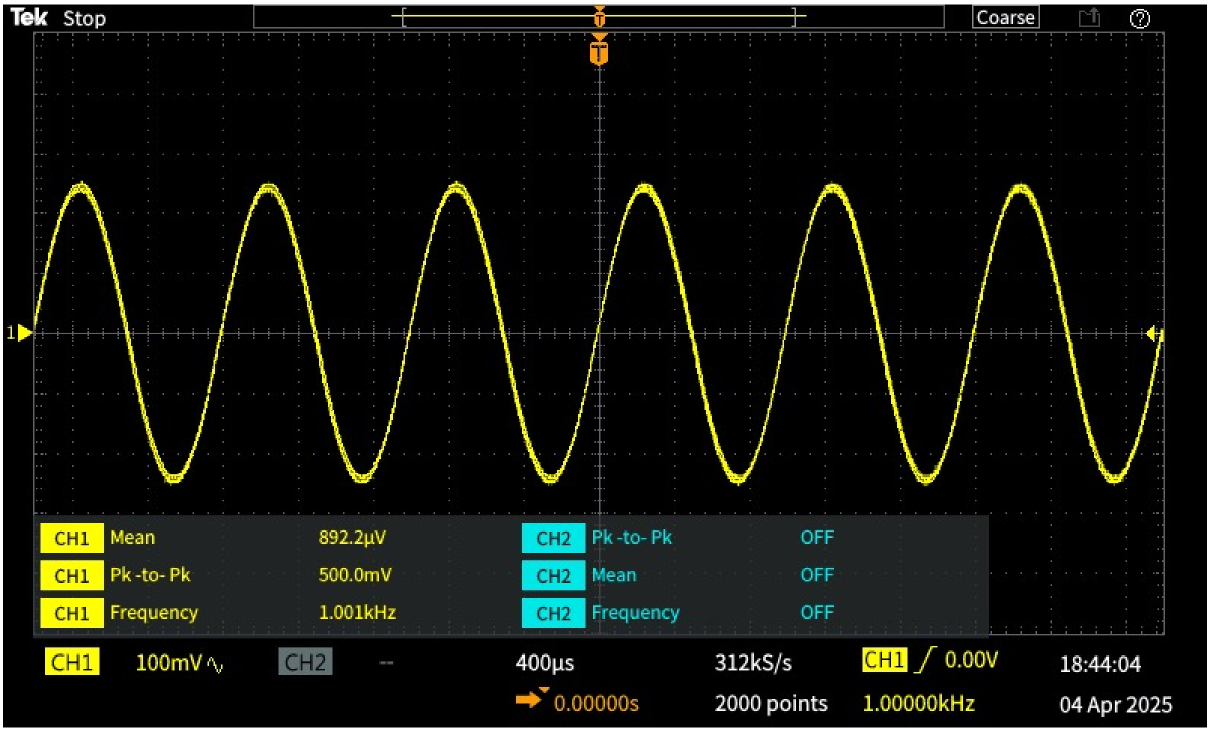
The circuit comprises:

- A five-transistor OTA as the core amplifier.
- The output directly fed back to the inverting input for unity gain.
- The non-inverting input receives the input voltage.
- Power supply: $V_{DD} = 10V$.

Experimental Procedure

1. Assemble the Five-Transistor OTA circuit on a breadboard as per Figure 3.
2. Set Vdd = 10 V.
3. Apply a sinusoidal input Vin1 with 500 mVpp, 1 KHz frequency, and Vincm as the DC offset.
4. Observe and plot the input and output waveforms on the oscilloscope.
5. Measure output amplitude and verify unity gain behavior.

3.5 Experimental Results



3.6 Key Observations

- The output voltage closely follows the input voltage.
- No phase shift is observed.
- The gain is approximately 1.

3.7 Conclusion and Inference

The unity gain buffer built using a five-transistor OTA successfully replicated the input signal with minimal distortion, confirming its unity gain and buffering capability. This experiment demonstrates the effectiveness of a five-transistor OTA in designing analog buffer circuits suitable for use in analog front-end systems.

3.8 Experiment Completion Status

I have successfully completed all the sections mentioned in this Experiment

4 Inverting Amplifier

4.1 Aim of the Experiment

To design and implement an inverting amplifier using a five-transistor OTA and analyze its gain and phase response.

4.2 Theory

An inverting amplifier using a five-transistor OTA operates with negative feedback, providing a controlled gain. The circuit follows the equation:

$$A_v = -\frac{R_2}{R_1} \tag{16}$$

where $R_2 = 10M\Omega$ and $R_1 = 1M\Omega$, giving a gain of -10.

4.3 Circuit Diagram (LT Spice):

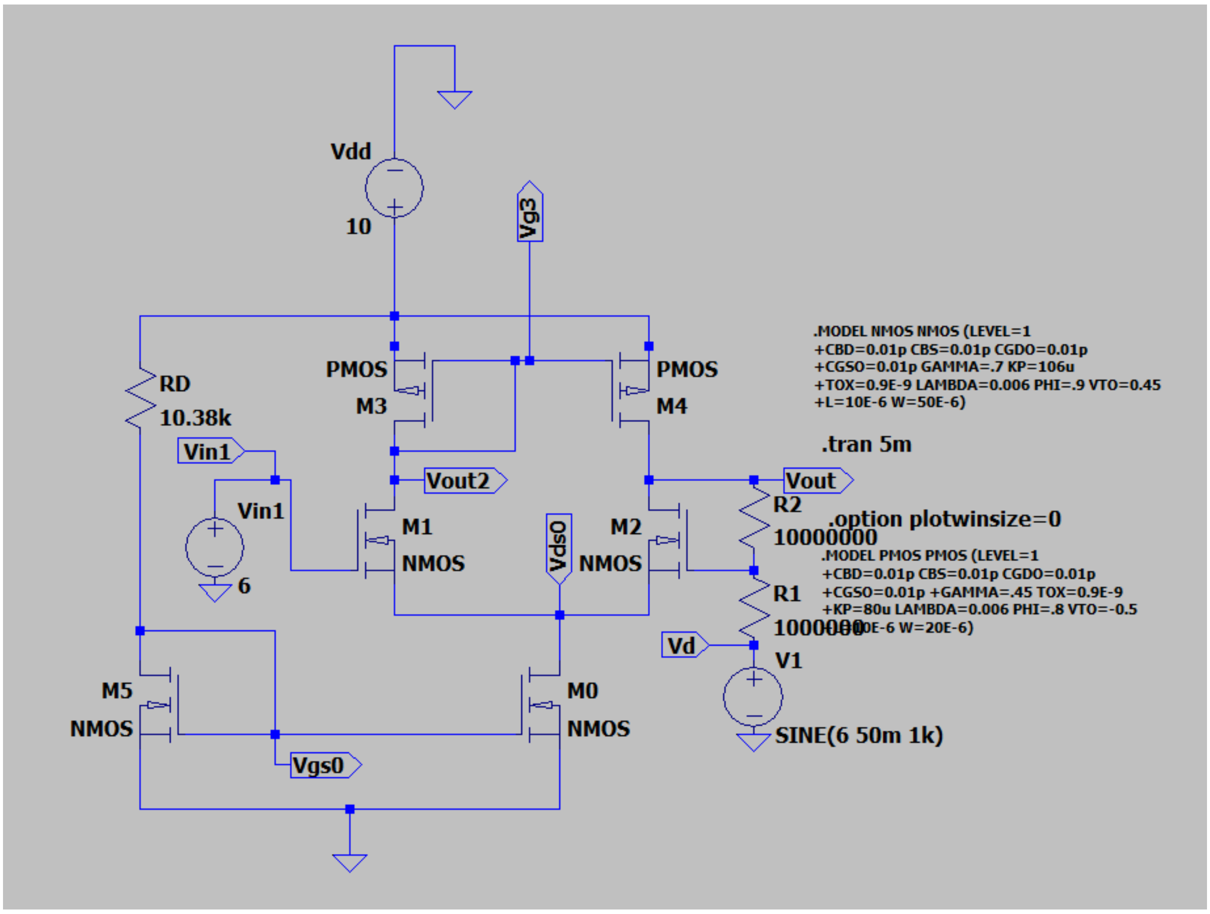


Figure 4: Inverting Amplifier

4.4 Circuit Design

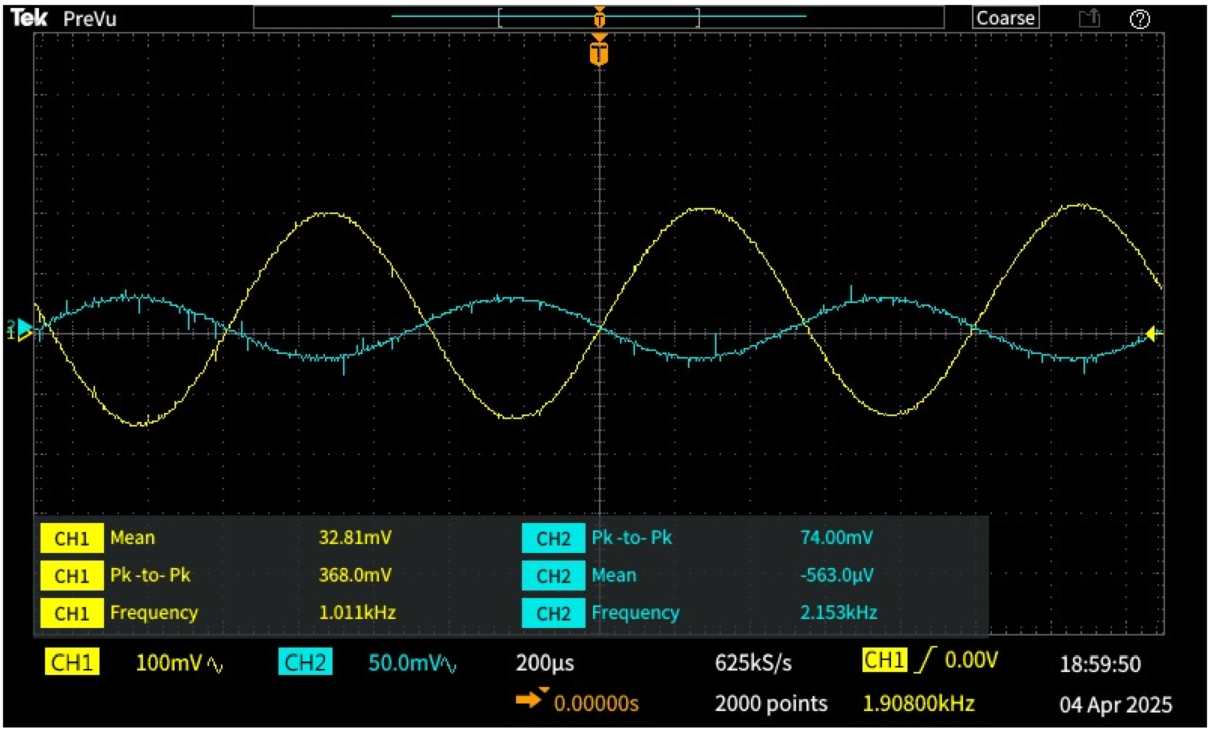
The circuit consists of:

- A five-transistor OTA.
- Resistors R_1 and R_2 to set the gain.
- Bias voltage set at V_{incm}.
- Power supply: $V_{DD} = 10V$.

Experimental Procedure

1. Assemble the inverting amplifier circuit using the Five-Transistor OTA on the breadboard.
2. Set Vdd = 10 V and apply Vincm as bias voltage at the gate of M1.
3. Apply Vbias + vd to R1, where vd is a sinusoidal input of 50 mVpp, 1 KHz.
4. Measure Vout and input waveforms using the oscilloscope.
5. Calculate theoretical gain as $-\frac{R2}{R1} = -10$.
6. Measure actual gain and phase shift.

4.5 Experimental Results



4.6 Key Observations

- The output signal is inverted.
- The measured gain is close to -10.
- A phase shift of 180° is observed.

4.7 Conclusion and Inference

The inverting amplifier using a Five-Transistor OTA achieved the expected phase shift and amplification. The high resistance values help maintain low loading and accurate gain. This setup validates the Five-Transistor OTA's use in analog signal conditioning applications, where gain and inversion are required.

4.8 Experiment Completion Status

I have successfully completed all the sections mentioned in this Experiment