Indian Institute of Technology Bombay

Analog Circuits Lab
EE 230

Lab 10a
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Contents

1 Differential Amplifier with Resistive Load

1.1 Aim of the Experiment

To design and simulate a differential amplifier with a resistive load, ensuring that the circuit meets the specified design constraints, including gain, input common-mode voltage, and output common-mode voltage.

1.2 Theory

1.2.1 Introduction

A differential amplifier is a fundamental building block in analog circuits, used for amplifying the difference between two input signals while rejecting common-mode noise. The circuit comprises:

- M1, M2: NMOS differential input pair
- R2, R3: Resistive loads
- M3: Tail current source
- R1, M3, and M4: Current mirror

The circuit is powered by a supply voltage of $V_{DD} = 10V$.

1.2.2 Circuit Diagram (LT Spice):

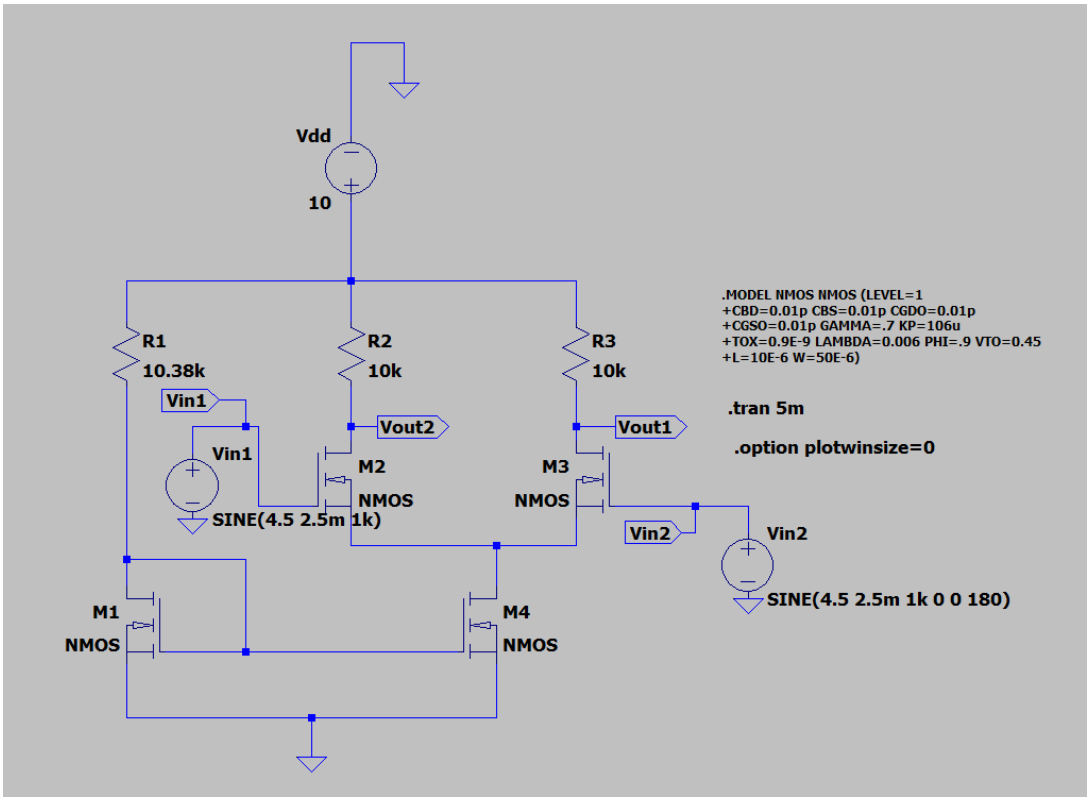


Figure 1: Differential Amplifier with Resistive Load

1.2.3 Design Considerations

The required specifications are:

- Gain $A_v > 12dB$
- Minimum input common-mode voltage $V_{in,cm(min)} = 3.5V$
- Output common-mode voltage $5V < V_{out,cm} < 7V$

1.3 Calculation Steps

1.3.1 Minimum Input Common-Mode Voltage

The minimum input common-mode voltage is determined by ensuring all MOSFETs operate in the saturation region:

$$V_{in,cm(min)} = V_{GS1} + V_{d_{sat3}} \tag{1}$$

Expanding using device parameters:

$$V_{in,cm(min)} = V_{TH1} + \sqrt{\frac{I_{tail}}{K_{n1}}} + \sqrt{\frac{2I_{tail}}{K_{n3}}} \tag{2}$$

Solving for I_{tail} to satisfy $V_{in,cm(min)} = 3.5V$.

$$3.5 = 4.5 + \sqrt{\frac{I_{tail}}{(0.53) * 10^{-3}}} + \sqrt{\frac{2I_{tail}}{(0.53) * 10^{-3}}}$$

$$I_{tail} = 0.84591mA$$

1.3.2 Gain Calculation

The voltage gain of the differential amplifier is:

$$A_v = g_{m1}R_2 \tag{3}$$

where g_{m1} is the transconductance of M1:

$$g_{m1} = \sqrt{2 * K_{n1} * I_{tail}} \tag{4}$$

Solving for R_2 to meet $A_v > 12dB$.

let $R_2 = 10$ kΩ,

$$A_V = \sqrt{2 * I_{tail} * K_{n1}} * R_2$$

$$(A_V)_{in-dB} = 20 * log(\sqrt{2 * I_{tail} * K_{n1}} * R_2)$$

$$(A_V)_{in-dB} = 20 * log(\sqrt{2 * 0.84591 * 10^{-3} * (0.53) * 10^{-3}} * (10) * 10^3)$$

$$(A_V)_{in-dB} = 19.5263$$

1.3.3 Output Common-Mode Voltage

The output common-mode voltage is given by:

$$V_{out,cm} = V_{DD} - \frac{I_{tail}}{2} R_2 \tag{5}$$

$$V_{out,cm} = 10 - \frac{0.84591 * 10^{-3}}{2} * 10^4$$

$$V_{out,cm} = 5.77045V$$

1.3.4 Current Mirror Reference Current

The reference current I_{ref} is set by resistor R_1:

$$I_{ref} = \frac{K_n}{2} * (V_{gs} - V_{th})^2 \tag{6}$$

$$0.84591 * 10^{-3} = \frac{(0.53) * 10^{-3}}{2} * (V_{gs} - 0.45)^2$$

$$0.58091 * 10^{-3} = (V_{gs} - 0.45)^2$$

for M_4,

$$V_{gs} = 1.2121V$$

$$R_1 = \frac{V_{DD} - V_{gs}}{I_{ref}}$$

$$R_1 = \frac{10 - 1.2121}{0.84591 * 10^{-3}}$$

$$R_1 = 10388.6938\Omega$$

1.4 Simulation

1.4.1 Circuit Implementation in LTSpice

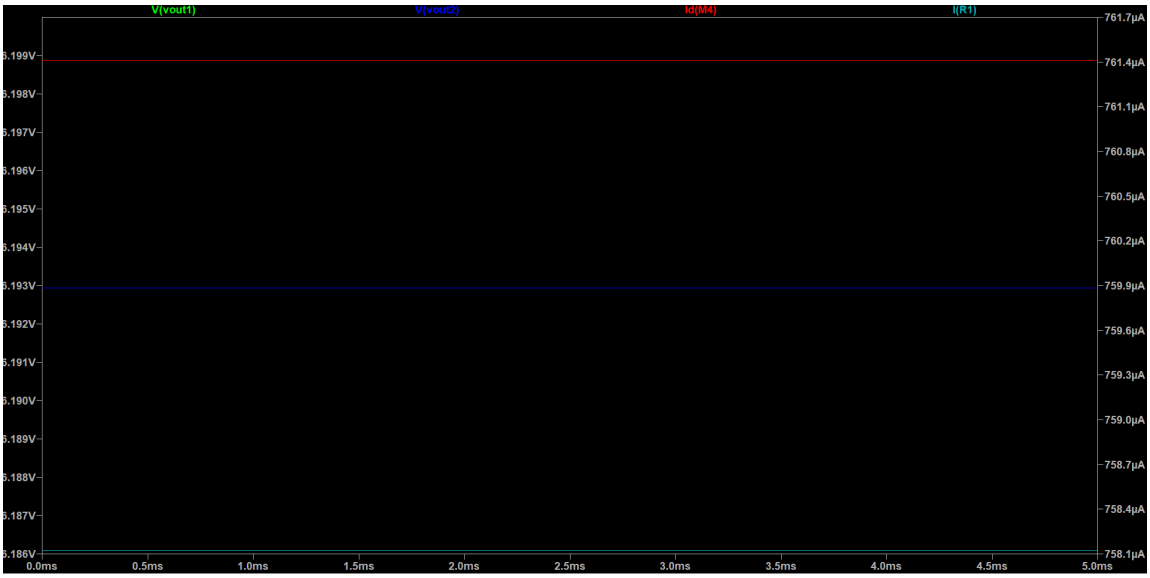
The schematic for the differential amplifier is drawn in LTSpice, ensuring:

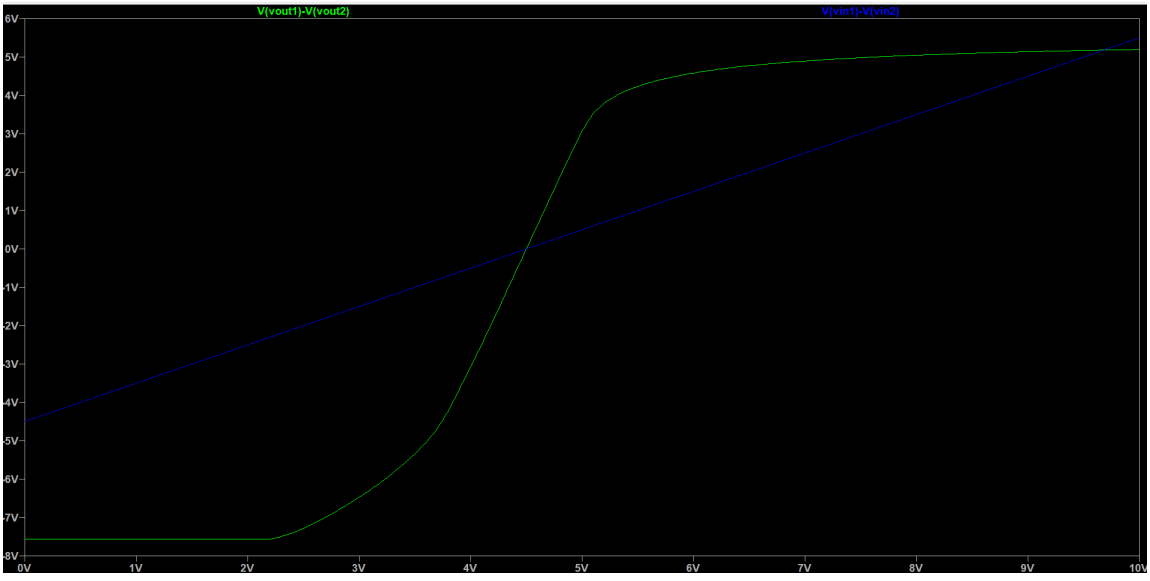
- $V_{in1} = V_{in2} = 4.5V$
- $V_{DD} = 10V$
- All MOSFETs operate in the saturation region ($V_{DS} > V_{GS} - V_{TH}$)

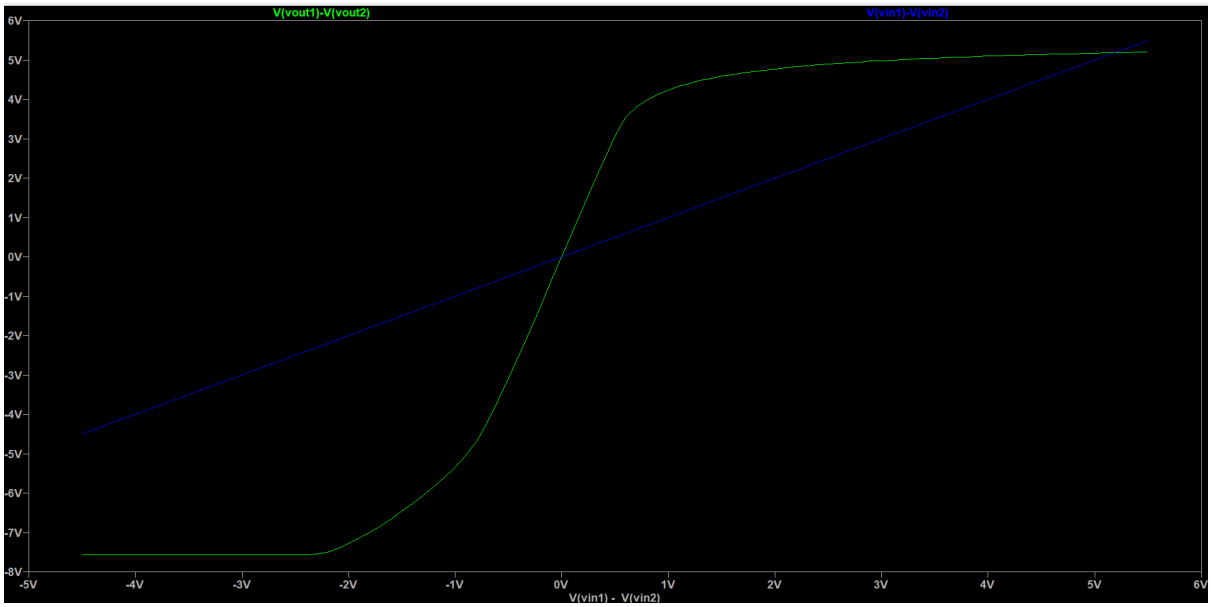
1.4.2 Simulation Steps

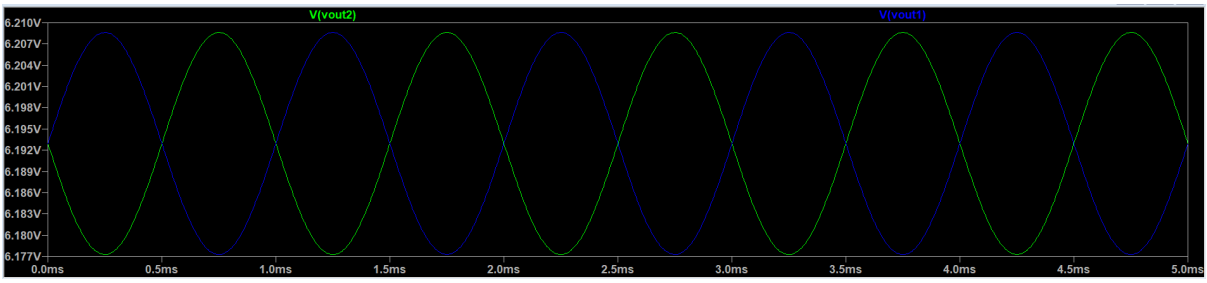
1. Perform DC operating point analysis to verify all node voltages and branch currents.
2. Tabulate results including node voltages, branch currents, and MOSFET operating regions.
3. Sweep V_{in1} from $0V$ to $10V$, keeping $V_{in2} = 4.5V$, and plot $(V_{out1} - V_{out2})$ vs. $(V_{in1} - V_{in2})$.
4. Apply a sinusoidal differential input:
   $V_{in1} = 5mV_{pp}, 1kHz, 4.5V$ offset
   $V_{in2} = 5mV_{pp}, 1kHz, 180°$ phase shift, 4.5V offset.
5. Plot V_{out1} and V_{out2}, observe phase shift, and measure differential gain.

1.5 Simulation Results









1.6 Key Observations

- DC operating point analysis confirms that all transistors operate in saturation.
- The differential amplifier gain meets or exceeds $12dB$.
- The output common-mode voltage falls within the required range ($5V < V_{out,cm} < 7V$).
- The differential input produces expected phase-shifted outputs.

1.7 Conclusion and Inference

The designed **differential amplifier with resistive load** was successfully simulated in LTSpice. The circuit met the required gain, input common-mode voltage, and output common-mode voltage constraints. The phase shift and differential gain were validated, demonstrating proper amplifier functionality.

1.8 Experiment Completion Status

I have successfully completed all the sections mentioned in this Experiment

2 Differential Amplifier with Active Load (5T-OTA)

2.1 Aim of the Experiment

To design and analyze a differential amplifier with an active load (Five-Transistor Operational Transconductance Amplifier, 5T-OTA), study its gain characteristics, input/output common mode voltage, and compare simulation results with theoretical calculations.

2.2 Theory

A differential amplifier with a current mirror load, also known as a **Five Transistor OTA (5T-OTA)**, is widely used in designing operational amplifiers (Op-Amps). The circuit consists of:

- M_1 and M_2 forming the NMOS differential pair.
- M_3 and M_4 acting as a current mirror load.
- M_0 as the tail current source.
- M_5 mirroring the current to M_0.

The tail current (I_0) is determined by the value of R_D.

2.2.1 Circuit Diagram (LT Spice):

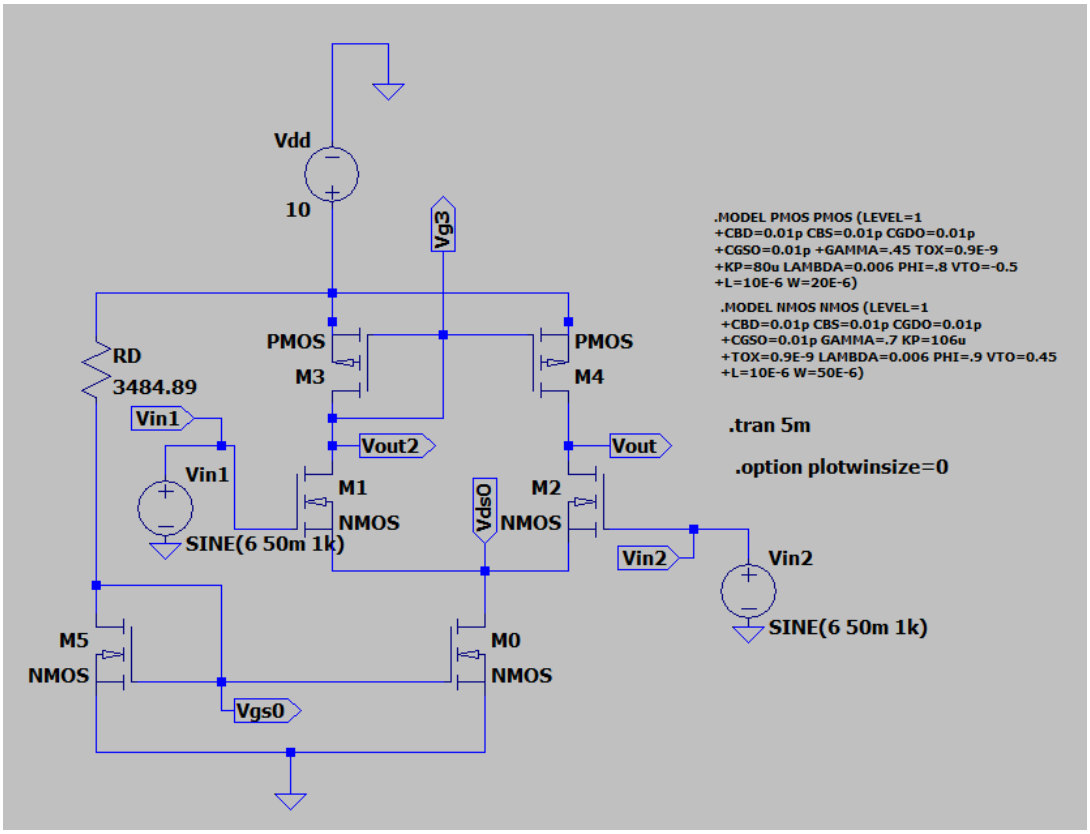


Figure 2: Differential Amplifier with Active Load

2.3 Calculation Steps

2.3.1 Calculation of current I_o

We know that,

$$V_{out,dc} = V_{DD} - \sqrt{\frac{I_o}{K_{n3}}} - V_{th3}$$

$$6 = 10 - \sqrt{\frac{I_o}{0.16 * 10^{-3}}} - 0.5$$

$$I_o = 1.96mA$$

2.3.2 Input Common Mode Voltage (V_{incm})

To ensure all transistors operate in the **saturation region**, the input common mode voltage must satisfy:

$$V_{incm(min)} = \sqrt{\frac{2I_0}{K_{no}}} + \sqrt{\frac{I_0}{K_{n1}}} + V_{th1} \tag{7}$$

$$V_{incm(max)} = V_{outdc} + V_{th1} \tag{8}$$

Thus, V_{incm} should be chosen within these limits.

$$V_{in,cm(min)} = \sqrt{\frac{2 * I_o}{K_{no}}} + \sqrt{\frac{I_o}{K_{n1}}} + V_{th1}$$

$$V_{in,cm(min)} = \sqrt{\frac{2 * 1.96 * (10^{-3})}{0.53 * (10^{-3})}} + \sqrt{\frac{1.96 * (10^{-3})}{0.53 * (10^{-3})}} + 0.45$$

$$V_{in.cm(min)} = 5.0569808291249V$$

$$V_{in.cm(max)} = V_{out,dc} + V_{th1}$$

$$V_{in.cm(max)} = 6 + 0.45$$

$$V_{in.cm(max)} = 6.45V$$

Assuming $V_{in,cm} = 6$V

2.3.3 Output Common Mode Voltage ($V_{out,cm}$)

Due to negative feedback, the equilibrium condition ensures:

$$V_{outdc} = V_{DD} - \frac{I_{tail} * R_2}{2} \tag{9}$$

$$6 = 10 - \frac{1.96 * (10^{-3}) * R_2}{2}$$

$$\frac{1.96 * (10^{-3}) * R_2}{2} = 4$$

$$R_2 = 4081.632653\Omega$$

2.3.4 Calculation of resistance R_D

$$V_{DD} - V_{gso} = I_o * R_D \tag{10}$$

$$I_o = \frac{K_{no}}{2} * (V_{gso} - V_{th0})^2 \tag{11}$$

$$V_{gso} = \sqrt{\frac{2 * 1.96 * (10^{-3})}{0.53 * (10^{-3})}} + 0.45$$

$$V_{gso} = 4.7324785628779 - 1.563$$

$$V_{gso} = 3.1696004146003V$$

substitute back V_{gso} back in equation(10),

$$10 - 3.1696004146003 = I_o * R_D$$

$$R_D = \frac{6.830399585399}{1.96 * (10^{-3})}$$

$$R_D = 3484.8977476528\Omega$$

2.3.5 Gain A_V

The voltage gain of the **5T-OTA** is given by:

$$A_V = -g_{m1}(r_{o2} \parallel r_{o4}) \tag{12}$$

where r_o is defined as:

$$r_o = \frac{1}{\lambda I_D} \tag{13}$$

This gain is highly dependent on the **channel length modulation coefficient** (λ), which can be obtained from the MOSFET model file.
Using:

- $V_{sg3} = \frac{I_0}{K_{n3}} + V_{th3}$.
- I_0 is the tail current source.

Calculation of V_{gs1}:

$$V_{gs1} = V_{in1} - (V_{ds})_{sat0}$$

$$V_{gs1} = 6 - (V_{gs0} - V_{th0})$$

$$V_{gs1} = 6 - (3.1696004146003 - 0.45)$$

$$V_{gs1} = 3.2803995853997V$$

Calculation of g_{m1}:

$$g_{m1} = \sqrt{2 * I_{d1} * K_{n1}}$$

$$g_{m1} = k_{n1} * (V_{gs1} - V_{th1})$$

$$g_{m1} = 0.53 * 10^{-3} * (3.2803995853997 - 0.45)$$

$$g_{m1} = 1.5 * 10^{-3}$$

Calculation of I_{d2}:

$$I_{d2} = \frac{K_{n2}}{2} * (V_{gs2} - V_{th2})^2$$

$$I_{d2} = \frac{0.53 * 10^{-3}}{2} * (3.2803995853997 - 0.45)^2$$

$$I_{d2} = 2.1229578804531 * 10^{-3}$$

Calculation of r_{o2}:

$$r_{02} = \frac{1}{\lambda_2 * I_{d2}}$$

$$r_{02} = \frac{1}{0.006 * 2.1229578804531 * 10^{-3}}$$

$$r_{02} = 78.5 * 10^3$$

Calculation of I_{d4}:

$$V_{g3} = V_{DD} - V_{sg3} \tag{14}$$

$$I_{d4} = \frac{K_{p4}}{2} * (V_{gs4} - V_{th4})^2 \tag{15}$$

$$V_{sg3} = \sqrt{\frac{I_o}{K_{n3}}} + V_{th3}$$

$$V_{sg3} = \sqrt{\frac{I_o}{K_{n3}}} + 0.5$$

$$I_{d4} = \frac{0.16 * 10^{-3}}{2} * ((V_{g3} - V_{DD}) - 0.5)^2$$

$$I_{d4} = \frac{0.16 * 10^{-3}}{2} * (-V_{sg3} - 0.5)^2$$

$$I_{d4} = 0.08 * 10^{-3} * (-\sqrt{\frac{I_o}{K_{n3}}} - 0.5 - 0.5)^2$$

$$I_{d4} = 0.08 * 10^{-3} * (-\sqrt{\frac{1.96 * 10^{-3}}{0.16 * 10^{-3}}} - 1)^2$$

$$I_{d4} = 162 * 10^{-5} A$$

Calculation of r_{o4}:

$$r_{04} = \frac{1}{\lambda_4 * I_{d4}}$$

$$r_{04} = \frac{1}{0.006 * 162 * 10^{-5}}$$

$$r_{04} = 102.88 * 10^3$$

Calculation of $r_{o2} \| \mathbf{r}_{o4}$:

$$r_{o2} \| r_{o4} = \frac{r_{o2} * r_{o4}}{r_{o2} + r_{o4}}$$

$$r_{o2} \| r_{o4} = \frac{78.5 * 10^3 * 102.88 * 10^3}{78.5 * 10^3 + 102.88 * 10^3}$$

$$r_{o2} \| r_{o4} = 44.525747050391 * 10^3$$

Calculation of gain A_V:

$$A_V = -g_{m1} * (r_{o2} \| r_{o4})$$

$$A_V = -1.5 * 10^{-3} * 44.525747050391 * 10^3$$

$$A_V = -66.788620575587$$

2.4 Simulation

2.4.1 Design Steps

1. Design the amplifier to achieve $V_{outdc} = 6V$ with $V_{DD} = 10V$.
2. Using equation (3), calculate the required tail current I_0.
3. Determine the limits for V_{incm} and select an appropriate value.
4. Calculate R_D based on I_0.

2.4.2 Simulation Steps

1. Draw the schematic of the differential amplifier with active load in LTspice.

   DC Analysis

2. Apply $V_{in1} = V_{in2} = V_{incm}$ and perform DC analysis. Tabulate:
   - Node voltages.
   - Branch currents.
   - MOSFET operating regions.

AC Analysis

3. Apply a sinusoidal differential input:

   - V_{in1} = 5mVpp, 1kHz.
   - V_{in2} = 5mVpp, 1kHz (180° phase-shifted).
   - Offset = V_{incm}.

   Plot V_{out} and $(V_{in1} - V_{in2})$ and report the gain.

4. Perform AC analysis and determine the DC gain. Compare with transient analysis results.

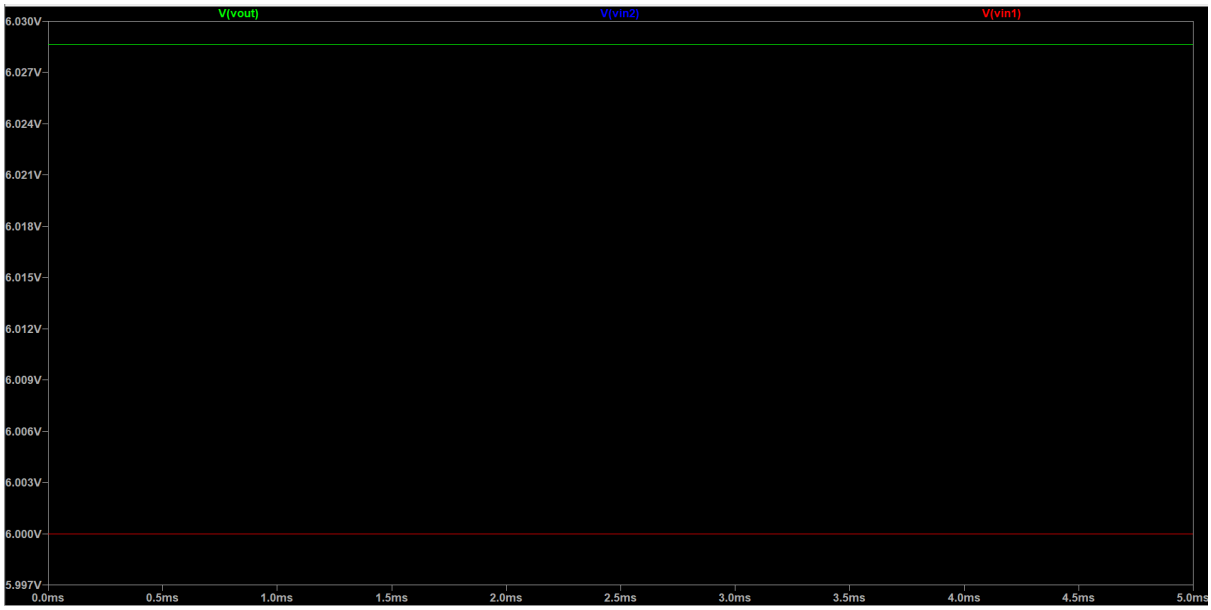
Common Mode Gain Measurement

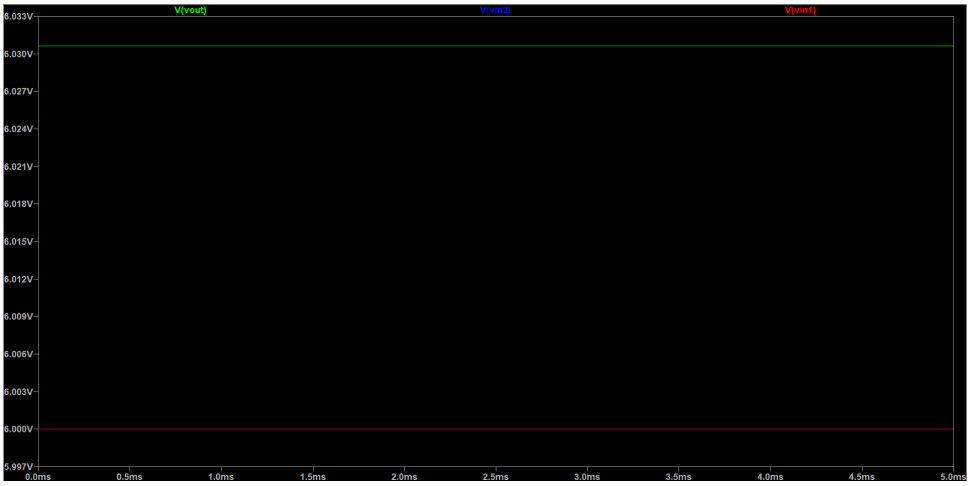
5. Measure the common mode gain:

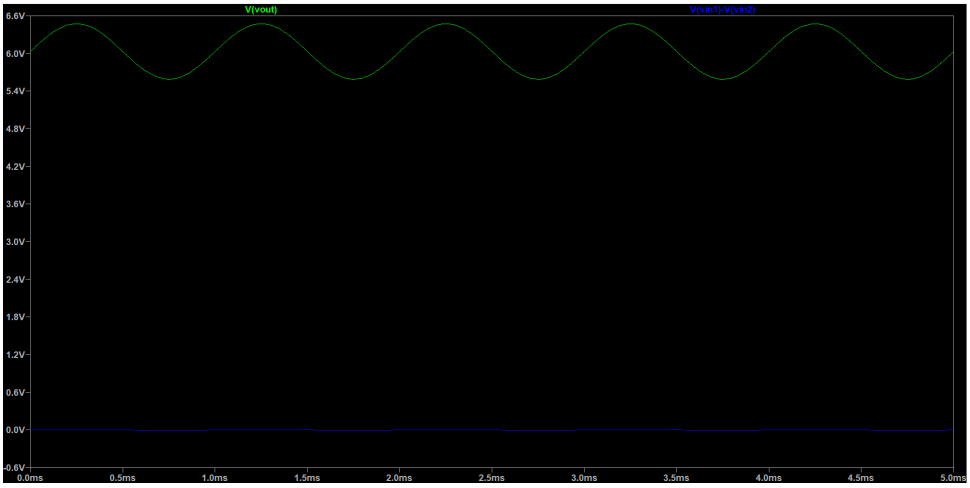
   - Short V_{in1} and V_{in2}.
   - Apply a sine wave (100mVpp, 1kHz, offset = V_{incm}).
   - Plot the output waveform.

   Report the common mode gain.

2.5 Simulation Results







2.6 Key Observations

Summarize the key findings:

- Calculated and simulated values of gain.
- Comparison of DC and AC gain.
- Observations on common mode gain.

Discuss any discrepancies and suggest improvements.

2.7 Conclusion and Inference

The differential amplifier with an active load was successfully simulated. The measured gain closely matched the theoretical calculations. The output common mode voltage was within the expected range, ensuring correct circuit operation. The experiment demonstrated the importance of current mirrors in differential amplifiers. The gain dependency on transistor parameters was validated, highlighting trade-offs between gain and output voltage range.

2.8 Experiment Completion Status

I have successfully completed all the sections mentioned in this Experiment

Simulation of the Five Transistor OTA Applications: Unity Gain and Inverting Amplifiers

3 Unity Gain Amplifier

3.1 Aim of the Experiment

To design and simulate a unity gain amplifier using a five-transistor OTA and analyze its DC and transient response.

3.2 Theory

A unity gain buffer (voltage follower) provides high input impedance and low output impedance, ensuring signal integrity while avoiding loading effects. The circuit utilizes a five-transistor OTA, where the output follows the input voltage with unity gain.

3.3 Circuit Diagram (LT Spice):

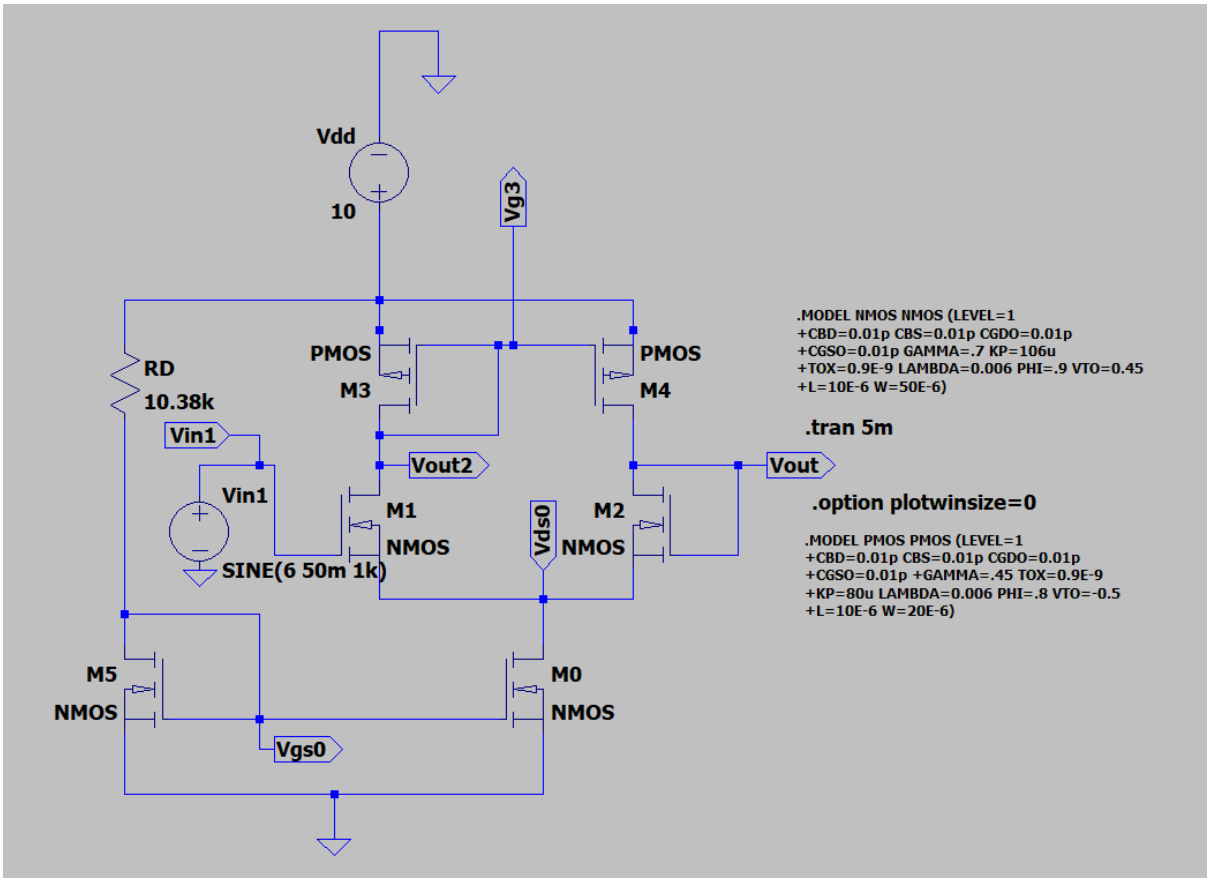


Figure 3: Unity Gain Amplifier

3.4 Circuit Design

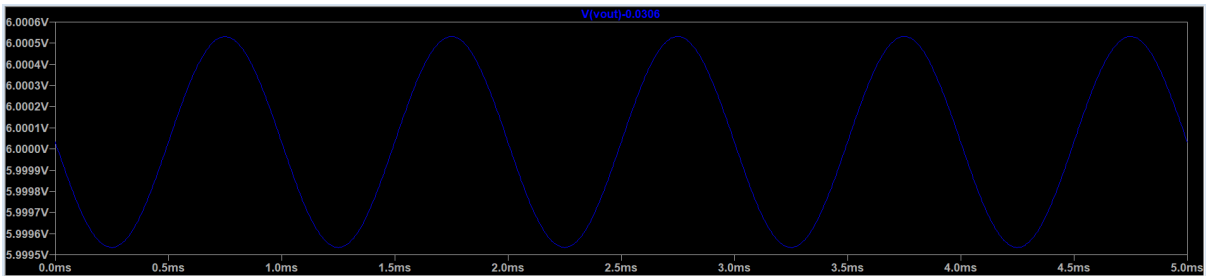
The circuit comprises:

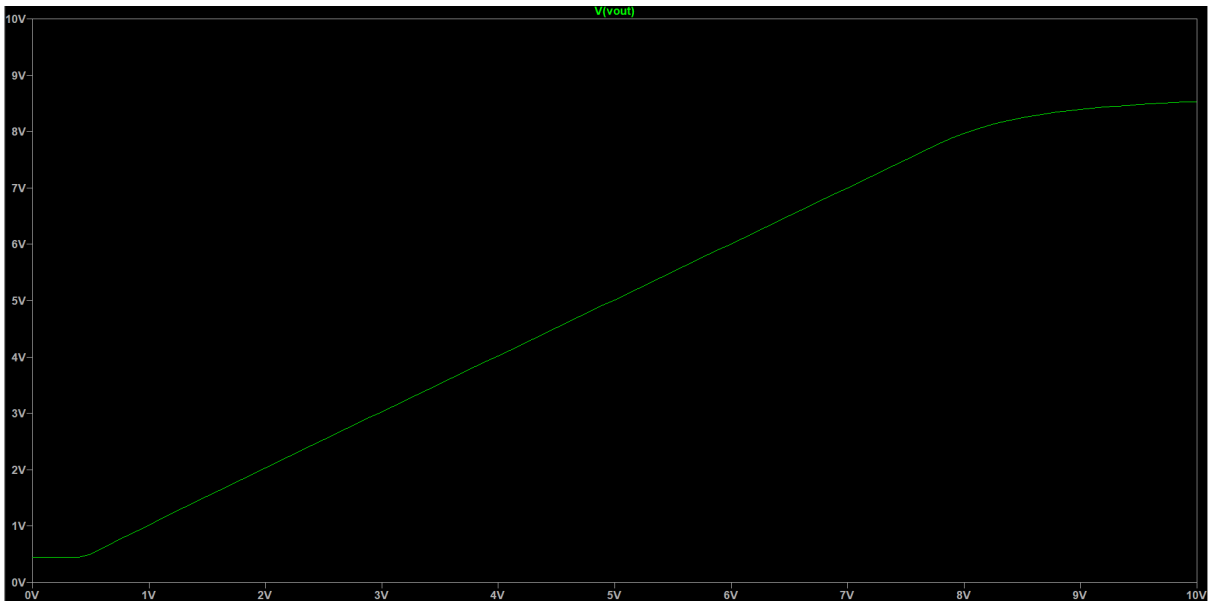
- A five-transistor OTA as the core amplifier.
- The output directly fed back to the inverting input for unity gain.
- The non-inverting input receives the input voltage.
- Power supply: $V_{DD} = 10V$.

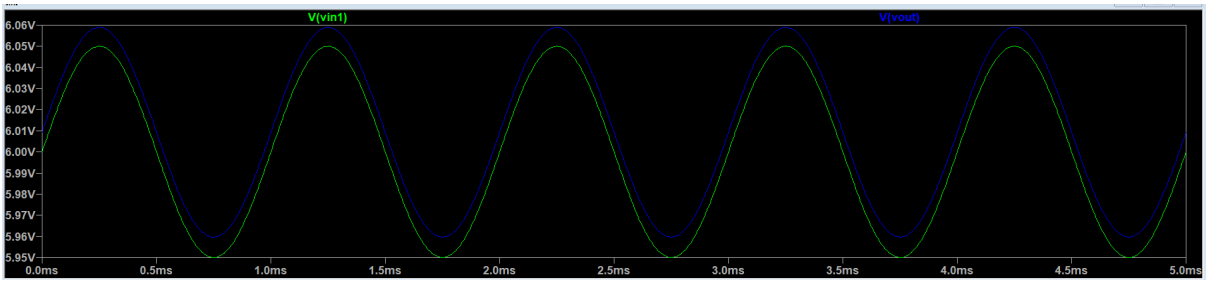
3.5 Simulation Steps

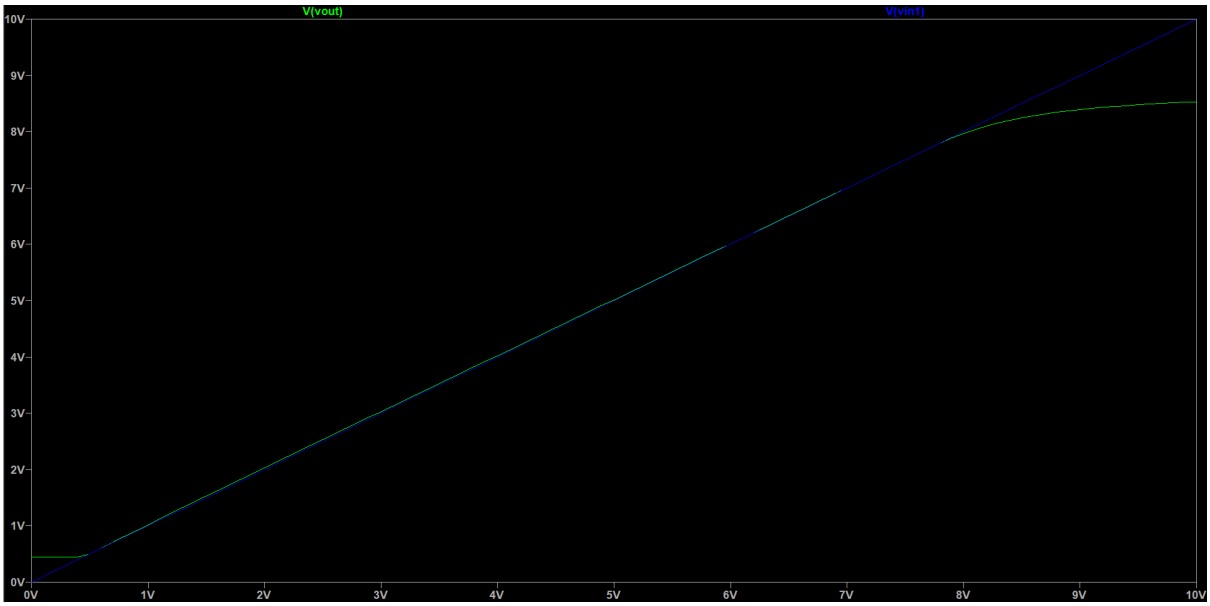
1. Design the circuit in LTspice.
2. Apply a DC sweep to Vin from 0V to 10V in 0.1V steps.
3. Perform transient analysis with $V_{in} = 100mV_{pp}$, $1kHz$ with a DC offset of V_{incm}.
4. Measure and plot V_{out} against V_{in}.

3.6 Simulation Results









3.7 Key Observations

- The output voltage closely follows the input voltage.
- No phase shift is observed.
- The gain is approximately 1.

3.8 Conclusion and Inference

The unity gain amplifier successfully follows the input voltage, confirming its buffering capability without amplification or attenuation. The five-transistor OTA effectively functions as a voltage buffer with high input impedance and low output impedance, making it suitable for signal conditioning applications.

3.9 Experiment Completion Status

I have successfully completed all the sections mentioned in this Experiment

4 Inverting Amplifier

4.1 Aim of the Experiment

To design and simulate an inverting amplifier using a five-transistor OTA and analyze its gain and phase response.

4.2 Theory

An inverting amplifier using a five-transistor OTA operates with negative feedback, providing a controlled gain. The circuit follows the equation:

$$A_v = -\frac{R_2}{R_1} \tag{16}$$

where $R_2 = 10M\Omega$ and $R_1 = 1M\Omega$, giving a gain of -10.

4.3 Circuit Diagram (LT Spice):

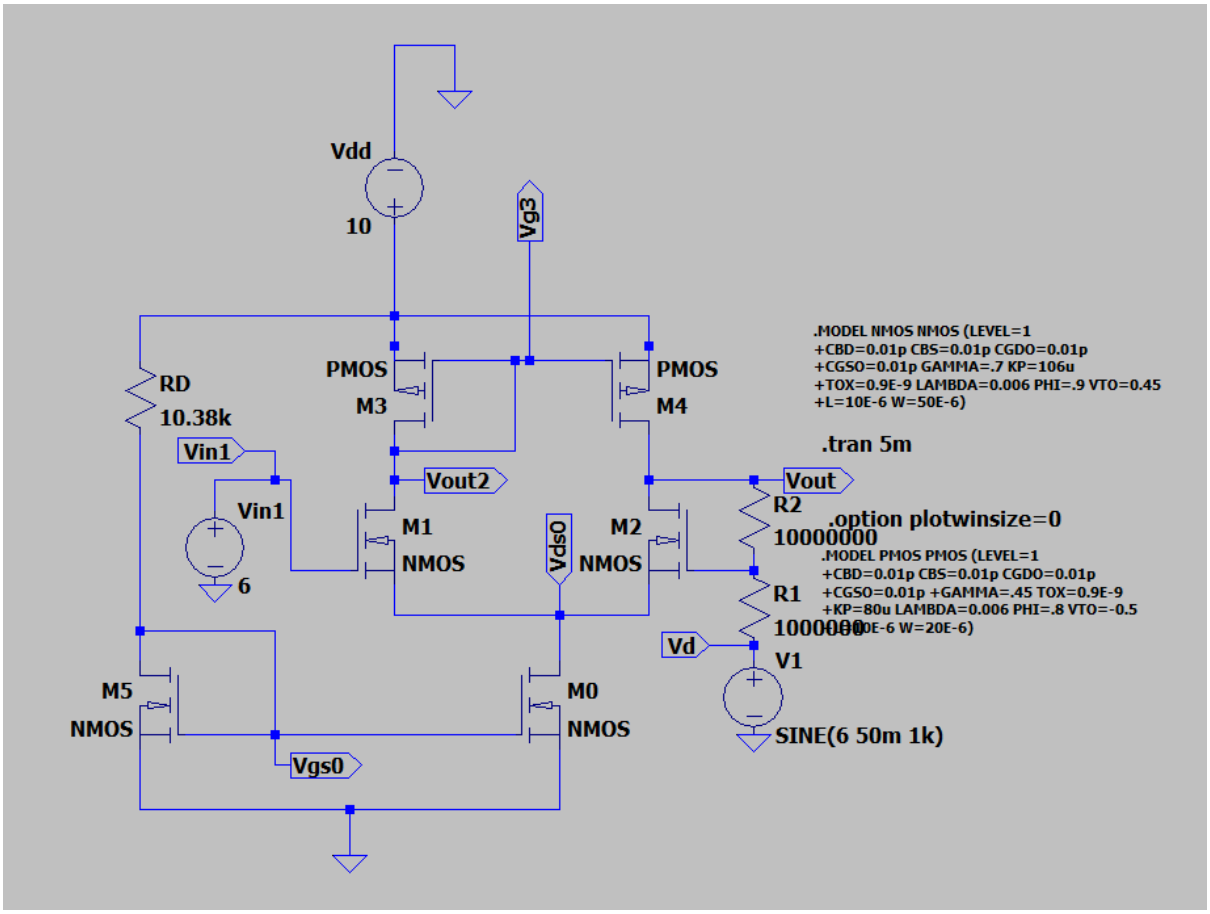


Figure 4: Inverting Amplifier

4.4 Circuit Design

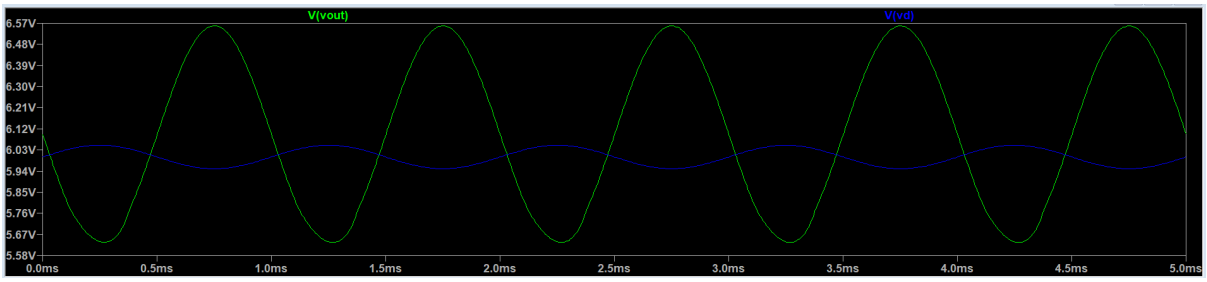
The circuit consists of:

- A five-transistor OTA.
- Resistors R_1 and R_2 to set the gain.
- Bias voltage set at V_{incm}.
- Power supply: $V_{DD} = 10V$.

4.5 Simulation Steps

1. Design the circuit in LTspice.
2. Apply a sinusoidal input of $100mV_{pp}$, $1kHz$, with an offset of V_{incm}.
3. Measure V_{out} and calculate gain.
4. Plot V_{out} and compare phase shift with the input.

4.6 Simulation Results



4.7 Key Observations

- The output signal is inverted.
- The measured gain is close to -10.
- A phase shift of 180° is observed.

4.8 Conclusion and Inference

The inverting amplifier successfully provides a gain of -10, demonstrating the negative feedback mechanism and controlled amplification. The five-transistor OTA, combined with resistors, enables precise control over gain and phase shift, making it suitable for signal processing applications.

4.9 Experiment Completion Status

I have successfully completed all the sections mentioned in this Experiment

5 Differentiator Circuit using Five-Transistor OTA

5.1 Aim of the Experiment

To design and simulate a Differentiator Circuit using a Five-Transistor Operational Transconductance Amplifier (OTA) in a negative feedback configuration and observe the input-output waveform characteristics.

5.2 Theory

A differentiator circuit produces an output proportional to the rate of change of the input voltage. It is commonly used in signal processing applications such as edge detection, motion sensing, and waveform shaping.

In an operational amplifier-based differentiator, a capacitor is placed in series with the input signal while a resistor provides negative feedback. The Five-Transistor OTA can be configured similarly, where the transconductance of the OTA plays a crucial role in determining the differentiation behavior.

The transfer function of an ideal differentiator is given by:

$$V_{out}(s) = -RC\frac{dV_{in}}{dt} \tag{17}$$

where R is the feedback resistor and C is the input capacitor.

5.3 Circuit Design

The circuit consists of:

- A Five-Transistor OTA configured in a negative feedback loop.
- A capacitor at the input to enable differentiation.
- A triangular wave input to verify the differentiation property.

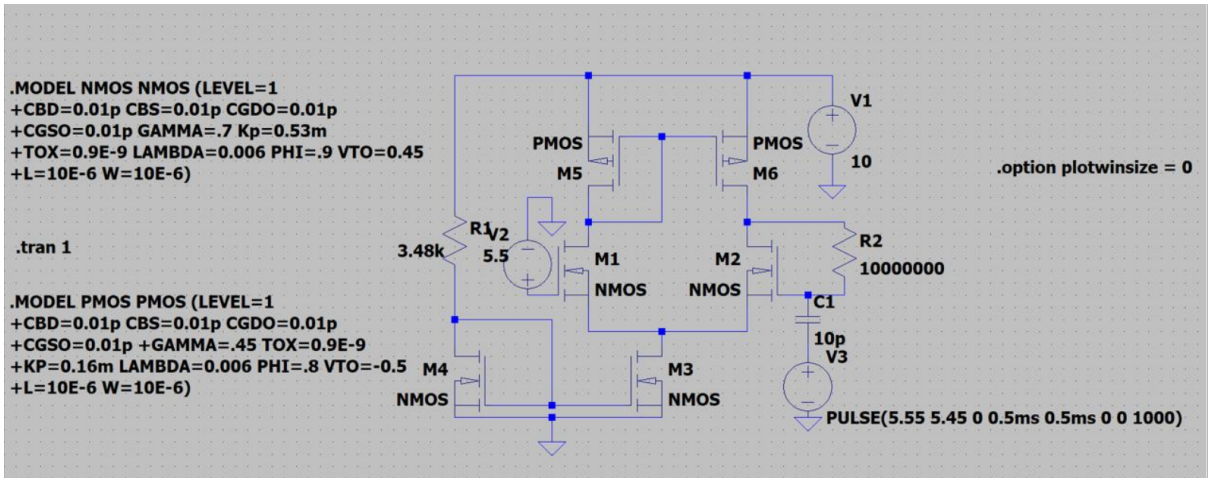
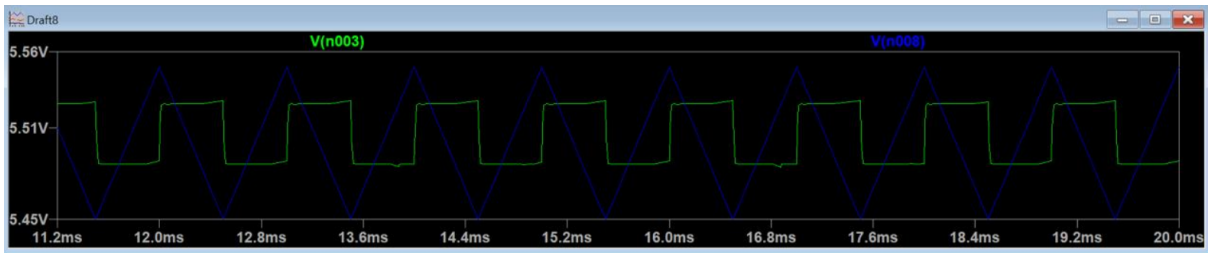


Figure 5: Differentiator Circuit using Five-Transistor OTA

5.4 Simulation Steps

1. Design the differentiator circuit using the Five-Transistor OTA.
2. Apply a triangular waveform input with an amplitude of 100 mVpp and a frequency of 1 kHz.
3. Perform a transient analysis to observe the output response.
4. Plot the input and output waveforms to verify the differentiation behavior.

5.5 Simulation Results



5.6 Key Observations

- The output waveform should be a square wave, as the derivative of a triangular wave is a square wave.
- Any deviation from the expected result may be due to non-idealities such as parasitic capacitances or transistor mismatches.

5.7 Conclusion

The differentiator circuit using the Five-Transistor OTA was successfully designed and simulated. The output was observed to be a square wave, confirming the differentiation property of the circuit. This experiment highlights the utility of OTAs in signal processing applications.

5.8 Inference

From this experiment, it is inferred that:

- OTAs can effectively implement differentiator circuits in analog signal processing.
- The performance of the differentiator is highly dependent on the transconductance of the OTA.
- Proper selection of circuit components is necessary to minimize errors due to non-idealities.

5.9 Experiment Completion Status

I was not able to complete all the sections mentioned in this Experiment during the lab session.