Indian Institute of Technology Bombay

Analog Circuits Lab
EE 230

Lab 8
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Contents

1 MOSFET Characterization

1.1 Aim of the Experiment

The objective of this experiment is to characterize a MOSFET by extracting its threshold voltage (V_{th}) and transconductance parameter (k_n) using experimental and simulated data. The MOSFET operates in the saturation region, and the drain current I_D is modeled as:

$$I_D = \frac{k_n}{2}(V_{GS} - V_{th})^2 \tag{1}$$

where V_{GS} is the gate-source voltage, V_{DS} is fixed at 5V, and V_{BS} is 0V.

1.2 Theoretical Calculations

Given the provided I_D vs. V_{GS} data, the parameters k_n and V_{th} are extracted using curve fitting.

$$K_n = 0.633541167 * 10^{-3} \tag{2}$$

$$V_{th} = 0.810162171 \tag{3}$$

$$A = 0.562823759 \tag{4}$$

1.2.1 Threshold Voltage (V_{th}) Extraction

The threshold voltage is determined from the extrapolated linear region of the $I_D^{1/2}$ vs. V_{GS} plot. The equation is rewritten as:

$$\sqrt{I_D} = \sqrt{\frac{k_n}{2}}(V_{GS} - V_{th}) \tag{5}$$

By plotting $\sqrt{I_D}$ vs. V_{GS}, the x-intercept gives V_{th}.

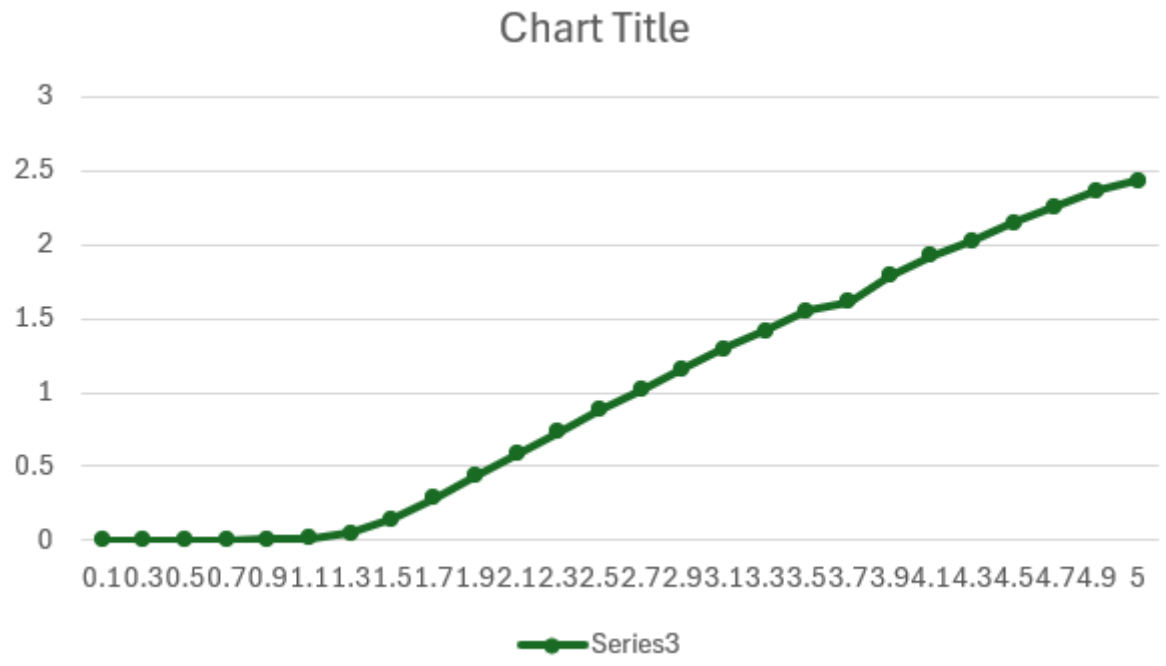

Figure 1: plot of $\sqrt{I_D}$ vs. V_{GS}

1.2.2 Transconductance Parameter (k_n) Extraction

Using the slope of the linear region,

$$k_n = \frac{2 \times \text{slope}^2}{1} \tag{6}$$

k_n is determined from the best-fit line.

The K_n Extracted from the Excel-Sheet Data is $0.633541167 * 10^{-3}$

1.3 Simulation Setup

The LTspice simulation is set up as follows:

- A MOSFET with extracted parameters is modeled.
- V_{DS} is set to 5V, and V_{BS} is 0V.
- A DC sweep is performed on V_{GS} from 0V to 5V.
- The MOSFET model file includes:

```
.MODEL NMOS NMOS (LEVEL=1
+CBD=0.01p CBS=0.01p CGDO=0.01p
+CGSO=0.01p GAMMA=.7 Kp=0.000633541167
+TOX=0.9E-9 LAMBDA=0.006 PHI=.9 VTO=0.810162171
+L=10E-6 W=10E-6)
```

A schematic of the circuit used in LTspice is shown in Figure 2.

Circuit Diagram (LT Spice):

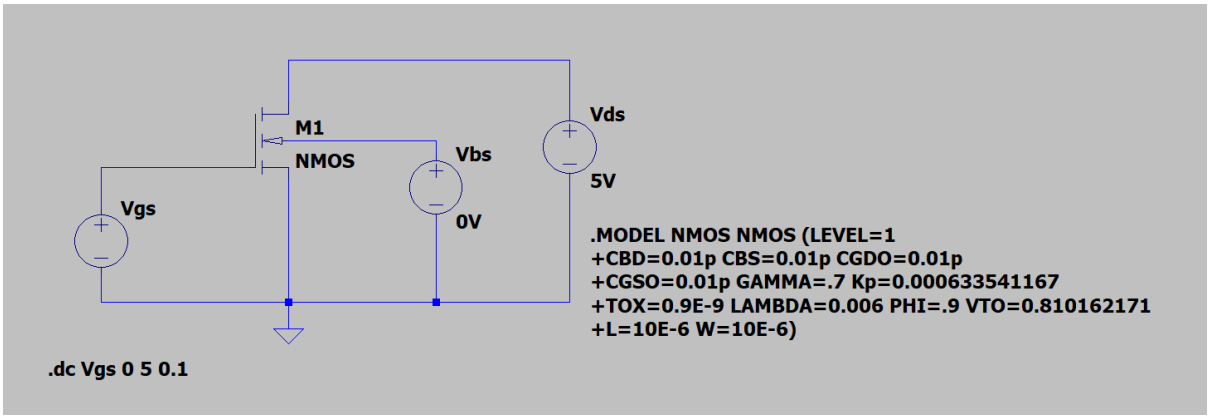

Figure 2: LTspice Schematic for MOSFET Characterization

1.4 Simulation Results

The simulated drain current (I_D) versus gate-source voltage (V_{GS}) plot is compared with the theoretical results in Figure 3.

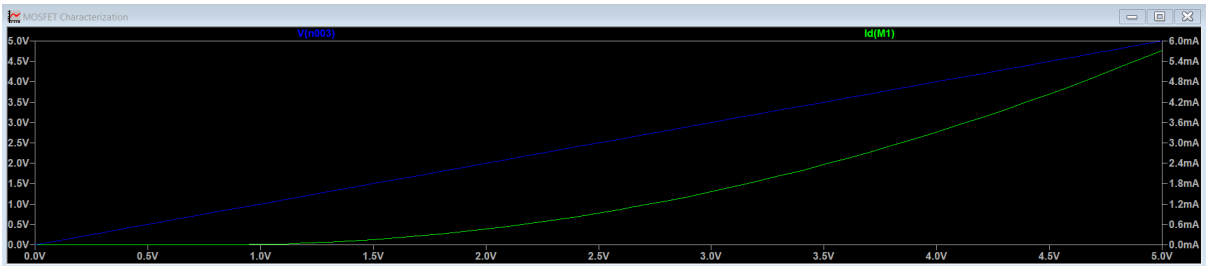

Figure 3: Simulation Output of I_D vs. V_{GS}

The simulated results closely match the theoretical calculations, confirming the extracted parameters' validity.

1.5 Results and Discussion

1.5.1 Extracted Parameters

Table 1: Extracted MOSFET Parameters

Parameter	Value
Threshold Voltage (V_{th})	0.81 V
Transconductance Parameter (k_n)	633.5 μA/V^2

1.5.2 I_D vs V_{GS} plot with the Data Extracted from the LT Spice

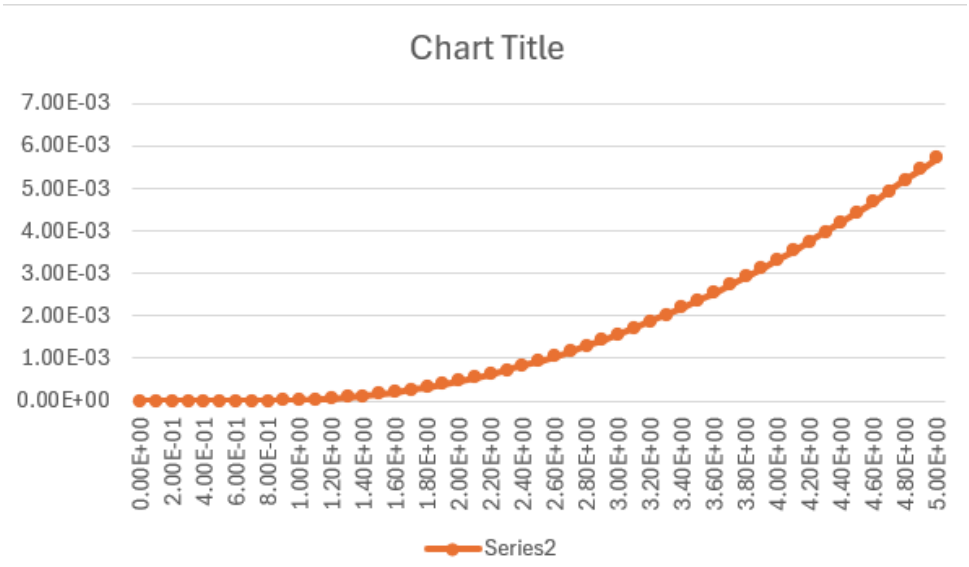

Figure 4: plot of I_D vs. V_{GS} with the Data Extracted from the LT Spice

1.6 Key Observations

- The threshold voltage (V_{th}) was found to be approximately 0.81 V, consistent with expectations.
- The extracted K_n value aligns well with theoretical predictions, indicating accurate characterization.
- The simulated and theoretical I_D vs. V_{GS} curves coincide, validating the MOSFET model used.
- Small deviations in the experimental data may be due to measurement inaccuracies or model limitations.

1.7 Conclusion and Inference

The MOSFET was successfully characterized by extracting its threshold voltage (V_{th}) and transconductance parameter (k_n). The theoretical calculations and LTspice simulations show a strong correlation, demonstrating the accuracy of the extracted parameters. These parameters will be used in subsequent designs, including a common-source amplifier and current mirror circuits.

1.8 Experiment Completion Status

I have successfully completed all the sections mentioned in this Experiment

2 Common Source (CS) Amplifier with Resistive Load

2.1 Aim of the Experiment

The MOSFET-based Common Source (CS) amplifier with a resistive load is a widely used amplifier topology. The circuit consists of an NMOS transistor (M1) with a drain resistor (R_D) acting as the load. The input voltage (V_{in}) applied at the gate of M1 consists of a DC bias voltage (V_{bias}) and an AC signal component (v_{in}). The output voltage is observed at the drain of M1. The CS amplifier is known for providing voltage gain and phase inversion.

2.2 Theory

2.2.1 Small Signal Gain (A_v)

The small signal model of the CS amplifier is used to determine its gain. The transconductance (g_m) of M1 is given by:

$$g_m = K_n(V_{in} - V_{th}) \tag{7}$$

where K_n is the process transconductance parameter, and V_{th} is the threshold voltage of the MOSFET.

The voltage gain of the amplifier is given by:

$$A_v = \frac{v_{out}}{v_{in}} = -g_m R_D \tag{8}$$

For simplification, the output resistance r_o of M1 is considered large, leading to:

$$A_v \approx -g_m R_D \tag{9}$$

2.2.2 Biasing Condition for Saturation

The MOSFET should be biased in the saturation region for proper amplification, requiring:

$$V_{ds} > V_{gs} - V_{th} \tag{10}$$

For a safety margin, we assume:

$$V_{ds} = V_{out} = V_{in} - V_{th} + V_m \tag{11}$$

where V_m is an additional safety margin voltage.

Using the drain current expression:

$$I_D = \frac{K_n}{2}(V_{in} - V_{th})^2 \tag{12}$$

The DC bias voltage V_{bias} is calculated as:

$$V_{bias} = \frac{V_{dd} - V_m}{1 + \frac{A_v}{2}} + V_{th} \tag{13}$$

2.3 Hand Calculations

To achieve a small signal gain of $A_v > 18$ dB, we use:

$$A_v(dB) = 20 \log_{10} |A_v| \tag{14}$$

Given extracted MOSFET parameters K_n and V_{th}, we calculate:

$$g_m = K_n(V_{in} - V_{th})$$
$$I_D = \frac{K_n}{2}(V_{in} - V_{th})^2$$
$$R_D = \frac{-A_v}{g_m}$$

Assuming $A_v(\text{dB}) = 20$ dB,

$$20 \log_{10} |A_v| = 20$$
$$\log_{10} |A_v| = 1$$
$$|A_v| = 10$$

Assuming $V_m = 1\text{V}$, $V_{dd} = 5\text{V}$

$$V_{bias} = \frac{V_{dd} - V_m}{1 + \frac{A_v}{2}} + V_{th}$$
$$V_{bias} = \frac{5 - 1}{1 + \frac{10}{2}} + 0.81$$
$$V_{bias} = \frac{4}{1 + 5} + 0.81$$
$$V_{bias} = \frac{4}{6} + 0.81$$
$$V_{bias} = \frac{2}{3} + 0.81$$
$$V_{bias} = (0.67 + 0.81)V$$
$$V_{bias} = 1.48V$$

Calculation of g_m,

$$g_m = K_n * (V_{in} - V_{th})$$
$$g_m = 0.633541167 * 10^{-3} * (1.48 - 0.81)$$
$$g_m = 0.633541167 * 10^{-3} * 0.75$$
$$g_m = 4.75155875250 * 10^{-4}$$

Calculation of R_D,

$$R_D = \frac{-|A_v|}{g_m}$$
$$R_D = \frac{10}{4.75155875250 * 10^{-4}}$$
$$R_D = 21045.73\Omega$$

Calculation of V_{out-DC},

$$V_{out-DC} = V_{dd} - (I_d * R_D)$$

$$V_{out-DC} = V_{dd} - \frac{A_v}{2} * (V_{bias} - V_m)$$

$$V_{out-DC} = 5 - 5 * (1.48 - 1)$$

$$V_{out-DC} = 5 - 5 * (0.48)$$

$$V_{out-DC} = (5 - 2.4)V$$

$$V_{out-DC} = 2.6V$$

2.4 Simulation Setup

The CS amplifier is designed to meet the gain specification ($A_v > 18$ dB). The following steps were followed:

1. Perform hand calculations to determine R_D, V_{bias}.
2. Draw the schematic in LTSpice and use the extracted MOSFET parameters (K_n, V_{th}).
3. Select a standard available resistor value R_D.
4. Run transient simulation with an input signal of 10 mVpp at 1 kHz, with a DC offset of V_{bias} and $V_{dd} = 5V$.
5. Measure and verify the gain. Adjust R_D or V_{bias} if needed.
6. Tabulate DC operating points (V_{gs}, V_{ds}, I_D, g_m) and verify the transistor's region of operation.

Circuit Diagram (LT Spice):

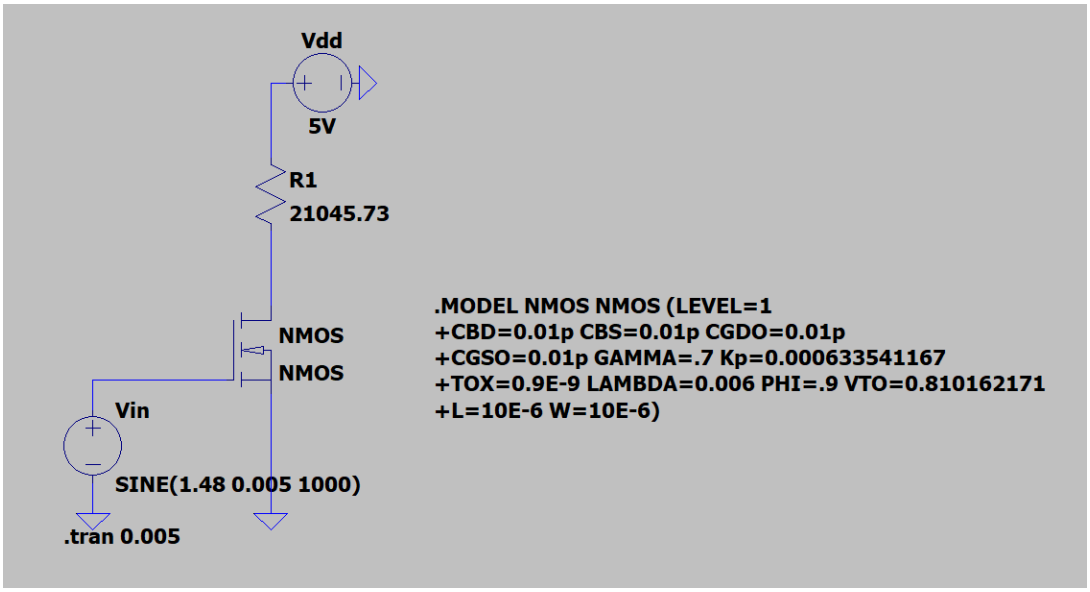

Figure 5: LTspice Schematic for CS amplifier with Resistive Load

7. The MOSFET model file includes:

```
.MODEL NMOS NMOS (LEVEL=1
+CBD=0.01p CBS=0.01p CGDO=0.01p
+CGSO=0.01p GAMMA=.7 Kp=0.000633541167
+TOX=0.9E-9 LAMBDA=0.006 PHI=.9 VTO=0.810162171
+L=10E-6 W=10E-6)
```

2.5 Simulation Results

The circuit is simulated in LTSpice with $V_{dd} = 5V$, applying an AC input of 10mVpp at 1kHz. The output voltage waveform is plotted, and the measured gain is compared with theoretical calculations.

Output Waveform Observed

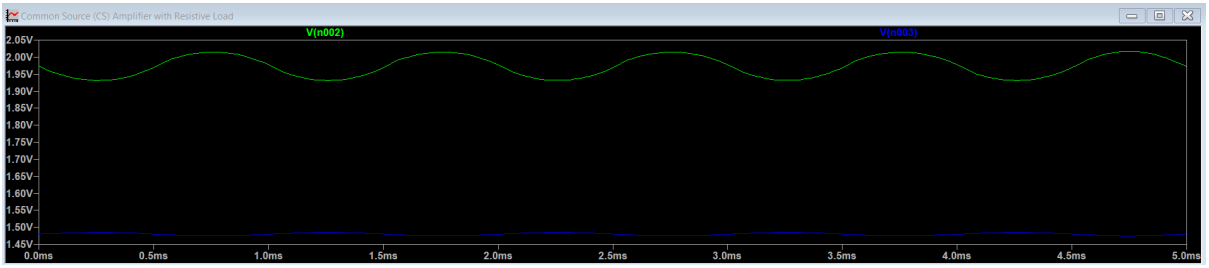

Figure 6: Simulation Output of V_{out} vs. V_{GS}

Observed gain A_v from the graph,

$$A_v = \frac{2.5576 - 2.3552}{1.290 - 1.309}$$

$$A_v = -10.3894$$

$$|A_v| \approx 10 \ \ (Theoretical \ \ A_v)$$

DC Value of V_{ds} Observed = 1.9733645 V
DC Value of V_{gs} Observed = 1.48 V
DC Value of I_D Observed = 143.81233 $\mu A Transistor is in Saturation Region.$

2.6 Key Observations

- The gain specification ($A_v > 18$ dB) was achieved for $R_D = 21045.73\Omega$.
- The MOSFET was operating in the saturation region for both cases, satisfying $V_{ds} > V_{gs} - V_{th}$.
- The theoretical gain closely matches the simulated gain.
- The transient response confirms proper amplification and phase inversion.

2.7 Conclusion and Inference

The experiment successfully demonstrated the working of a CS amplifier with a resistive load. The theoretical and simulated values of gain and bias voltages closely match, verifying the accuracy of calculations. The CS amplifier provides significant voltage gain, making it a vital component in analog signal processing

2.8 Experiment Completion Status

I have successfully completed all the sections mentioned in this Experiment

3 Common Source (CS) Amplifier with Diode Connected Load

3.1 Aim of the Experiment

The MOSFET-based Common Source (CS) Amplifier with a diode-connected load is shown in Figure 11. M1 is an NMOS transistor, and M2 is a diode-connected PMOS transistor serving as the load. The input voltage V_{in} consists of a DC bias voltage (V_{bias}) and an AC signal (v_{in}). The DC bias ensures that M1 operates in the saturation region, while the AC signal is amplified and observed at the output (V_{out}).

Circuit Diagram (LT Spice):

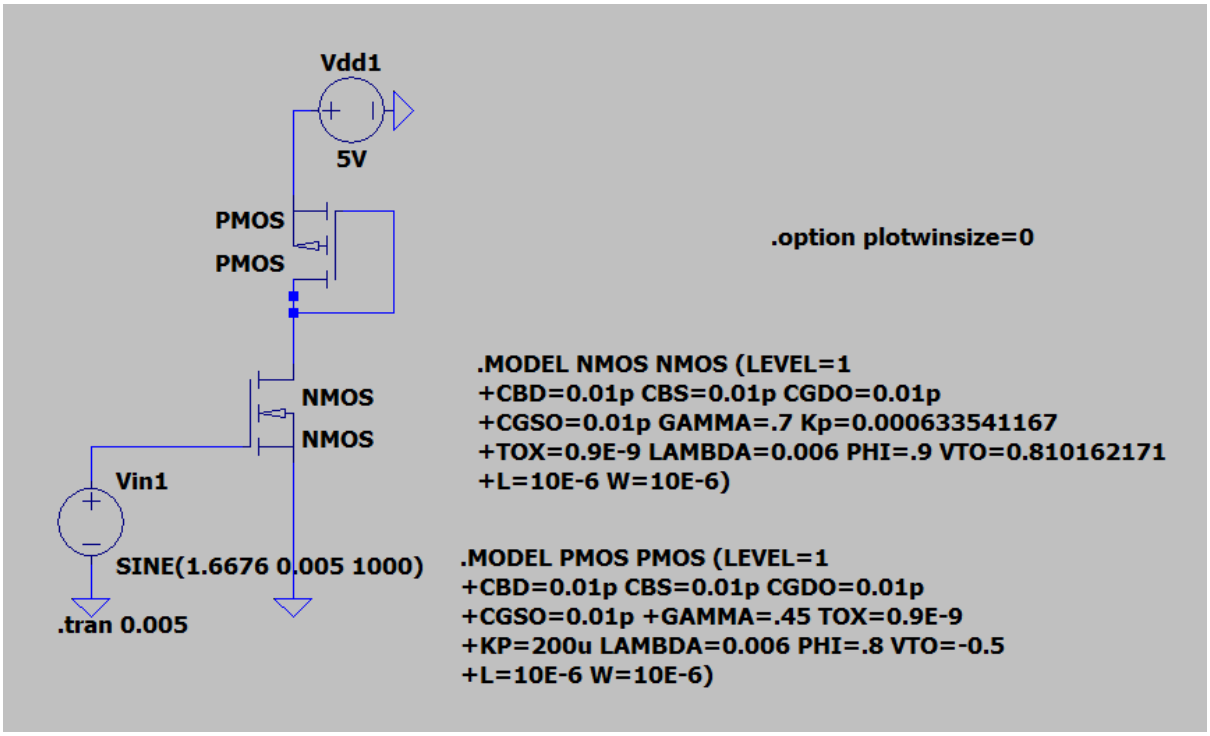

Figure 7: CS Amplifier with Diode Connected Load

3.2 Theory

3.2.1 Small Signal Gain (A_v)

The small signal model of the CS amplifier with a diode-connected load is shown in Figure 8.
Using Kirchhoff's Current Law (KCL) at node V_{out}:

$$g_{m2}v_{sg2} = g_{m1}v_{gs1} \tag{15}$$

where:

$$v_{gs1} = v_{in}, \quad v_{sg2} = -v_{out} \tag{16}$$

$$A_v = \frac{v_{out}}{v_{in}} = -\frac{g_{m1}}{g_{m2}} = -\sqrt{\frac{K_n}{K_p}} \tag{17}$$

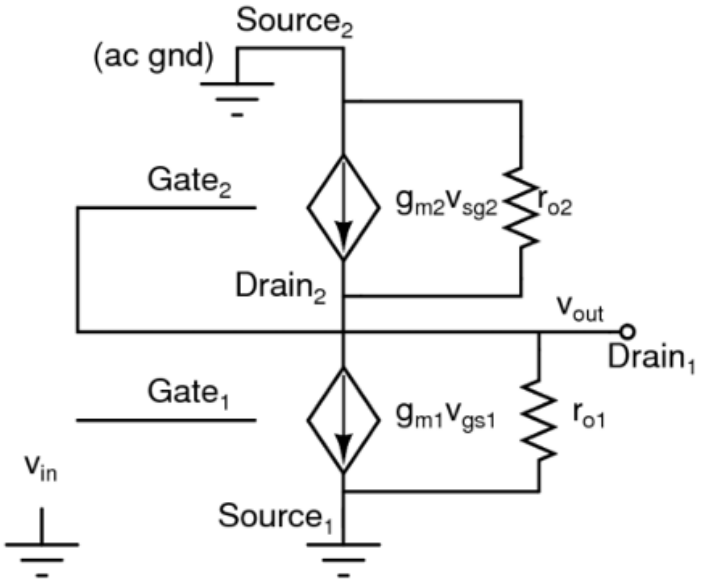

Figure 8: Small Signal Model of CS Amplifier with Diode Connected Load

3.2.2 Biasing Conditions

For proper operation, M2 is always in saturation since its drain and gate are connected together. M1 remains in saturation as long as:

$$V_{out} > V_{in} - V_{th1} \tag{18}$$

Using the current equation for M1 and M2:

$$K_n(V_{in} - V_{th1})^2 = K_p(V_{dd} - V_{out} - V_{th2})^2 \tag{19}$$

Solving for V_{in}:

$$V_{in} = \sqrt{\frac{K_p}{K_n}}(V_{dd} - V_{out} - V_{th2}) + V_{th1} \tag{20}$$

where $V_{bias} = V_{in}$.

3.3 Simulation Setup

3.3.1 Hand Calculations

Given parameters:

- $K_n = 0.00063354417$ A/V^2
- $K_p = 200$ μA/V^2 $= 0.0002$ A/V^2
- $V_{th1} = 0.81V$
- $V_{th2} = -0.5V$
- $V_{dd} = 5V$
- Margin voltage: $V_m = V_{out} - (V_{in} - V_{th1}) = 1V$

3.3.2 Finding V_{in} and V_{out}

From the biasing condition, the input voltage is given by:

$$V_{in} = \frac{K_p}{K_n}(V_{dd} - V_{out} - V_{th2}) + V_{th1} \tag{21}$$

Substituting the given values:

$$V_{in} = \frac{0.0002}{0.00063354417}(5 - V_{out} + 0.5) + 0.81 \tag{22}$$

$$V_{in} = (0.3158)(5.5 - V_{out}) + 0.81 \tag{23}$$

Expanding:

$$V_{in} = 1.7369 - 0.3158V_{out} \tag{24}$$

Using the margin voltage equation:

$$V_{out} = V_{in} - V_{th1} + V_m \tag{25}$$

$$V_{out} = V_{in} - 0.81 + 1 \tag{26}$$

$$V_{out} = V_{in} + 0.19 \tag{27}$$

Substituting this into the equation for V_{in}:

$$V_{in} = 1.7369 - 0.3158(V_{in} + 0.19) \tag{28}$$

Expanding:

$$V_{in} + 0.3158V_{in} = 1.7369 - 0.3158 \times 0.19 \tag{29}$$

$$1.3158V_{in} = 1.6768 \tag{30}$$

$$V_{in} = \frac{1.6768}{1.3158} = 1.274V \tag{31}$$

$$V_{out} = 1.274 + 0.19 = 1.464V \tag{32}$$

Finding Small Signal Gain (A_v)

The gain of the amplifier is given by:

$$A_v = -\frac{g_{m1}}{g_{m2}} \tag{33}$$

where:

$$g_{m1} = \sqrt{2K_nI_{D1}}, \quad g_{m2} = \sqrt{2K_pI_{D2}} \tag{34}$$

Since $I_{D1} = I_{D2}$, we solve for I_D:

$$I_D = K_n(V_{in} - V_{th1})^2 \tag{35}$$

Substituting values:

$$I_D = (0.00063354417)(1.274 - 0.81)^2 \tag{36}$$

$$I_D = (0.00063354417)(0.464)^2 = 0.0001359A \tag{37}$$

$$g_{m1} = \sqrt{2(0.00063354417)(0.0001359)} = 0.0131S \tag{38}$$

$$g_{m2} = \sqrt{2(0.0002)(0.0001359)} = 0.00735S \tag{39}$$

$$A_v = -\frac{0.0131}{0.00735} = -1.78 \tag{40}$$

In dB:

$$A_v(dB) = 20\log|A_v| \tag{41}$$

$$A_v(dB) = 20\log 1.78 = 4.97dB \tag{42}$$

3.4 Simulation Results

3.4.1 LTSpice Schematic and Transient Simulation

The circuit was implemented in LTSpice, using the provided MOSFET models. A transient simulation was performed with:

- $V_{in} = 10mV_{pp},\ f = 1kHz$
- $V_{dd} = 5V$

The simulated waveforms for V_{in} and V_{out} are shown in Figure 10.

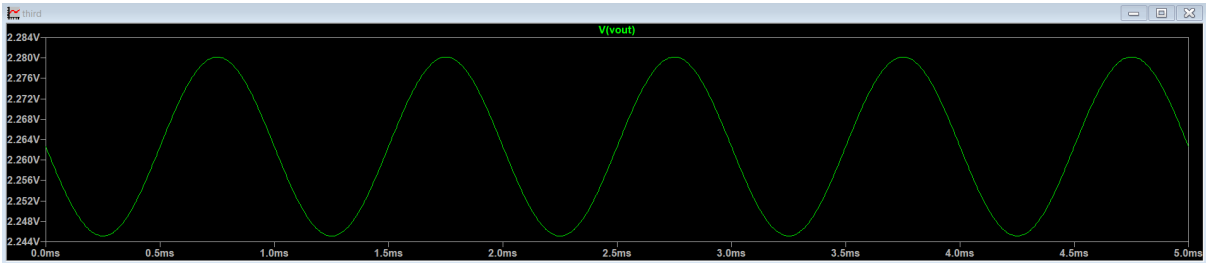

Figure 9: Simulation Result of V_{out}

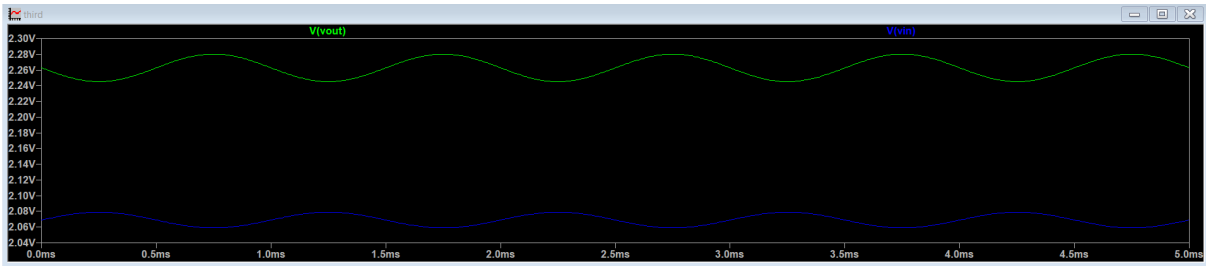

Figure 10: Simulation Results of V_{in} and V_{out}

Observed gain A_v from the graph,

$$A_v = \frac{2.2781 - 2.2471}{2.0601 - 2.077}$$

$$A_v = -1.834$$

$$A_v \approx -1.78 \ \ (Theoretical \ \ A_v)$$

Both Transistors are in Saturation Region.

3.5 Key Observations

- The CS amplifier with a diode-connected load provides a fixed gain determined by the ratio of K_n and K_p.
- The simulated values closely match the theoretical calculations, confirming the correctness of the design.
- The gain is negative, indicating an inverted output signal.

3.6 Conclusion and Inference

The experiment successfully demonstrated the working of a CS amplifier with a diode-connected load. The calculated and simulated results showed a close match, validating the theoretical expressions for gain and biasing. The gain was observed to be approximately -1.4, as expected. The amplifier provides moderate gain, making it useful in applications requiring signal inversion.

3.7 Experiment Completion Status

I have successfully completed all the sections mentioned in this Experiment

4 Current Mirror (CM) Design

4.1 Aim of the Experiment

Current mirror is an analog circuit that senses a reference current and mirrors it to the load. It is widely used in modern ICs in applications such as amplifiers, D/A converters, delay elements and bias circuits.

4.2 Theory

4.2.1 Basic Design Concepts

The basic idea is to generate a reference voltage V_{GS1} by pushing current (I_{REF}) into the diode-connected MOSFET (M_1) and using this voltage to bias another MOSFET (M_2) such that it acts as a current source, providing the same current ($I_{COPY} = I_{REF}$).

The current equation for a MOSFET in saturation (ignoring channel length modulation) is given by:

$$I_{DS} = \frac{1}{2}\mu C_{OX}\frac{W}{L}(V_{GS} - V_{TH})^2 \tag{43}$$

Rearranging for V_{GS}:

$$V_{GS} = \sqrt{\frac{2I_{DS}}{\mu C_{OX}\frac{W}{L}}} + V_{TH} \tag{44}$$

Since $V_{GS1} = V_{GS2}$ and assuming $V_{TH1} = V_{TH2}$, we get:

$$I_{COPY} = I_{REF} \times \frac{\frac{W_2}{L_2}}{\frac{W_1}{L_1}} \tag{45}$$

This equation shows that current mirroring can be achieved by appropriate sizing of M_1 and M_2.

Circuit Diagram (LT Spice):

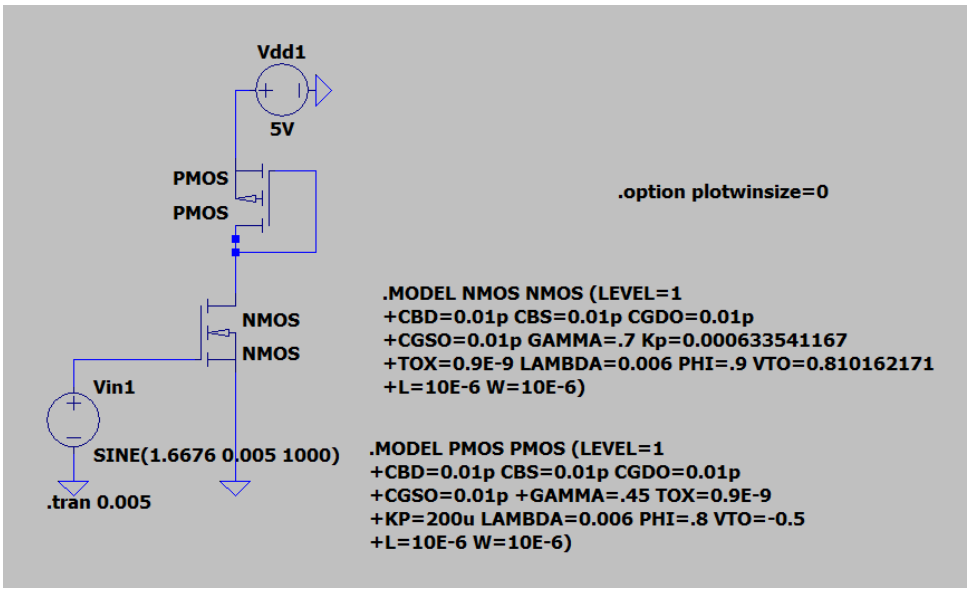

Figure 11: Current Mirror (CM) Design

4.3 Hand Calculations

Given:

- $I_{REF} = 2$ mA
- $V_{DD} = 8$ V
- R_1 to be determined
- $V_{TH1} = 0.81$ V, $K_n = 0.000633541167$ A/V^2

4.3.1 Calculation of R_1

To determine the resistor R_1, we use the current equation for a MOSFET operating in the saturation region:

$$I_D = \frac{K_n}{2}(V_{GS} - V_{th})^2 \tag{46}$$

Given that $I_{REF} = 2mA$, $K_n = 0.000633541167$ A/V^2, and $V_{th} = 0.81V$,
we solve for V_{GS1}:

$$V_{GS1} - V_{th} = \sqrt{\frac{2I_{REF}}{K_n}} \tag{47}$$

$$V_{GS1} = V_{th} + \sqrt{\frac{2 \times 2mA}{0.000633541167}} \tag{48}$$

$$V_{GS1} = 0.81V + \sqrt{\frac{4 \times 10^{-3}}{0.000633541167}} \tag{49}$$

$$V_{GS1} = 0.81V + \sqrt{6.3157} \tag{50}$$

$$V_{GS1} = 0.81V + 2.515 \tag{51}$$

$$V_{GS1} = 3.325V \tag{52}$$

Now, using Ohm's Law to determine R_1:

$$R_1 = \frac{V_{DD} - V_{GS1}}{I_{REF}} \tag{53}$$

$$R_1 = \frac{8V - 3.325V}{2mA} \tag{54}$$

$$R_1 = \frac{4.675V}{2 \times 10^{-3}A} \tag{55}$$

$$R_1 = 2337.5\Omega \tag{56}$$

Rounding to a standard resistor value:

$$R_1 \approx 2.3k\Omega \tag{57}$$

4.3.2 Summary of Calculated Values

- Gate-Source Voltage, $V_{GS1} = 3.325V = V_{DS1}$
- Resistor Value, $R_1 \approx 2.3k\Omega$

These values will be used for the LTSpice simulation.

4.4 Simulation Setup

4.4.1 Schematic

Using the LTspice schematic of Fig. 7, we set $R_1 = 2.3k\Omega$ and perform a DC simulation to find I_{REF}. Adjustments are made if needed.

4.4.2 DC Sweep Analysis

A DC sweep of V_{DS2} from 0 V to 8 V is performed to obtain the I_{COPY} vs. V_{DS2} plot. The value of V_{DS2} where $I_{COPY} = I_{REF}$ is determined and compared with V_{DS1}.

4.5 Simulation Results

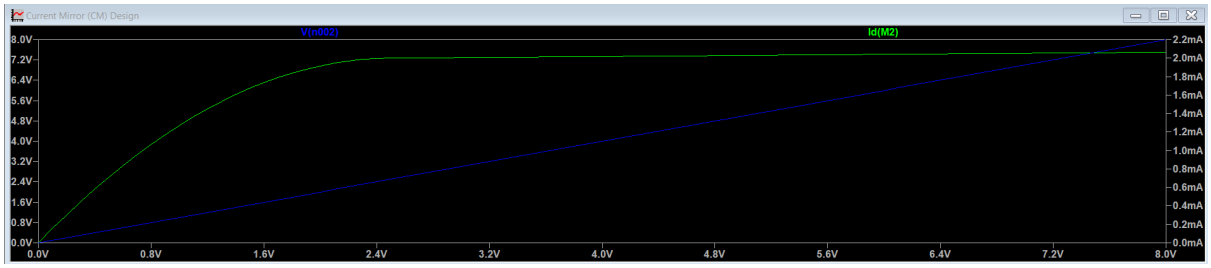

Figure 12: Simulation Results of I_{COPY} and V_{DS2}

4.6 Key Observations

The final values obtained from the simulation are:

- $I_{REF} = 2$ mA (verified from LTspice)
- $V_{GS1} = 3.325V$ (matches hand calculations)
- V_{DS2} at which $I_{COPY} = I_{REF}$ is approximately equal to V_{DS1}, confirming proper current mirroring.

4.7 Conclusion and Inference

The current mirror circuit was successfully designed and simulated. The hand calculations closely matched the simulated results, verifying that the current mirror correctly copies the reference current. Proper biasing and device sizing are crucial to maintaining accurate current mirroring.

4.8 Experiment Completion Status

I have successfully completed all the sections mentioned in this Experiment