Indian Institute of Technology Bombay

Analog Circuits Lab
EE 230

Lab 5
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Contents

1 Log and Anti-log Amplifier Hardware Implementation

1.1 Aim of the experiment

The experiment aims to design and implement an **analog square root computation circuit** using **logarithmic** and **anti-logarithmic amplifiers** based on operational amplifiers (op-amps). This builds upon the simulation performed in **Lab 4**, where the circuit behavior was verified using software tools. In this lab, the focus is on **hardware implementation** using real electronic components.

1. Implement a square root function using **log** and **anti-log amplifiers**.
2. Understand the **role of diodes** in logarithmic and exponential functions.
3. Explore **practical design considerations**, including component selection, diode characteristics, and circuit calibration.
4. Construct and test the circuit on **a breadboard** and verify the results experimentally.

1.2 Procedure Outline

1. **Circuit Development:**
   - Use log-amp and anti-log amp configurations with diodes.
   - Implement a four-block circuit with appropriate feedback resistors.
   - Ensure proper bias voltage selection to eliminate offsets.
2. **Hardware Implementation:**
   - Assemble the circuit on a breadboard using **TL084** op-amp.
   - Use a multi-turn potentiometer for precision in setting bias voltages.
   - Employ Keithley Digital Power Supply for controlled voltage input.
3. **Testing & Analysis:**
   - Sweep V_{in} from 1V to 15V and record V_{out}.
   - Compare experimental results with theoretical calculations.
   - Plot V_{out} vs. V_{in} and $ln(V_{out})$ vs. $ln(V_{in})$ to validate circuit performance.
   - Investigate the effects of diode polarity reversal and other component variations.

1.3 Design of the circuit

The circuit consists of four main blocks, each performing a specific function:

1. **Block 1: Logarithmic Amplifier**
    - Converts the input voltage into a logarithmic form using a diode.
    - Uses an inverting amplifier configuration to generate the log function.
2. **Block 2: Offset Adjustment**
    - Eliminates offset voltage (a_2 term in equations) using a reference voltage V_{b1}.
    - Ensures that only the scaled logarithmic term is passed to the next stage.
3. **Block 3: Scaling and Gain Adjustment**
    - Implements a scaling factor (β) to achieve the required 1/2 exponent.
    - The gain is set to ensure accurate scaling of the logarithmic term.
4. **Block 4: Anti-Logarithmic Amplifier**
    - Converts the scaled log function back into an exponential (anti-log) output.
    - Produces the final output $V_{out} = \sqrt{V_{in}}$ using a second diode.
5. **Additional Design Considerations:**
    - Choice of Diode:
        - Selected based on linearity in $ln(I_D)$ vs. V_D characteristics.
        - Should have minimal variation in saturation current (I_S) and ideality factor (n).
    - Resistor and Bias Voltage Selection:
        - Values of R_3, V_{b1}, and V_{b2} are tuned experimentally to achieve an accurate square-root response.
    - Resistor R_3 acts as a fine adjustment, while V_{b2} provides coarse tuning.

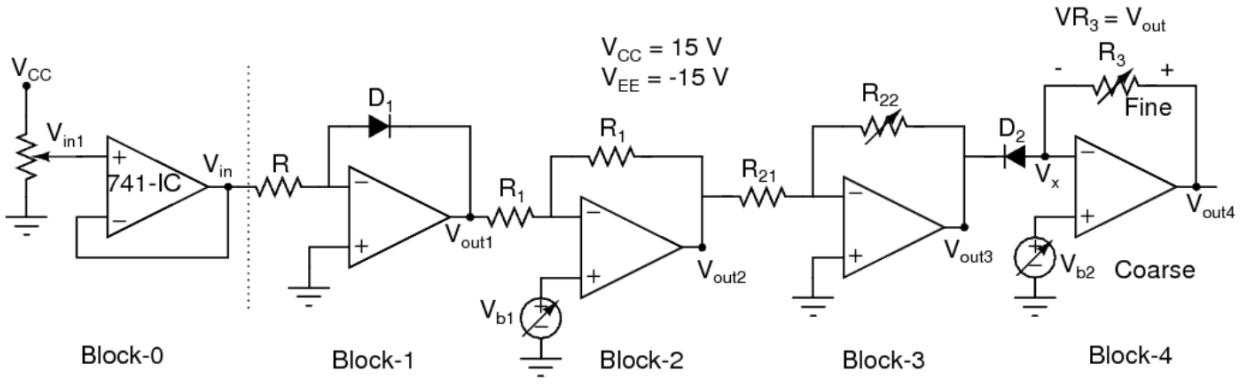

Figure 1: Square-Root Amplifier on Hardware

1.4 Experimental results

Sr. No.	Parameter	Value
1	R_1	10 kΩ
2	V_{b1}	-0.178129838 V
4	R_{21}	10 kΩ
5	R_{22}	Variable
6	V_{b2}	0.56 V
7	R_3	Variable
8	V_{CC}	15 V
9	V_{EE}	-15 V

Table 1: Various circuit parameters

Sr. No.	V_{in}	V_{R_3}
1	9.0 V	2.95 V
2	8.46 V	2.91 V
3	8.34 V	2.85 V
4	8 V	2.82 V
5	7.77 V	2.79 V
6	7 V	2.66 V
7	6.84 V	2.65 V

Table 2: V_{in} and V_{R_3} values

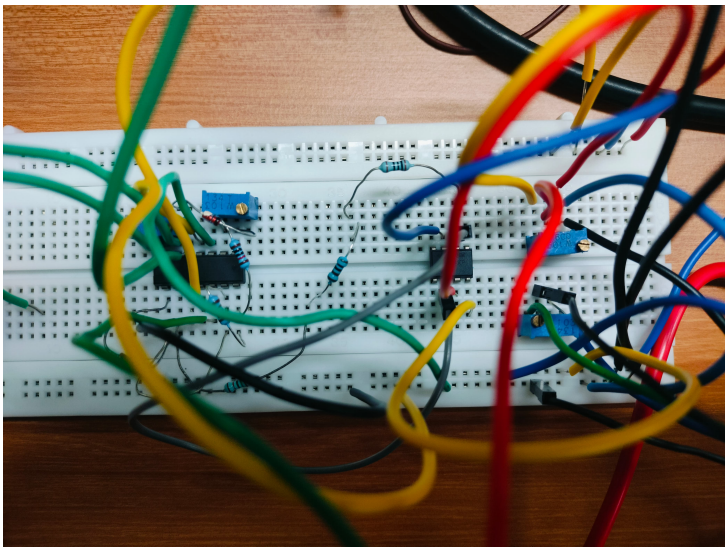

Figure 2: Circuit Diagram

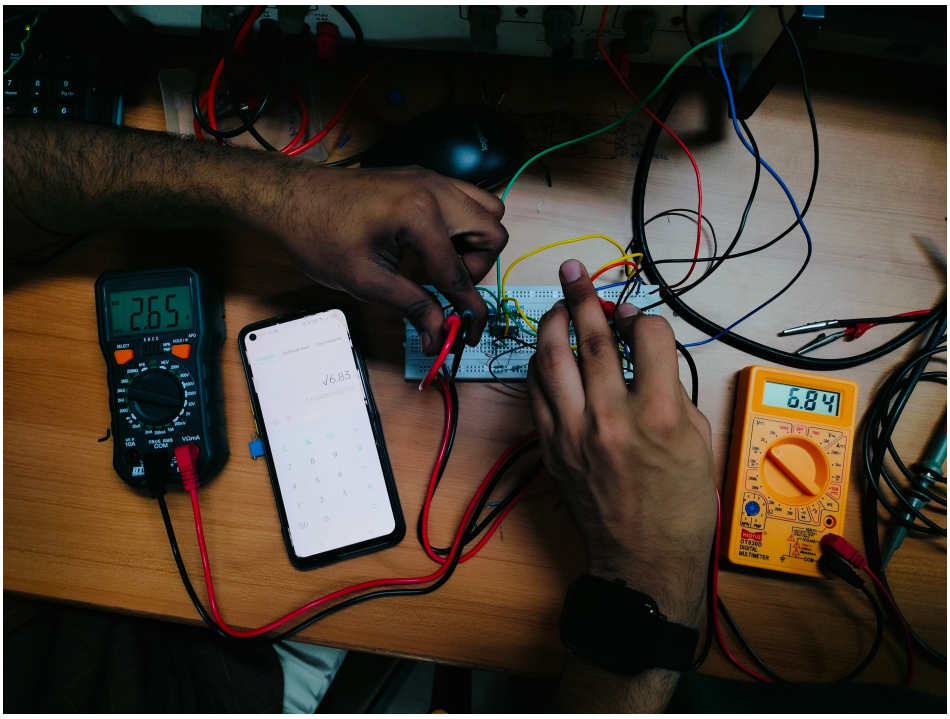

Figure 3: V_{out} at V_{in} of 6.84 V

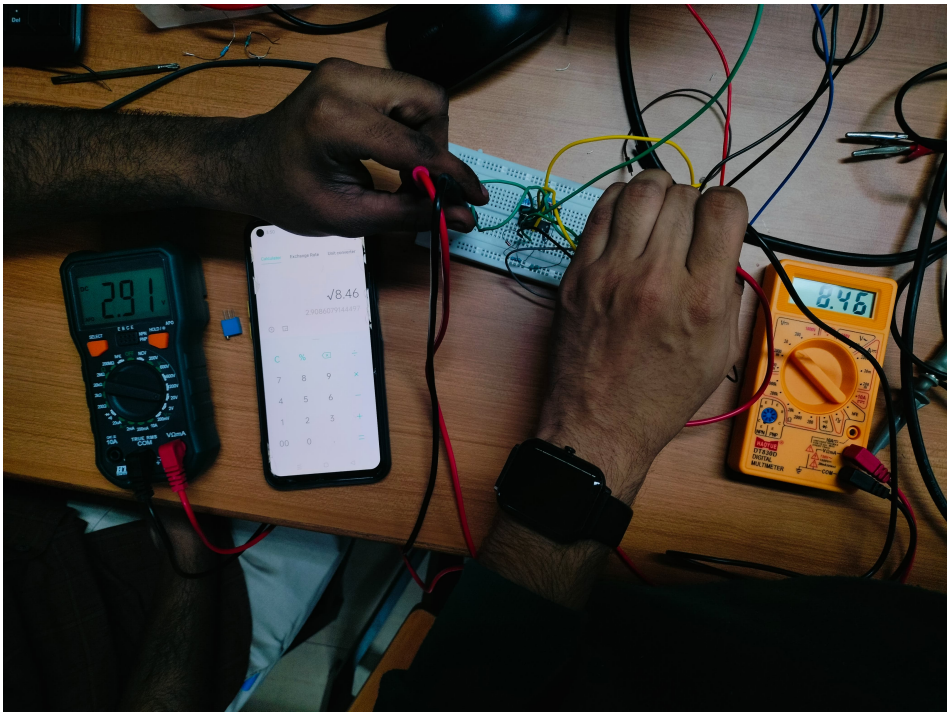

Figure 4: V_{out} at V_{in} of 8.46 V

1.5 Conclusion and Inference

1. **What is the purpose of Block-0?**
   - Block-0 is likely a pre-conditioning stage that ensures a stable and well-defined input voltage before feeding it to the logarithmic amplifier. It could also provide buffering or level shifting.
2. **What if V_{in} is directly connected to V_{in1}?**
   - Directly connecting V_{in} to V_{in1} may bypass necessary impedance matching and cause errors in the log-amp response. The input voltage must be conditioned to ensure proper operation.
3. **Determine the input impedance seen from V_{in1} looking into the inverting terminal of Block-1.**
   - The input impedance is primarily determined by the resistor R used in the inverting amplifier configuration.
   $$Z_{in} = R \tag{1}$$
4. **Derive V_{b1} and V_{b2} DC voltages using a multi-turn potentiometer for better precision.**
   - V_{b1} is set to cancel out the offset (a_2 term in equation 12 in handout).
   - V_{b2} is adjusted to ensure correct scaling in the anti-log amplifier.
5. **Tuning procedure for V_{b1}, V_{b2}, Block-3 Gain, and Resistor R_3:**
   - Set V_{b1} by applying $V_{in} = 1$ V and adjusting until the offset is removed.
   - Adjust V_{b2} and R_3 so that the voltage across R_3 matches the square root function.
   - Set the gain of Block-3 to ensure that $b_2 = 1/2$, maintaining the square root operation.
6. **Tabulate the values of V_{b1} and V_{b2}.**
   - Already done in the previous section.
7. **Why does the potentiometer in Block-4 act as a coarse adjustment, while R_3 is a fine adjustment?**
   - The potentiometer at the non-inverting terminal affects the overall offset, while R_3 fine-tunes the gain.
   - Mathematically:
   $$V_{out} = R_3 I_{D2} + V_{b2} \tag{2}$$
   - V_{b2} affects the overall level (coarse adjustment).
   - R_3 determines the sensitivity of the response (fine adjustment).
8. **Tabulate V_{in} vs. V_{out} readings.**

- Already done in the last section.

9. **Plot V_{out} vs. V_{in} for simulation, experimental, and theoretical results.**
    - Theoretical: Straight line (ideal behavior).
    - Experimental: Open circles (measured data).
    - Simulation: Cross symbols (SPICE results).
10. **Plot $ln(V_{out})$ vs. $ln(V_{in})$ for simulation, experimental, and theoretical results.**
    - Ideal slope = 1/2.
11. **What should be the expected slope of $ln(V_{out})$ vs. $ln(V_{in})$ plot?**
    - Expected slope = 1/2.
12. **What happens if the polarity of diode D_2 is reversed?**
    - The anti-log function will fail because the current flow direction is incorrect.
    - The exponential response will no longer be valid, causing an incorrect output.

This lab involves practical implementation of a square root amplifier using log and anti-log circuits with op-amps. The experiment builds upon previous simulations (Lab 4) and focuses on tuning the circuit for real-world accuracy. The results will be verified using both experimental and theoretical analysis, emphasizing circuit calibration and diode behavior.

1.6 Experiment completion status

The complete experiment was performed in front of the TA in the lab itself.