EE 230 - Analog Lab
Wadhwani Electronics Laboratory
Electrical Engineering IIT Bombay

Lab:4

Instructions:

- Write down all your observations in notebook.
- Verify your calculations with your respective TA.

Objectives:

- Familiarizing with Log and Antilog amplifier.

Contents

1 Introduction

- **logarithmic amplifier**:
  A logarithmic amplifier (log-amp) gives an output that is the logarithm of the input. The base can be any value of choice. Applications of logarithmic amplifiers include direct analog conversion of values in decibels. For example, the acoustic noise levels are expressed in decibels. Logarithmic amplifiers are also used for extending the dynamic range of circuits.
- **Anti-logarithmic amplifier**:
  Anti-logarithmic amplifier (Anti-log-amp) gives an output that is the anti-log of the input. Applications of Anti-logarithmic amplifiers include signal compression and process control. Anti-Log amplifiers with log-amplifiers can be used to realize analog multiplier, square root amplifier, cube root amplifier, etc.

You have already worked with several op-amp based analog circuits. One common feature of many of these circuits is that the output versus input relationships are governed mainly by the external components connected to the op-amp. Taking this as a lead, for implementation of square-root amplifier we require a component, the terminal characteristics of which include a logarithmic or exponential function. A pn junction diode is such a device. We will use a diode and op-amps, and other components to design and simulate a square-root amplifier. The square-root amplifier in the design presented in subsequent sections would give as output the square-root of the input.

2 Basic Design Concepts

The basic principle idea behind designing square root amplifier is to take logarithm of the input, $\ln(V_{in})$ next scale it by half($\frac{ln(V_{in})}{2}$) and then take its anti-log to get $e^{\frac{ln(V_{in})}{2}} = Vin^{1/2}$.

The equation for the terminal characteristics of a pn junction diode in forward bias is

$$I_D = I_S * (e^{V_D/nV_T} - 1) \tag{1}$$

where, I_D is the current through the diode, V_D is the voltage across the diode, I_S is the reverse saturation current, n is the ideality factor of the diode, and V_T is the thermal voltage given by kT/q , where k is the Boltzmann constant, T is the temperature in Kelvin, and q is the elementary charge. We will assume for the time being that I_S and n are constants. The value of V_T at 27°C or 300 K, as you may verify, is 0.026 V. When $V_D >> n * V_T$, say $V_D > n * 100mV$, we may approximate equation (1) as

$$I_D = I_S * e^{V_D/nV_T} \tag{2}$$

and

$$V_D = nV_T * (\ln(I_D) - \ln(I_S)) \tag{3}$$

Equation (3) can be rewritten as

$$\ln(I_D) = V_D/nV_T + \ln(I_S) \tag{4}$$

Equation (2) and (3) suggests that an anti-log and log-amp may be realised by forcing a forward voltage across the pn junction diode and a forward bias current through a pn junction diode, respectively. However the diode voltage would not be true natural logarithm of the input current and diode current would not be a true anti-logarithm of the input voltage. It would contain an offset and also a multiplying factor. Moreover we may want to give a voltage input to the amplifier.

3 Development of the Circuit

A voltage can be easily converted to a current using the inverting amplifier configuration. You may please draw the circuit in your note book. The voltage applied to the input resistor is converted to a current, $I = V_{in}/R$, where R is the input resistor connected to the inverting terminal of the amplifier. The same current I is then forced through the device connected between the output of the op-amp and the inverting terminal. The device can as well be a diode. The circuit is given in figure 1.

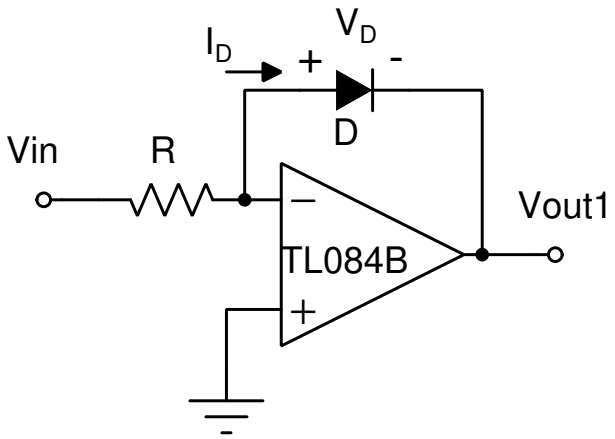

Figure 1: Basic log-amp circuit. For this circuit to function as a log-amp, the polarity of the input voltage should be positive.

From figure 1,

$$I_D = V_{in}/R \tag{5}$$

$$V_{out1} = -V_D \tag{6}$$

Substituting equation (5) in equation (3), and rearranging,

$$V_{out1} = nV_T * (\ln(I_S R) - \ln(V_{in})) \tag{7}$$

Equation (7) can be written in the following form.

$$V_{out1} = -a_1 \ln(V_{in}) + a_2 \tag{8}$$

where,

$$a_1 = n_1 V_T \tag{9}$$

$$a_2 = n_1 V_T \ln(I_S R) \tag{10}$$

Equation (8) tells us that the output of the circuit in figure 1 is the natural logarithm of the input scaled by a factor a_1 and then offset by a_2. We can remove the offset by subtracting a_2 from V_{out1}. The Block-2 is used for removing the offset from V_{out1} as shown in figure 2.

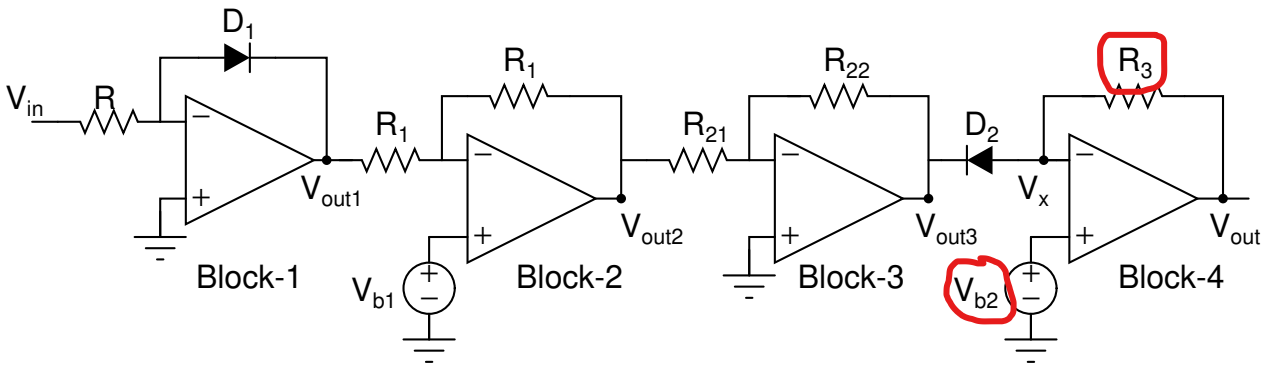

Figure 2: Complete Analog Square-root Circuit.

$$V_{out2} = -V_{out1} + 2V_{b1} \tag{11}$$

$$= a_1 \ln(V_{in}) - a_2 + 2V_{b1} \tag{12}$$

set $V_{b1} = a_2/2$ in equation (12). So the input to Block-3 would be $a_1 \ln(V_{in})$.

$$V_{out3} = -a_1 \beta \ln(V_{in}) = \ln(V_{in})^{-a_1 \beta} \tag{13}$$

In equation (13) β is the magnitude of the gain Block-3 which is $\frac{\mathbf{R_{22}}}{\mathbf{R_{21}}}$. The output V_{out3} is applied to Block-4 which is an Antilog Amplifier. With virtual ground concept $V_x = V_{b2}$, thus the voltage across diode would be $V_{D2} = V_{b2} - V_{out3}$. The current through the diode can be calculated by substituting V_{D2} in equation (2). The current I_{D2} flowing through diode D_2 will also flow through resistor R_3 then V_{out} will be

$$V_{out} = R_3 I_{D2} + V_{b2} \tag{14}$$

$$= R_3 I_{S2} e^{\frac{V_{b2} - V_{out3}}{n_2 V_T}} + V_{b2} \tag{15}$$

If you substitute the V_{out3} from equation (13) and a_1 in equation (15) then the final V_{out} will be

$$V_{out} = R_3 I_{S2} e^{\frac{V_{b2}}{n_2 V_T}} V_{in}^{\frac{n_1}{n_2}\beta} + V_{b2} \tag{16}$$

The voltage across resistor R_3 would be

$$V_{R3} = V_{out} - V_x = R_3 I_{S2} e^{\frac{V_{b2}}{n_2 V_T}} V_{in}^{\frac{n_1}{n_2}\beta} \tag{17}$$

$$V_{R3} = b_1 V_{in}^{b_2} \tag{18}$$

where,

$$b_1 = R_3 I_{S2} e^{\frac{V_{b2}}{n_2 V_T}} \tag{19}$$

$$b_2 = \frac{n_1}{n_2}\beta \tag{20}$$

Choosing $b_1 = 1$, $b_2 = \frac{1}{2}$ and substituting in equation (18), then V_{R3} would be

$$V_{R3} = V_{in}^{\frac{1}{2}} \tag{21}$$

Voltage across the resistor R_3 is our final output which is the square root of the input voltage.

4 Practical Design Considerations

4.1 Diode Specific Considerations

In section 2, the diode was assumed to be ideal, in the sense that the current through the diode would exponentially increase with the voltage across the diode. We also assumed that the ideality factor, n and the saturation current, I_S are constants. Figure 3 shows the measured current - voltage characteristics of 4 different models of silicon diodes. Please note that $\ln(I_D)$ is plotted as a function of voltage across the diode.

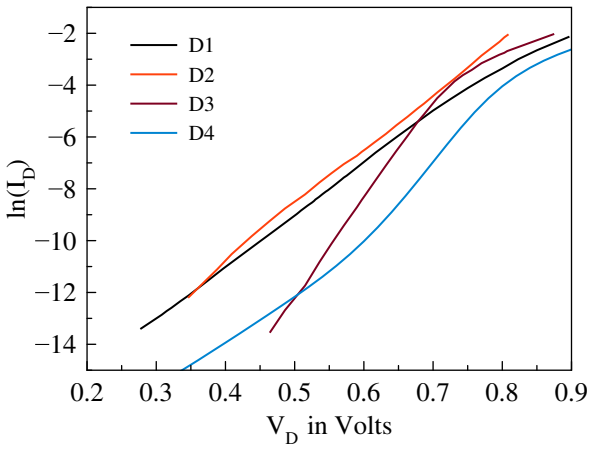

Figure 3: Comparison of the measured current - voltage characteristics of 4 different models of diodes.

The following observations can be made from figure 3.

1. As per equation (4) which is the basis for the design of the square root amplifier, $\ln(I_D)$ versus V_D should be a straight line, if n and I_S are constants. In case of D1, D2 and D3, this is true only over limited ranges of currents. These diodes can be used for making log-amps only over those specific ranges of currents. In case of D4, there seems to be multiple linear segments, each segment with much smaller current ranges than in the case of other diodes. We will not consider diodes like D4 for realisation of log-amps. In fact this diode can be modelled using what is called a 2-diode model. We will not elaborate further on this.

2. By comparing D1 and D3, for current range over which $\ln(I_D)$ versus V_D is linear, you may note that the slopes $(1/nV_T)$ as per equation (4) are not identical. Since V_T is a constant at a given temperature, we may conclude that the ideality factor, n, is different for D1 and D3. The slopes look similar for D1 and D2, indicating that the ideality factors for these two models of diodes are close.

3. The y-intercept of $\ln(I_D)$ versus V_D is $\ln(I_S)$. Hence the saturation current can be estimated from the y-intercept. The saturation currents for different diode models are different.

4. From the above discussion, it is clear that the square root amplifier design is specific to the model of diode used in the circuit. A circuit designed for D1 would not work with D3, for example.

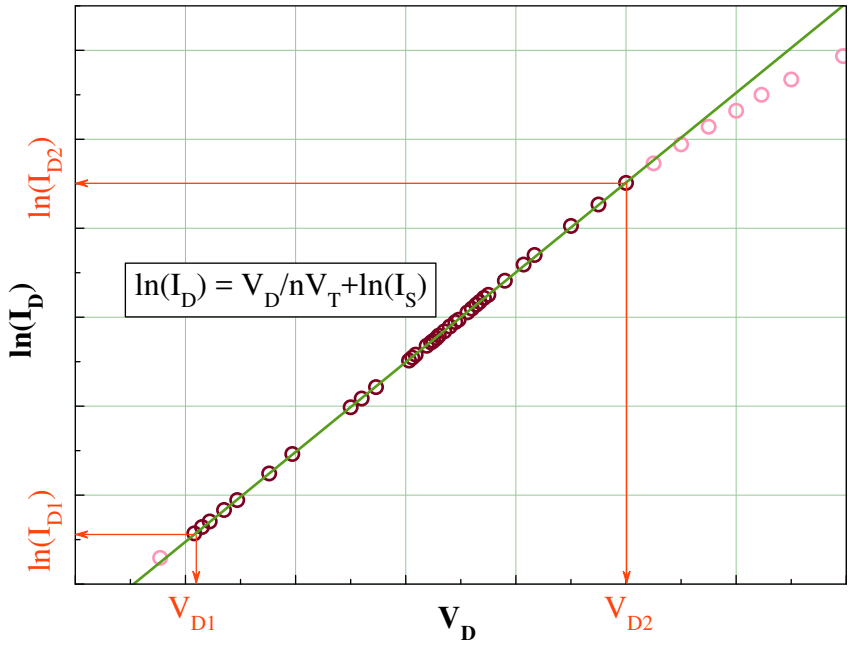

Figure 4: Current - voltage characteristics of a specific model of diode. The open symbols represent the actual measured data. The straight line represent a linear fit to $\ln(I_D)$ versus V_D data. Equation (4) is valid only over the current range I_{D1} to I_{D2}.

4.2 Selecting the Input Voltage Range

The $\ln(I_D)$ versus V_D plot for one specific model of diode is shown in figure 4. The open symbols represent the actual measured data. A straight line is fitted to a range of $\ln(I_D)$ highlighted in the figure in maroon colour. The corresponding range of current is I_{D1} to I_{D2}. Using equation (5), the range of input voltage would be from $V_{in1} = I_{D1}/R$ to $V_{in2} = I_{D2}/R$.

If we assume that the maximum input voltage, $V_{in2} = 15V$, then $R = 15/I_{D2}$. Using equation (5), we can also write, $V_{in1} = V_{in2} * I_{D1}/I_{D2}$.

4.3 Extraction of Diode Model Parameters

The diode saturation current, I_S can be calculated from the y-intercept of the linear fit shown in figure 4. Ideality factor, n, can be calculated from the slope of the linear fit shown in figure 4. The SPICE model for the diode can be specified using these parameters as,

.model diode1 D(Is = ? N = ?)

"Is" in the above statement is the saturation current and N is the ideality factor. "?" should be replaced with the values of these parameters estimated from the fitting exercise.

4.4 Choice of Op-Amp

Operational amplifiers require input DC bias currents flowing into the inverting and non-inverting terminals. The input bias current should be much less than I_{D1} for the log-amp to work to specification in the low input voltage range. For example, the input bias current of 741 can be upto 0.5 μA. If $I_{D1} < 5\mu$A, 741 is not a good choice. A precision op-amp with low input bias currents would be a better choice. You may consider TL084 for this experiment.

5 Simulation

After carefully reading this document you are expected to conduct the simulation. You would be provided the measured I_D versus V_D data for two diodes suitable for square root amplifier implementation. The simulation would involve the following steps, which should be executed and should be carefully documented.

1. You would be provided a text file containing the measured current - voltage characteristics of two diodes suitable for implementing square root amplifier. Plot $\ln(I_D)$ versus V_D. Use open markers (no line) as

shown in figure 4 for plotting the experimental data. You can use any plotting tool you are comfortable with.

2. In the above plot, manually identify the range over which $\ln(I_D)$ is a linear function of V_D. This can be done by manually drawing a line passing through the linear segment of the plot identified by visual inspection. Determine the linear fit using two sufficiently far spaced data points falling on the manually drawn straight line. Calculate I_S and n. (Recommendation: If you know how to use the curve fitting functions of the plotting software you are using, use it.)

3. Create a SPICE model file for both the diodes. Specify I_S and n for the diodes as calculated above.

4. Determine the range of diode currents over which the $\ln(I_D)$ vs V_D is linear. Select one of the diode to be used in Block-1. Determine the value of R as described in section 4.2.

5. Write down the expression for V_{out1}.

6. Determine the values of V_{b1} to remove the offset from V_{out2}. The Resistor R_1 can be chosen arbitrarily. You may choose R_1 between 1k-10k. The systematic approach to eliminate offset is to set input voltage V_{in} =1V to get rid of a_1(since $\ln(Vin) = 0$) so that a_2 can be eleminated by varying V_{b1} easily.

7. When we apply input signal as 1 V then from equation (17), the voltage $V_{R3} = R_3 I_{S2} e^{\frac{V_{b2}}{n_2 V_T}}$ should be made equal to 1 V. So the next task is to set the $R_3 I_{S2} e^{\frac{V_{b2}}{n_2 V_T}} = 1$. We have two variables V_{b2} and R_3 for attaining $V_{R3} = 1V$. You have to adjust these two variables such that the voltage across diode D_2 lies in the linear region ($\ln(I_D)$ vs V_D should be a straight line) and $b_1 = 1$.

8. After that you have to adjust b_2 by varying the gain of Block-3 such that you get V_{R3} to be 3 V when you apply input voltage 9 V.

9. Verify and fine tune the design using SPICE simulations. Create a plot containing the ideal expected $\ln(V_{out})$ versus $\ln(V_{in})$ (a line plot is recommended), and the data obtained from SPICE simulations (a scatter plot with open markers is recommended). The ideal expected plot would be a straight line passing through zero and would have slope of 1. Any deviation of the results of simulation (easily identified if the plots are made as recommended) calls for fine tuning of the design.