EE309(S2): Microprocessors

Spring 2025

[Week #1 Slides]

Instructor: Shalabh Gupta

Course Logistics

Prerequisites: Digital Systems + Lab (EE 214, 224)

Text books: None

Reference material:

- Datasheets etc. will be provided
- R. S. Gaonkar, Microprocessor Architecture: Programming and Applications with the 8085/8080A, Penram International Publishing, 1996
- John L. Hennessy and David A. Patterson, Computer Architecture: A Quantitative Approach (The Morgan Kaufmann Series in Computer Architecture and Design), December 2017
- Douglas Hall, Microprocessors Interfacing, Tata McGraw Hill, 1991.
- Kenneth J. Ayala, The 8051 Microcontroller, Penram International Publishing, 1996
- Wikipedia / Internet

Grading policy

Quizzes: 30% (weekly on Monday mornings, best *n-1* of *n* quizzes)

Missed quiz policy: Prorated only if missed due to medical situation (with IITB doctor's endorsement)

Mid-Sem: 30% (topics covered until mid-sem)

End-Sem: 40% (entire syllabus)

Quizzes will have short objective type questions.

Please install SAFE App for the quizzes and attendance.

Minimum attendance required to avoid the DX grade: 85%

Contact Details

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Please include "EE309" in subject line in ALL communication for this course

TAs: The names of TAs with their roles will be announced

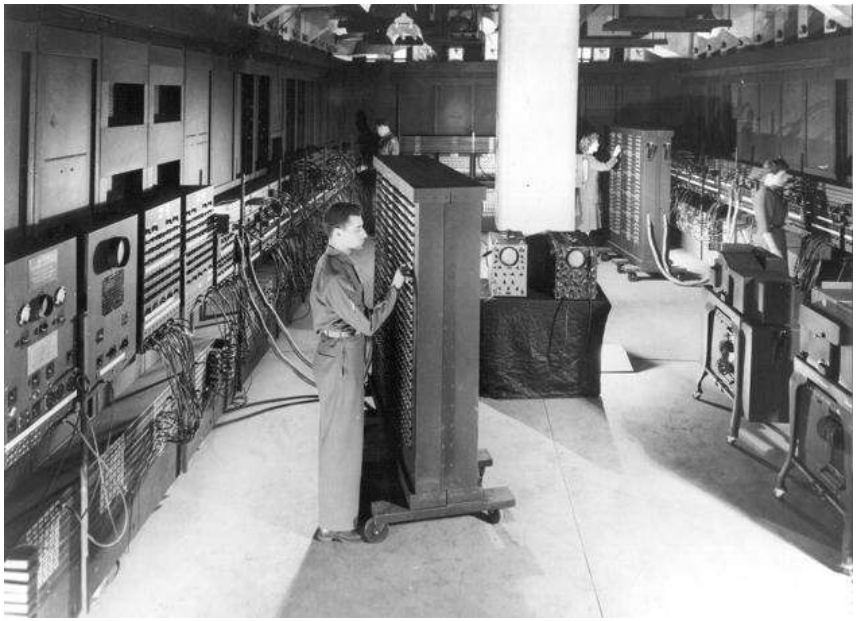
Course Contents

1. Block diagram view of a general purpose processor
2. Elements of hardware and software architectures
3. Introduction to concepts of data and control paths, registers and memory organization.
4. Instruction set basics and assembly language programming.
5. Instruction structure and addressing modes, instruction encoding, and study of 8085A instruction set, hardware architecture and interrupts.
6. Introduction to microcontrollers
7. 8051 hardware and instruction set architecture
8. Timers/counters, interrupts
9. Serial interface (including multi-processor communication).
10. Interfacing basics using examples of I/O devices: parallel port, serial ports, keypad, display, etc.
11. Introductory discussion on processor performance evaluation and design using a RISC ISA
12. Concepts of pipelining, pipelining hazards, cache, virtual memory and parallelism.

ENIAC: Electronic Numerical Integrator and Computer

The first general purpose digital computer

- **Vacuum Tubes**: ENIAC utilized approximately 18,000 vacuum tubes as primary electronic switching elements.
- **Memory**: Memory comprised of mercury delay lines, could hold up to 20 ten-digit decimal numbers at once temporarily
- **Input and Output**: Punched cards
- **Modular Design**: A large, modular computer, composed of individual panels -- 20 of these modules could add, subtract but hold ten-digit decimal numbers in memory.
- **Size and Power**: Spanned approximately 1,800 square feet and consumed around 150 kilowatts of power.
- **Computational Power**: 5000 additions per second



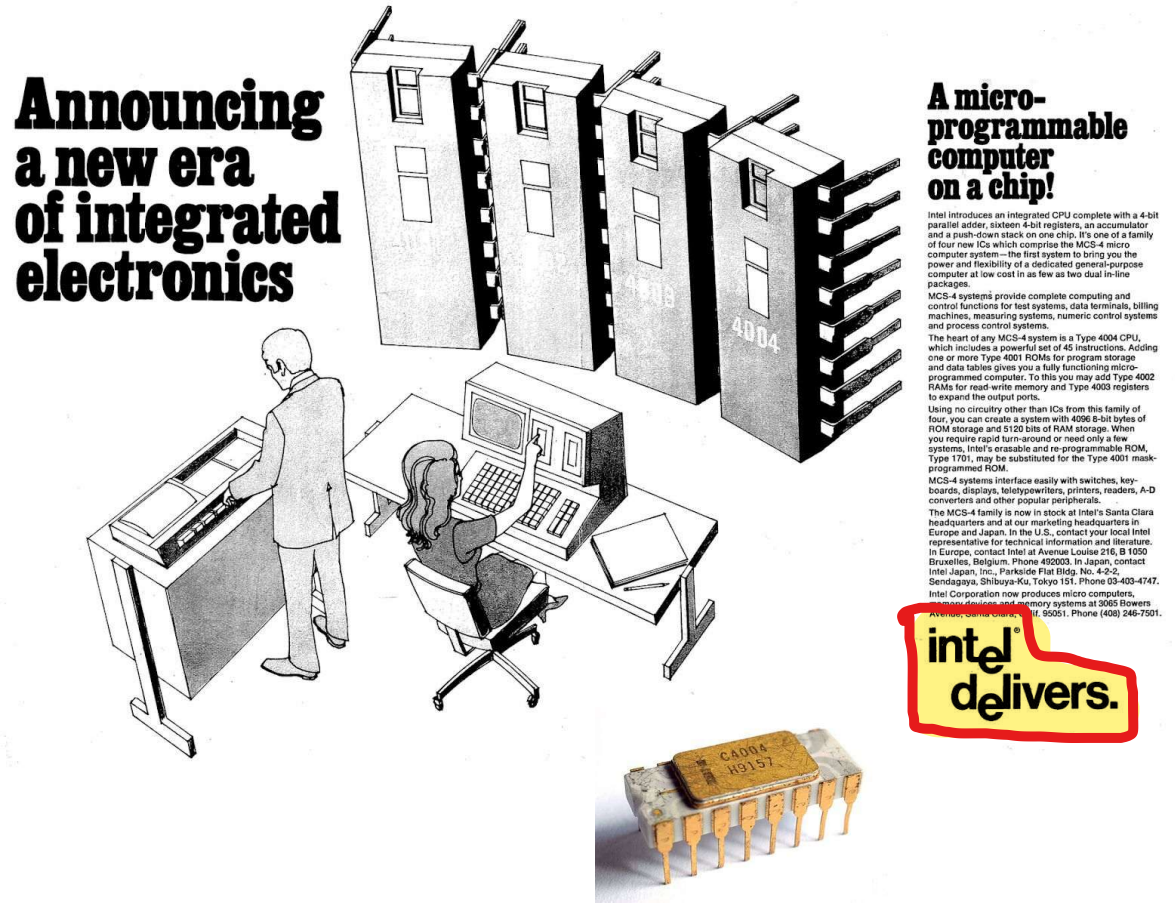
ENIAC [Cost: $500K (~$7M of today)]

Today's Processors/GPUs: ~100 Tera-FLOPS (10^{14} floating point operations/sec)

Power: ~500W; Cost: ~$30K

Reduction in Energy / FLOP: $3x10^{13}$ [Assuming one FLOP = 5 10-digit decimal add

4004: First Commercial Microprocessor



Data width refers to the size of data, in bytes, that can be stored or processed at once. It can also refer to the number of data lines used in parallel transmission.

Salient features:

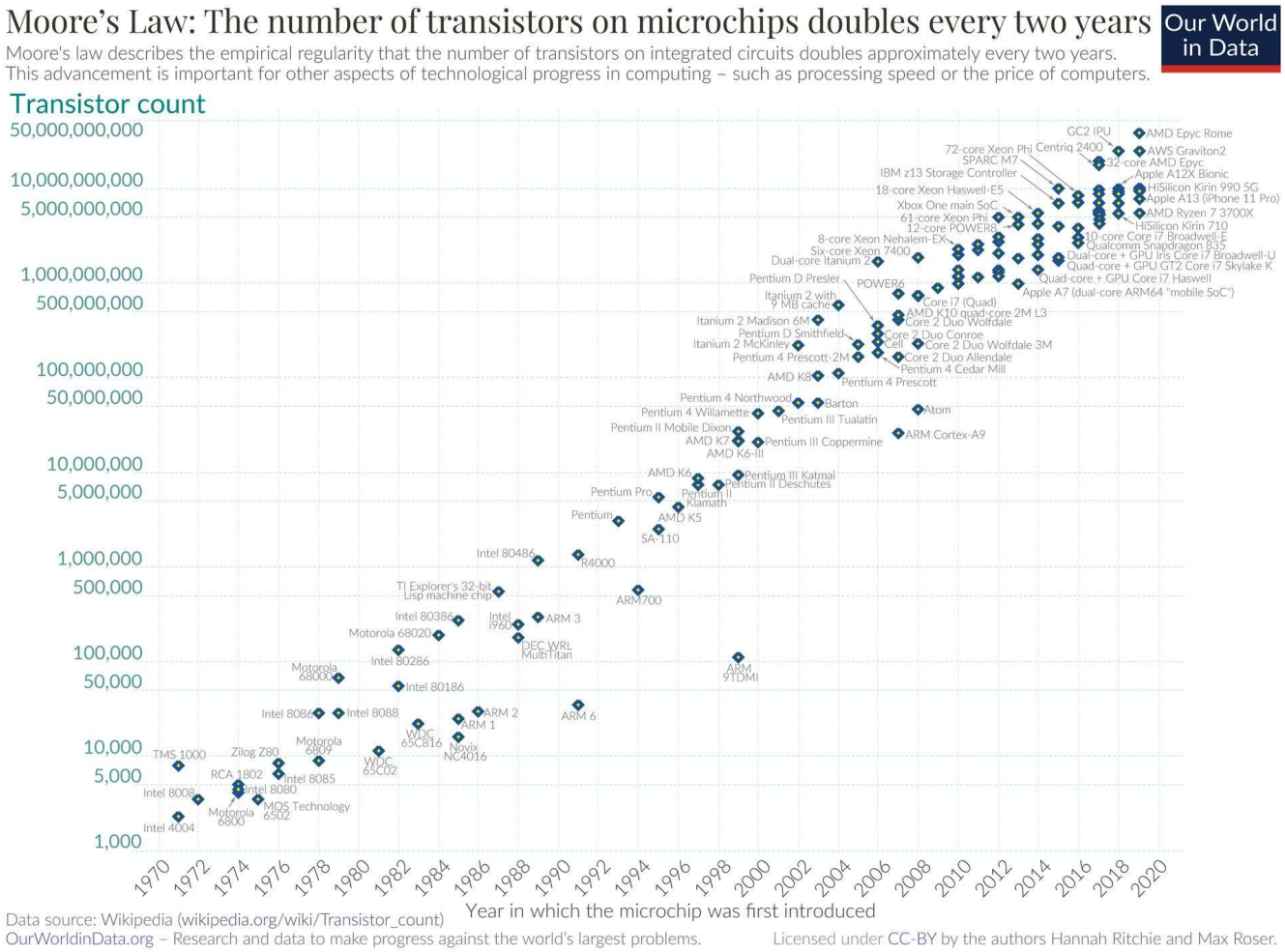
- 2300 transistors
- Data: 4-bit data width
- Address: 12 bits
- Application:
  Calculators for arithmetic operations
- Clock rate: 750 kHz
- Technology node: 10um
- Instruction set: 4-bit

The "4000 family" had

- the Intel 4001, a 256-byte 4-bit ROM;
- the Intel 4002, DRAM with four 20-nibble registers (total size 40 bytes);
- the Intel 4003, an I/O chip comprising a 10-bit static shift register with serial and parallel outputs
- the Intel 4004 CPU

Could interface multiple chips with one CPU

Historical Perspective: Moore's Law



Intel 4004 was the first microprocessor - had 2300 transistors

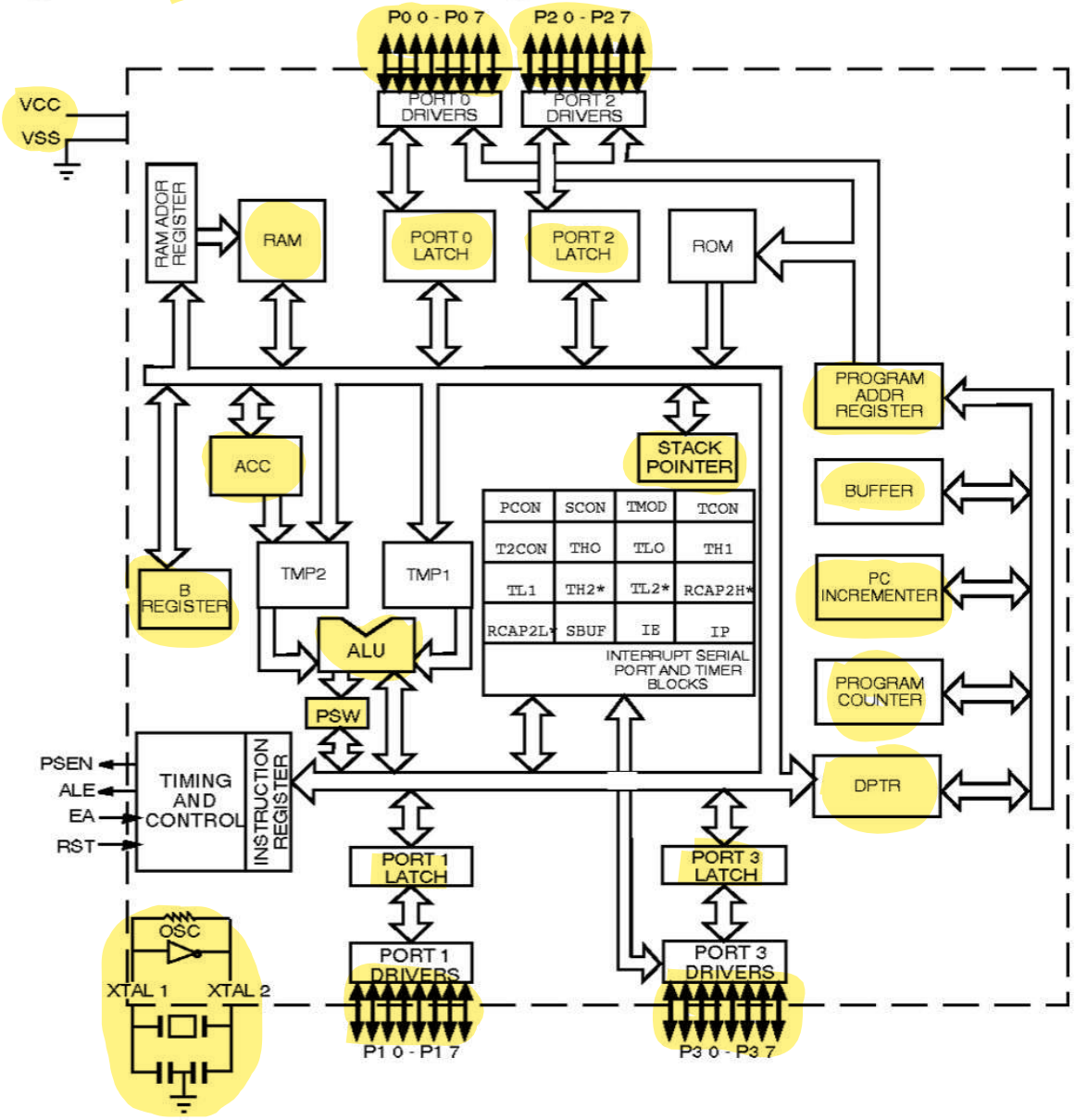
Moore's Law: The transistor count doubled every 2 years (not anymore)

Moore's 1965 paper available at:
http://download.intel.com/museum/Moores_Law/Articles-Press_Releases/Gordon_Moore_1965_Article.pdf

8051 Microcontroller: Block Diagram

Source:
Manual for 8051 microcontrollers
(uploaded in Moodle)

Figure 2-1. 8051 Architecture Block Diagram



8051 Microcontroller: Memory Range

The **8051 microcontroller** has a variety of address ranges for different types of memory:

1. **Program Memory (Code Memory)**:
   - The 8051 has a 16-bit address bus for program memory, allowing it to address up to **64 KB of program memory**.

2. **Data Memory (RAM)**:
   - **Internal RAM**: The 8051 microcontroller has 128 bytes of internal RAM, with address range **0x00 to 0x7F**. Some variants have extended internal RAM up to 256 bytes (0x00 to 0xFF).
   - **External RAM**: Using external memory, the 8051 can address up to **64 KB** of data memory with an additional address space.

3. **Special Function Registers (SFRs)**:
   - The SFRs are mapped to the upper 128 bytes of internal RAM, with address range **0x80 to 0xFF**. These registers control various functions of the microcontroller.

Instruction Set Architecture

1. Instruction Format

- **Length**: Fixed or variable-length instructions.
- **Fields**: Components like opcode, operand(s), and addressing mode.

2. Instruction Types

- **Arithmetic**: Operations like addition, subtraction.
- **Logical**: AND, OR, XOR.
- **Data Transfer**: Load, store, move.
- **Control Flow**: Jumps, branches, calls, returns.
- **Special**: System calls, no-ops.

3. Addressing Modes

- **Immediate**: Operand specified directly.
- **Register**: Operand in a register.
- **Direct**: Operand in a memory location.
- **Indirect**: Address of operand in a register.
- **Indexed**: Base address plus an offset.

4. Instruction Decoding and Execution

- **Fetch**: Retrieve instruction.
- **Decode**: Determine action.
- **Execute**: Perform action.
- **Write-back**: Store result.

5. Performance and Efficiency

- **CISC**: Complex Instruction Set Computing; many specialized instructions.
- **RISC**: Reduced Instruction Set Computing; fewer, simpler instructions.

6. Compatibility

- **Backward Compatibility**: Support for older instructions.
- **Forward Compatibility**: Provision for future instructions.

7. Execution time

- **Number of clock cycles**
- **Number of machine cycles**