Microprocessors (EE309-S2)

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8085 Microprocessor Architecture

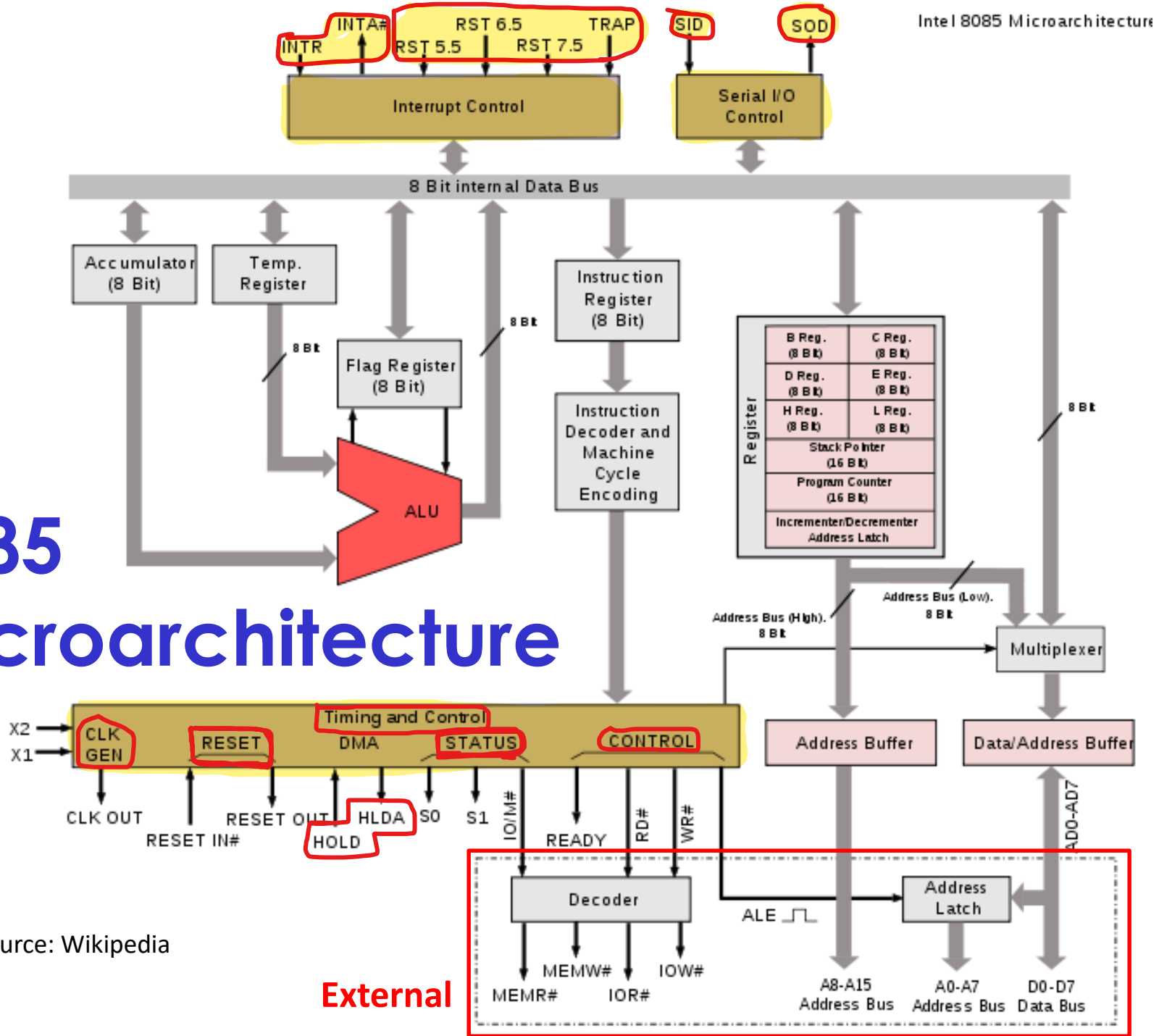
- 8085 based on Von Neumann Architecture
  - Data/Program memory is shared
  - Same bus
  - Separate CPU
  - Separate I/O
- CPU: ALU, Control and Timing Unit, Interface, Registers

8085AH/8085AH-2/8085AH-1
8-BIT HMOS MICROPROCESSORS

- Single +5V Power Supply with 10% Voltage Margins
- 3 MHz, 5 MHz and 6 MHz Selections Available
- 20% Lower Power Consumption than 8085A for 3 MHz and 5 MHz
- 1.3 μs Instruction Cycle (8085AH); 0.8 μs (8085AH-2); 0.67 μs (8085AH-1)
- 100% Software Compatible with 8080A
- On-Chip Clock Generator (with External Crystal, LC or RC Network)
- On-Chip System Controller; Advanced Cycle Status Information Available for Large System Control
- Four Vectored Interrupt Inputs (One Is Non-Maskable) Plus an 8080A-Compatible Interrupt
- Serial In/Serial Out Port
- Decimal, Binary and Double Precision Arithmetic
- Direct Addressing Capability to 64K Bytes of Memory
- Available in 40-Lead Cerdip and Plastic Packages
  (See Packaging Spec., Order #231369)

The Intel 8085AH is a complete 8-bit parallel Central Processing Unit (CPU) implemented in N-channel, depletion load, silicon gate technology (HMOS). Its instruction set is 100% software compatible with the 8080A microprocessor, and it is designed to improve the present 8080A's performance by higher system speed. Its high level of system integration allows a minimum system of three IC's [8085AH (CPU), 8156H (RAM/IO) and 8755A (EPROM/IO)] while maintaining total system expandability. The 8085AH-2 and 8085AH-1 are faster versions of the 8085AH.

8085 microarchitecture



Source: Wikipedia

External

Registers

- General Purpose
  - B(8), C(8) or BC(16)
  - D(8), E(8) or DE(16)
  - H(8), L(8) or HL(16)
- Special Purpose
  - Stack Pointer – SP(16), Program Counter – PC(16), Address Latch(16)
  - Accumulator – A or Acc(8), Temp(8), Instruction Reg(8), Flag Register(8)
  - Program-Status-Word(PSW) (16) is a combination of Acc(8) and Flag Register(8)
  - Flag Register consists of Zero(Z), Carry (CY), Sign (S), Parity (P), and Auxiliary Carry (AC) flags
- Apart from User Accessible registers (RED), there are many other internal registers for intermediate operations

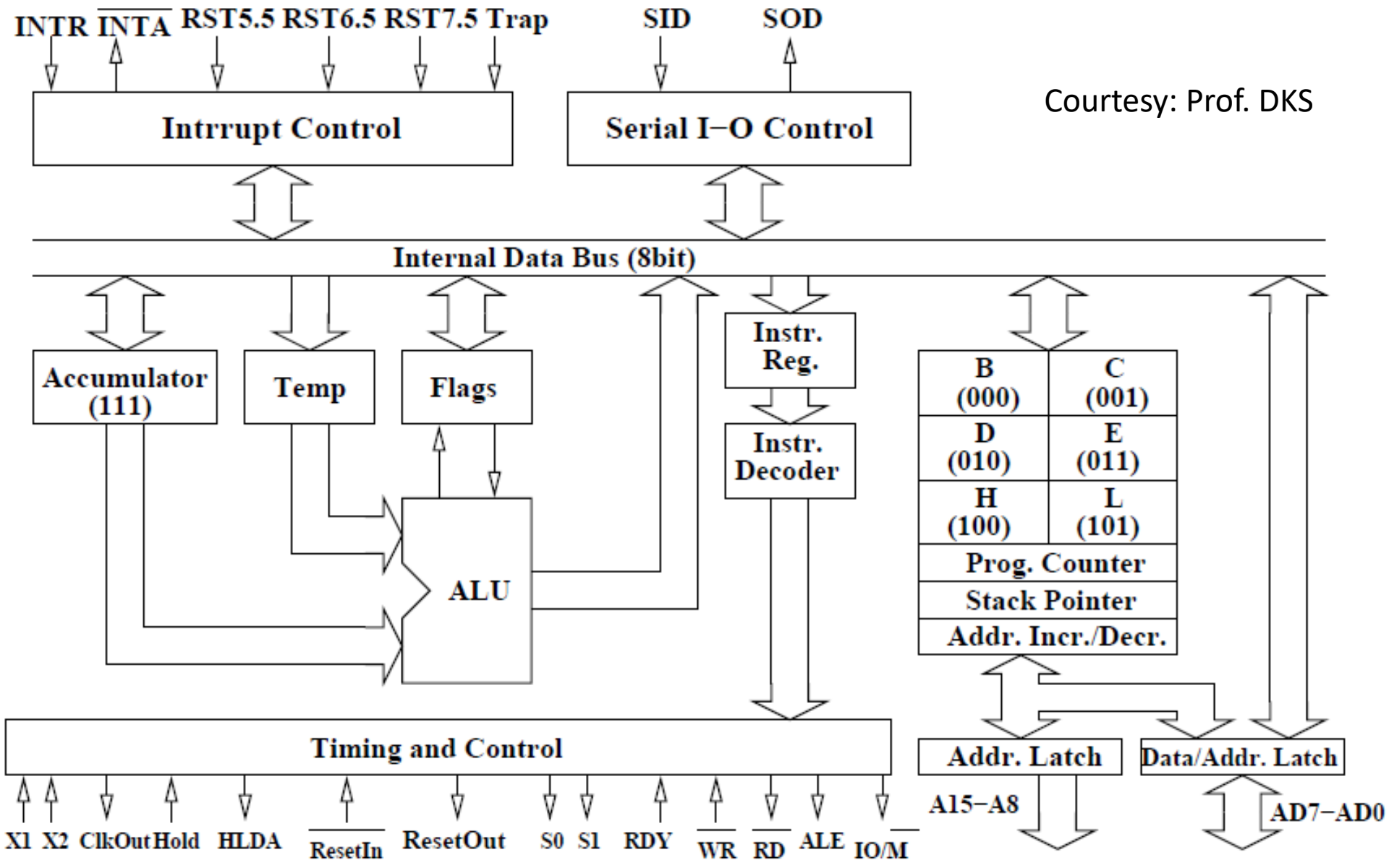
8085 Architecture: ALU

- Arithmetic Operations
  - Add, Subtract, Increment, Decrement
  - NO multiplication available
  - Programs have to be written to multiplication, adding/subtracting bigger numbers
  - Shift Right/Left: Divide or Multiply by 2
- Logic Operations
  - AND, OR, XOR, NOT, Compare (>, <, ==)

Interrupts

- TRAP: Non-maskable interrupt
- RST7.5, RST6.5, RST5.5, INTR: Maskable Interrupts

8085 Internal Architecture



Courtesy: Prof. DKS

Timing & Control Unit

- Consists of sequential and combinatorial logic
- Senses inputs for external world (RESET IN, READY, Interrupts, HOLD etc.)
- Provides handshake signals for external chips – RDB, WRB, HLDA, INTAB
- Provides clock and control signals for internal modules

Clock Generator

- External Crystal (Quartz Resonator) provides frequency reference
- Internal circuitry completes the oscillator
  - And divides the clock by 2 to obtain 2-phase clock
- Alternatively, external source connect at one of the inputs can directly provide clock (see datasheet)
- CLK (out) and internal microprocessor clock are divided-by-2
  - i.e. CLK frequency half of the clock frequency at X1 or X2.

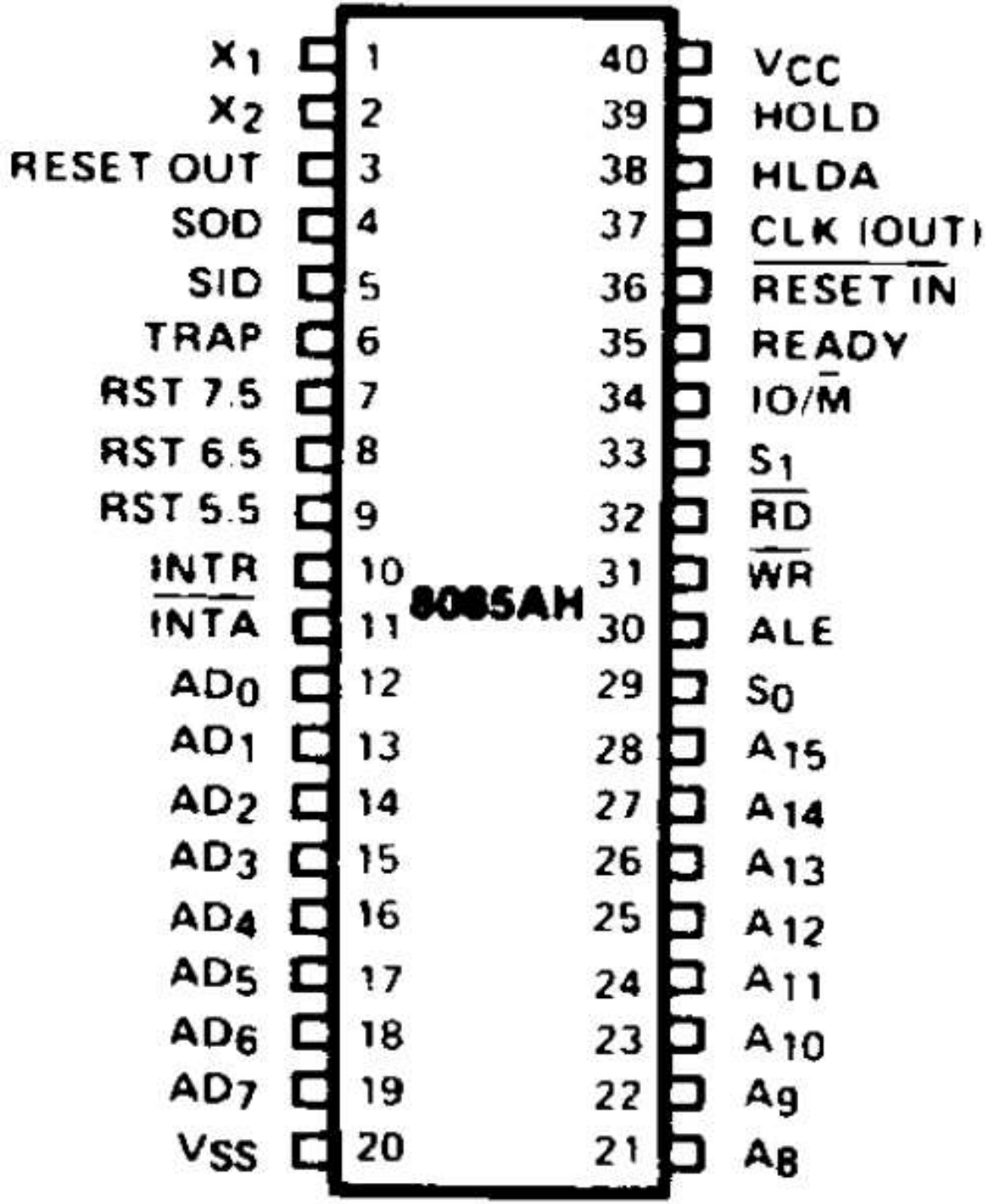
Interrupts

Interrupt	Mask -able	Restart Address	Trigger	Priority
TRAP (RST 4.5)	No	24H	Rising Edge & High Level*	1
RST 7.5	Yes	3CH	Rising Edge	2
RST 6.5	Yes	34H	High Level*	3
RST 5.5	Yes	2CH	High Level*	4
INTR	Yes	Instr.	High Level*	5

*until sampled

Restart interrupts also called "Vectored Interrupts"

Pinout

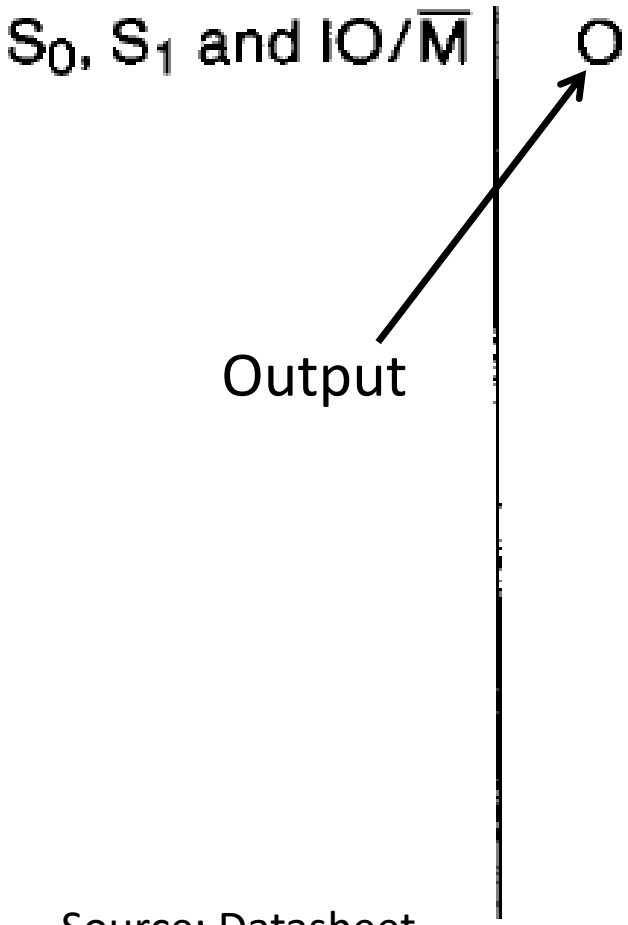


Source: Datasheet

8085 Instruction Execution

- Instruction Cycle consists of a few machine cycles such as
  - Opcode Fetch
  - Memory Read or Write
- Every Instruction Cycle
  - Begins with Opcode Fetch
  - Opcode Fetch Cycle
    - Typically 4 clock periods, sometimes more
  - Execution Cycle(s)
    - Read/Write – 3 clocks (T-states)

Machine Cycle Status Lines



MACHINE CYCLE STATUS:

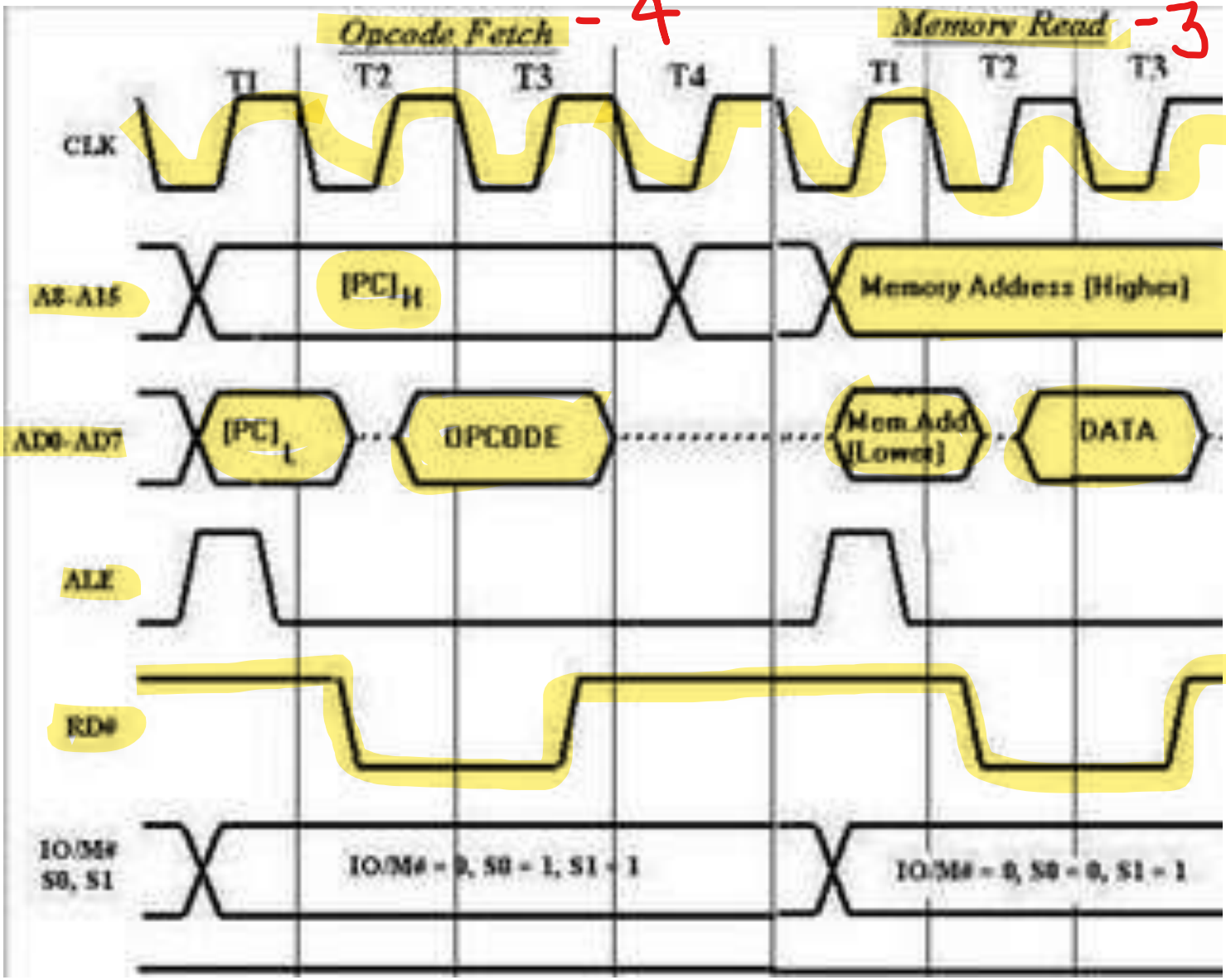
IO/$\overline{M}$	S_1	S_0	Status
0	0	1	Memory write
0	1	0	Memory read
1	0	1	I/O write
1	1	0	I/O read
0	1	1	Opcode fetch
1	1	1	Interrupt Acknowledge
*	0	0	Halt
*	X	X	Hold
*	X	X	Reset

* = 3-state (high impedance)

X = unspecified

Source: Datasheet

Instruction Cycle: Timing Diagram



Source: http:// rohanranjangaonkar.blogspot.in

Example

Store the contents of Accumulator at Memory location $526A_H$

Instruction (mnemonic): STA $526A_H$

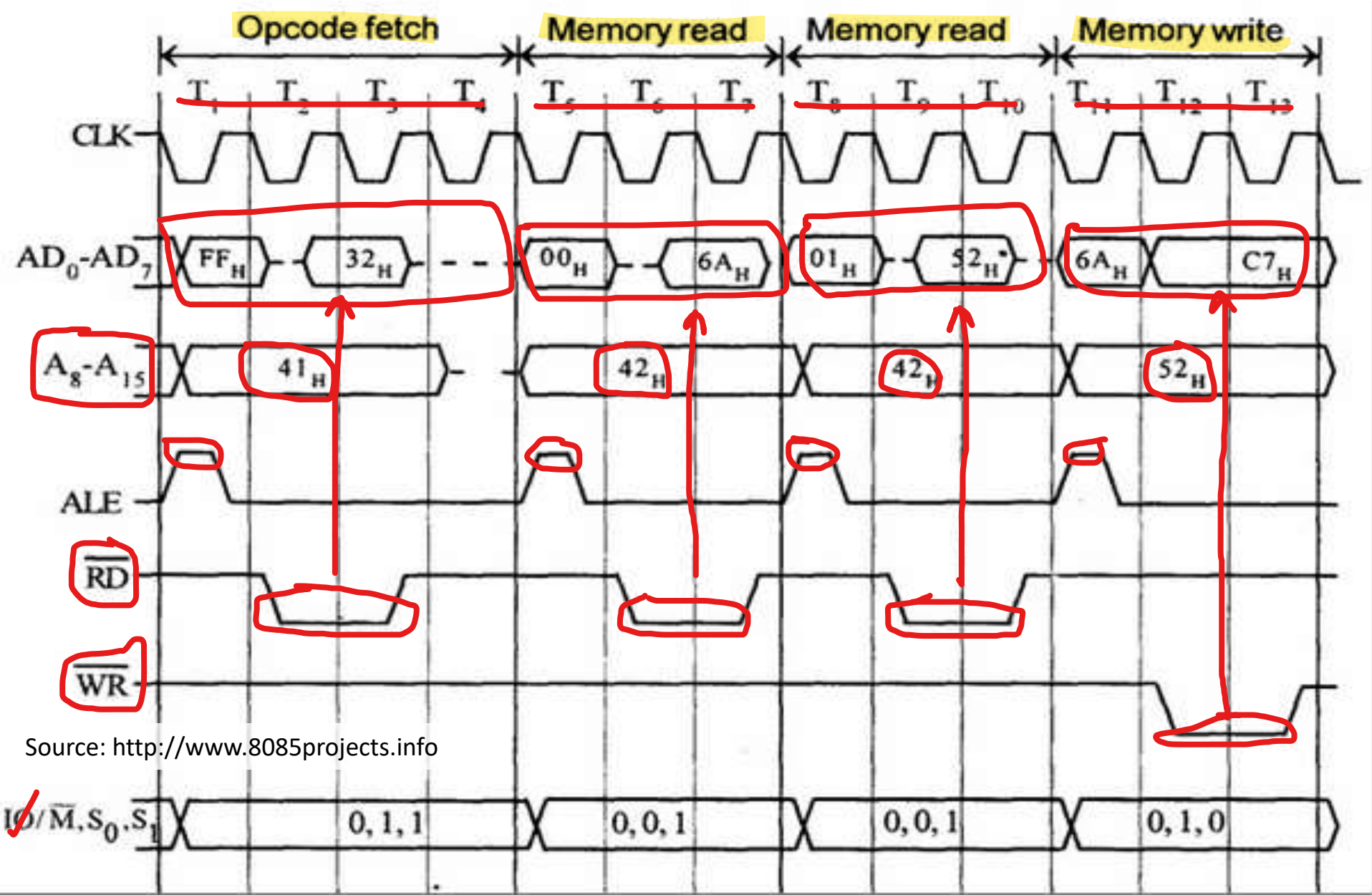
External Memory Location	Memory content	Description of contents
$41FF_H$	32_H	Opcode for STA
4200_H	$6A_H$	Lower Byte of $526A_H$
4201_H	52_H	Upper Byte of $526A_H$
..	..	..
$526A_H$	unknown	

Before execution: PC = $41FF_H$

External Memory Location	Memory content	Description of contents
$41FF_H$	32_H	Opcode for STA
4200_H	$6A_H$	Lower Byte of $526A_H$
4201_H	52_H	Upper Byte of $526A_H$
..	..	..
$526A_H$	Same data as in the accumulator	

After execution: PC = 4202_H

Timing Diagram: STA $526A_H$



Source: http://www.8085projects.info

8085 Instruction Execution

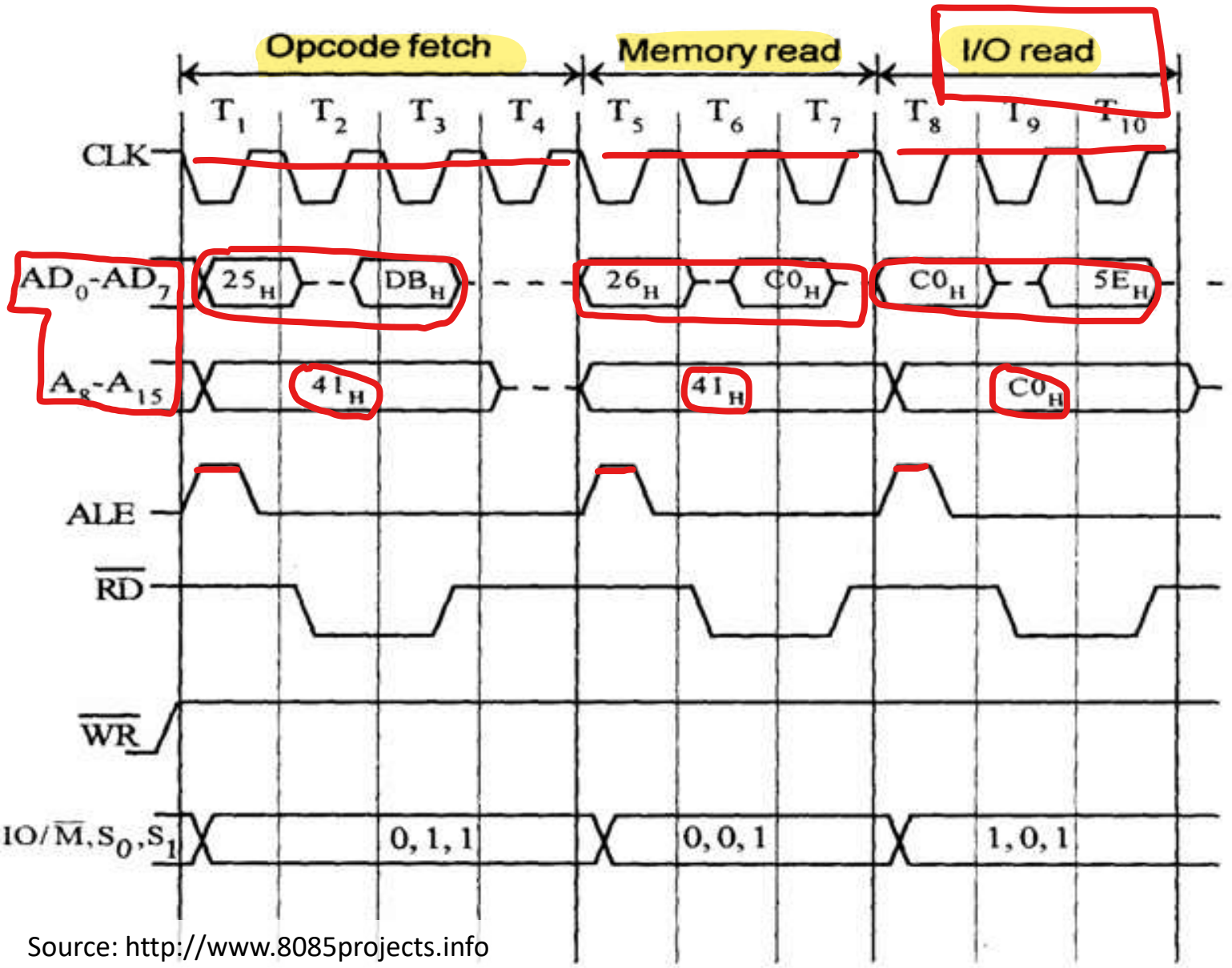
- Instruction Cycle consists of a few machine cycles such as
  - Opcode Fetch
  - Memory Read or Write
- Every Instruction Cycle
  - begins with Opcode Fetch
  - Opcode Fetch Cycle (4 clock periods) or sometimes more
  - Execution Cycle(s) require
    - Read/Write – Typically 3 clocks (T-states)/MC
    - Bus Idle Machine Cycle

Example

Store the contents of I/O device with address $C0_H$ to Acc.
Instruction (mnemonic): $\underline{IN\ \ C0_H}$

External Memory Location	Memory content	Description of contents
4125_H	DB_H	Opcode for IN
4126_H	$C0_H$	I/O address
..	..	..

Timing Diagram: IN $C0_H$



Source: http://www.8085projects.info

T-states/instruction: Rule of thumb

- Most instructions require

  *(3+w)*n+1* T-states

  – w is the number of T-states inserted if the memory device is slow

  – n is the number of times the memory or IO device has to be read or written

Wait States: Slow Mem/IO device

Wait state inserted if READY signal is found to be low towards the end of 2nd T-state of the machine cycle

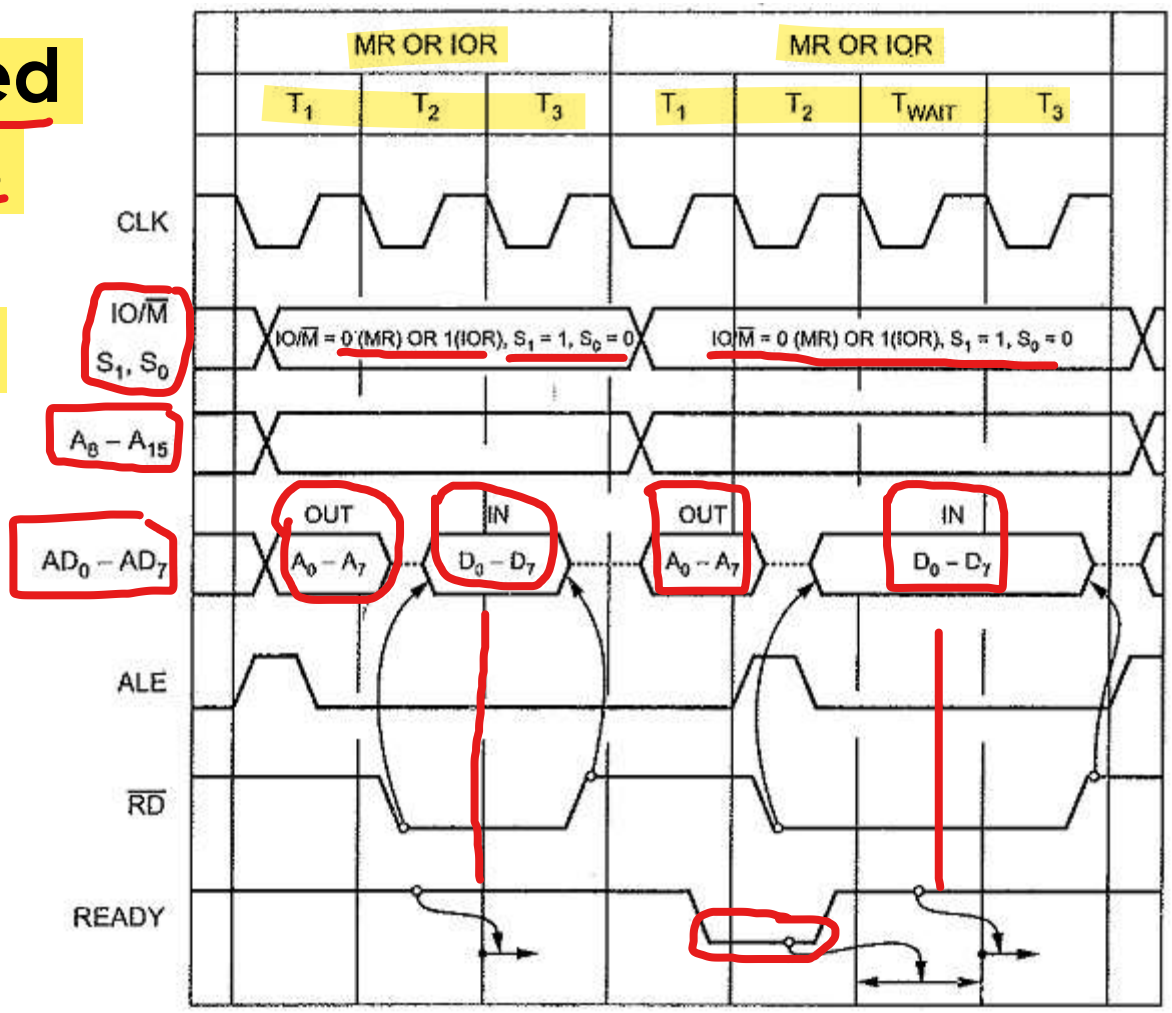


Fig. 1.24 Read machine cycle with and without wait state

https://www.eeeguide.com/machine-cycle-in-8085-microprocessor/

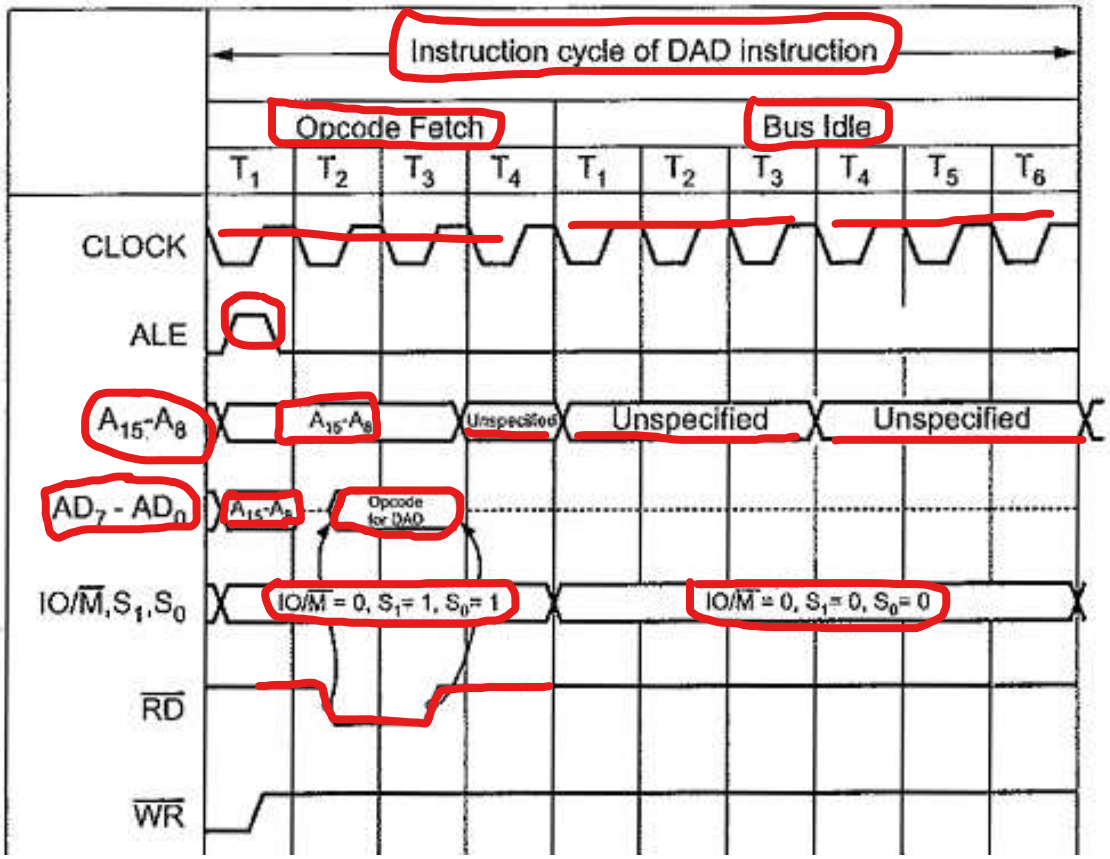
Exceptions

- Instructions involving 16-bit operations:
  - 6 T-state Opcode Fetch cycles are there in the following:
    - INR, DCR: 16-bit data has to be incremented or decremented
    - CALL, PUSH instruction – 16-bit SP has to be decremented after Instruction decoder tells that it is a CALL/PUSH instruction

      Note: RETURN, POP have 4 T-state OF cycle only (SP is not changed during OF cycle, is changed in parallel during read cycles of RETURN/POP)

Other Exceptions

DAD instruction require ~~12~~10 T-States (OF: ~~6~~ 4, two Bus Idle cycles of 3 T-states each)



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Sample Problem: Draw the timing diagram for the RET (Return) instruction.
This instruction pops the return address from the stack and resumes execution from the return address.

Other Exceptions

- Other exceptions that involve longer operation after Opcode is decoded:
  - Conditional Jump instructions
  - Conditional Call Instructions
  - Conditional Return instruction
  - HALT, PCHL, RST, SPHL

Number Systems used in Microprocessors (for additional reading, not included in quiz/exam syllabus)

- **References: Goankar: Appendix A**
- **Wikipedia page:**

  http://en.wikipedia.org/wiki/IEEE_754-1985

  Converter for floating point numbers (in IEEE 754 format):

  http://www.h-schmidt.net/FloatConverter/IEEE754.html