EE309(S2): Microprocessors

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[Week#7 Slides]

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Interrupt Priority

IP: INTERRUPT PRIORITY REGISTER. BIT ADDRESSABLE

If the bit is 0, the corresponding interrupt has a lower priority and if the bit is 1 the corresponding interrupt has a higher priority.

–	–	–	PS	PT1	PX1	PT0	PX0

–	IP.7	Not implemented, reserved for future use.*
–	IP.6	Not implemented, reserved for future use.*
–	IP.5	Not implemented, reserved for future use.*
PS	IP.4	Defines the Serial Port interrupt priority level.
PT1	IP.3	Defines the Timer 1 interrupt priority level.
PX1	IP.2	Defines External Interrupt 1 priority level.
PT0	IP.1	Defines the Timer 0 interrupt priority level.
PX0	IP.0	Defines the External Interrupt 0 priority level.

* User software should not write 1s to reserved bits. These bits may be used in future 80C51 products to invoke new features.

Table 2-27. Interrupt Priority Level

	Source	Priority Within Level
1	IE0	(highest)
2	TF0	
3	IE1	
4	TF1	
5	RI + TI	
6	TF2 + EXF2	(lowest)

Computer Architecture

Computer Architecture

Computer Organization

- Deals with microprocessors from the end user / programmers perspective

Computer Architecture

- Deals with microprocessors from the circuit designers perspective

Both perspectives important for improving performance of computing systems and using them efficiently

Reference Book:
Computer Architecture: A Quantitative Approach, 4th Edition by David A. Patterson and John L. Hennessy (2006)

Computer Architecture: Topics

- **Performance evaluation**
- **Instruction Set Architecture**
  - **ALU design: ALU components**
- **Processor design**
  - **How the processor can be designed to execute different instructions**
  - **Hardware architecture**
- **Performance Improvement**
  - **Pipelining**
  - **Cache and Virtual Memory**
  - **Parallelism**

Microprocessor Architecture

Instruction Set Architecture

–RISC (Reduced Instruction Set Computer)

–CISC (Complex Instruction Set Computer)

Micro-architecture

–How different modules are organized

–How data flows

Performance Evaluation

Performance measurement in terms of time only

–Execution Time

- **Throughput or (No. of tasks)/(unit time)**
- **Important for signal processing**

–Latency (Delay)

- **Response time**
- **Important for data movement tasks such as data base queries or servicing interrupts**
- **Important for systems involving feedback**

Different performance benchmarks are based on different tasks (or programs) such as gaming, video encoding/ decoding, compiler operation, AI training / parameter handling

Performance at What Cost

Cost of the microprocessor

- **Chip area**
- **Technology used**
- **Design effort**

Power Consumption => Cost

- **Data Centers or battery powered devices**
- **ASP (average selling price) of the product**

Power or Energy consumed

- **Energy consumed per unit task**
- **Power consumed for a given throughput**

Reducing Power <> Energy (Tradeoff)

Energy-Delay trade-off as voltage can be scaled

- **Less Execution Time (or Delay) => More Energy required for the task**

Energy-Delay tradeoff can be broken using more hardware

- **Parallel architectures**
- **Pipelining**

Dynamic voltage scaling possible using some processors, operating systems

Other discussions

- Multi-processor communication example
- Dynamic voltage scaling for performance vs power tradeoff
- Parallelism for more throughput or power saving along with voltage scaling - example.