EE309(S2): Microprocessors

Spring 2025

[Week #3 Slides]

Instructor: Shalabh Gupta

Program Status Word (PSW

What is the default RS0 and RS1 pair??

Table 1-1. PSW: Program Status Word Register

(MSB)							(LSB)
CY	AC	F0	RS1	RS0	OV	-	P

Symbol	Position	Name and Significance
CY	PSW.7	Carry flag
AC	PSW.6	Auxiliary Carry flag. (For BCD operations.)
F0	PSW.5	Flag 0 (Available to the user for general purposes.)
RS1	PSW.4	Register bank Select control bits 1 & 0. Set/cleared by software to determine working register bank (see Note).
RS0	PSW.3	
OV	PSW.2	Overflow flag.
-	PSW.1	(reserved)
P	PSW.0	Parity flag. Set/cleared by hardware each instruction cycle to indicate and odd/even number of "one" bits in the accumulator, i.e., even parity.

Note:
The contents of (RS1, RS0) enable the working register banks as follows:
(0.0)-Bank 0(00H-07H)
(0.1)-Bank 1(08H-0FH)
(1.0)-Bank 2(10H-17H)
(1.1)-Bank 3(18H-1FH)

Courtesy: 8051 Manual

Data Transfer Instructions (Internal RAM)

58 instructions that can be used with the operation "MOV"

Table 1-4. Atmel 8051 Data Transfer Instructions that Access Internal Data Memory Space

Mnemonic	Operation	Addressing Modes				Execution Time @ 12MHz (µs)
		Dir	Ind	Reg	Imm	
MOV A, <src>	A = <src>	X	X	X	X	1
MOV <dest>, A	<dest> = A	X	X	X		1
MOV <dest>, <src>	<dest> = <src>	X	X	X	X	2
MOV DPTR, # data 16	DPTR = 16-bit immediate constant				X	2
PUSH <src>	INC SP: MOV "@SP", <scr>	X				2
POP <dest>	MOV <dest>, "@SP": DEC SP	X				2
XCH A, <byte>	ACC and <byte> Exchange Data	X	X	X		1
XCHD A, @Ri	ACC and @ Ri exchange low nibbles		X			1

Courtesy: 8051 Manual

Data Transfer: External RAM

Table 1-7. Data Transfer Instructions that Access External Data Memory Space

Address Width	Mnemonic	Operation	Execution Time @ 12MHz (µs)
8 bits	MOVX A, @Ri	Read external RAM @ Ri	2
8 bits	MOVX @ Ri, A	Write external RAM @ Ri	2
16 bits	MOVX A, @ DPTR	Read external RAM @ DPTR	2
16 bits	MOVX @ DPTR, A	Write external RAM @ DPTR	2

Courtesy: 8051 Manual

Look Up Table

Table 1-8. Lookup Table Read Instructions

Mnemonic	Operation	Execution Time @ 12MHz (µs)
MOVC A, @A + DPTR	Read Pgm Memory at (A + DPTR)	2
MOVC A, @A + PC	Read Pgm Memory at (A + PC)	2

Indexed Addressing

```
MOV A, ENTRY_NUMBER
CALL  TABLE

#The subroutine “TABLE”:

TABLE: MOVC A, @A + PC
RET
```

Courtesy: 8051 Manual

Arithmetic Instructions

Table 1-2. A list of the Atmel 8051 Arithmetic Instructions.

Mnemonic	Operation	Addressing Modes				Execution Time in X1 Mode @12 MHz (µs)
		Dir	Ind	Reg	Imm	
ADD A, <byte>	A = A + <byte>	X	X	X	X	
ADDC A, <byte>	A = A + <byte> + C	X	X	X	X	1
SUBB A, <byte>	A = A – <byte> – C	X	X	X	X	1
INC A	A = A + 1	Accumulator only				1
INC <byte>	<byte> = <byte> + 1	X	X	X		1
INC DPTR	DPTR = DPTR + 1	Data Pointer only				2
DEC A	A = A – 1	Accumulator only				1
DEC <byte>	<byte> = <byte> – 1	X	X	X		1
MUL AB	B:A = B × A	ACC and B only				4
DIV AB	A = Int [A/B] B = Mod [A/B]	ACC and B only				4
DA A	Decimal Adjust	Accumulator only				1

Courtesy: 8051 Manual

ADD Instructions

Instructions	OpCode	Bytes	Flags
ADD A,*#data*	0x24	2	C, AC, OV
ADD A,*iram addr*	0x25	2	C, AC, OV
ADD A,@R0	0x26	1	C, AC, OV
ADD A,@R1	0x27	1	C, AC, OV
ADD A,R0	0x28	1	C, AC, OV
ADD A,R1	0x29	1	C, AC, OV
ADD A,R2	0x2A	1	C, AC, OV
ADD A,R3	0x2B	1	C, AC, OV
ADD A,R4	0x2C	1	C, AC, OV
ADD A,R5	0x2D	1	C, AC, OV
ADD A,R6	0x2E	1	C, AC, OV
ADD A,R7	0x2F	1	C, AC, OV

Affects C, AC, OV flags

OV flag is set if the two's complement number addition overflows

ADD A,R_n

Bytes: 1

Cycles: 1

Encoding:

0	0	1	0	1	r	r	r

Operation: ADD
(A) ← (A) + (R_n)

ADD A,direct

Bytes: 2

Cycles: 1

Encoding:

0	0	1	0	0	1	0	1	direct address

Operation: ADD
(A) ← (A) + (direct)

ADD A,@R_i

Bytes: 1

Cycles: 1

Encoding:

0	0	1	0	0	1	1	i

Operation: ADD
(A) ← (A) + ((R_i))

ADD A,#data

Bytes: 2

Cycles: 1

Encoding:

0	0	1	0	0	1	0	0	immediate data

Operation: ADD
(A) ← (A) + #data

Courtesy: 8051 Manual

List of operands (arguments) in 8051

Addr11: An 11-bit address destination. This argument is used by ACALL and AJMP instructions. The target of the CALL or JMP must lie within the same 2K page as the first byte of the following instruction.

Addr16: A 16-bit address destination. This argument is used by LCALL and LJMP instructions.

Bit: A direct addressed bit in internal data RAM or SFR memory.

Direct: An internal data RAM location (0-127) or SFR (128-255).

Immediate: A constant included in the instruction encoding.

Offset: A signed (two's complement) 8-bit offset (-128 to 127) relative to the first byte of the following instruction.

@Ri: An internal data RAM location (0-255) addressed indirectly through R0 or R1.

Rn: Register R0-R7. There are 2^(8) RAM locations in 8051 and each one of them is 8-bit long = 2^(8)