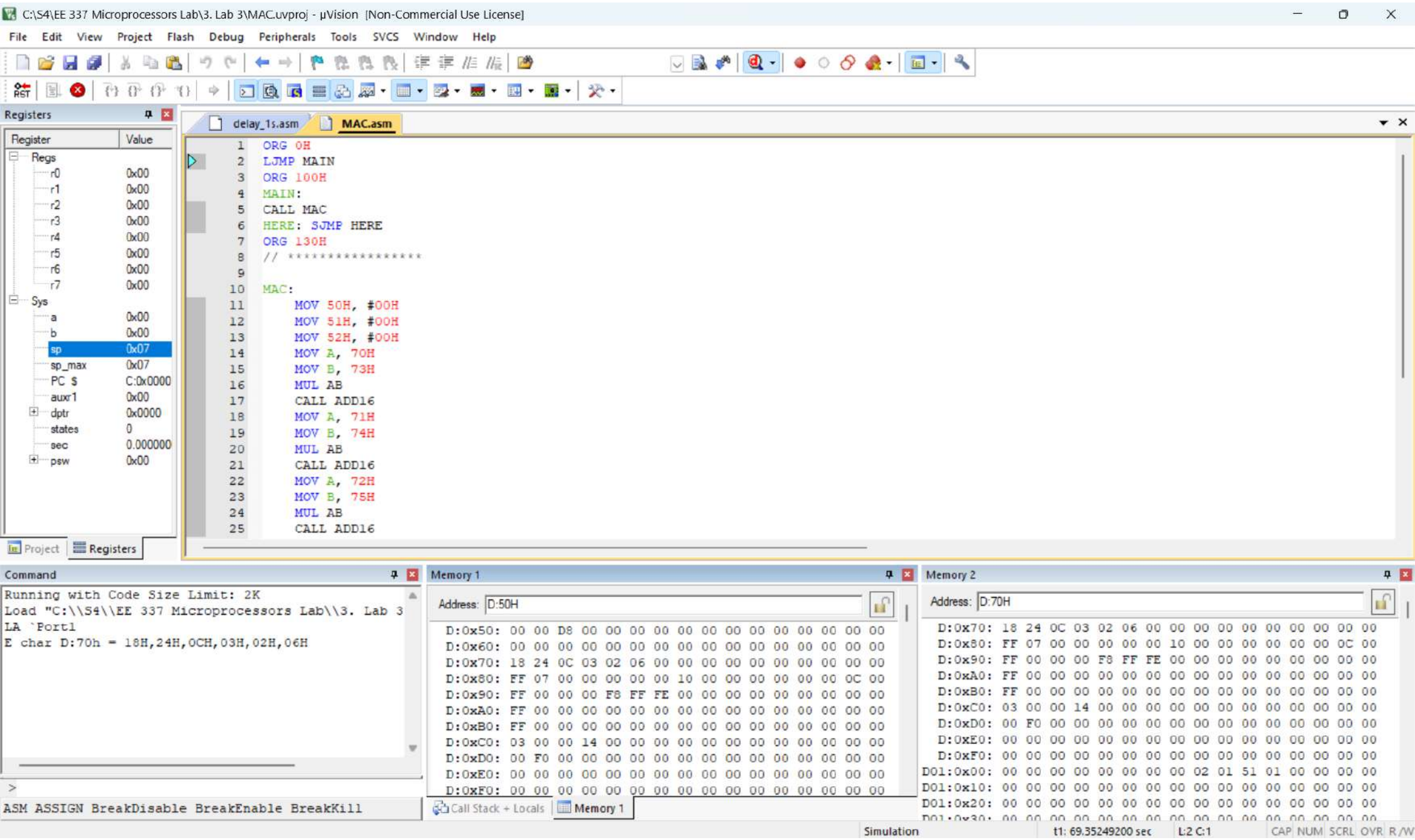
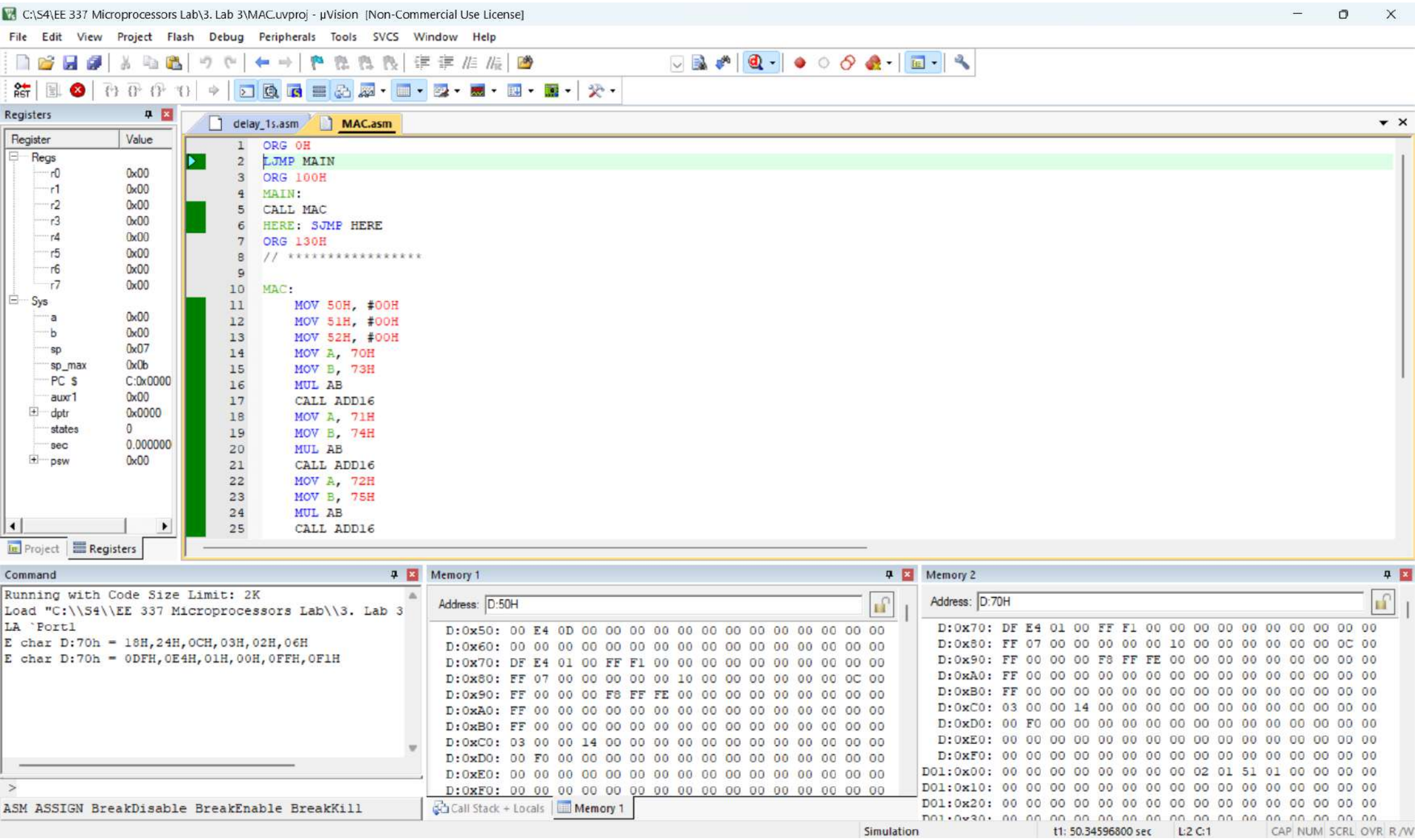
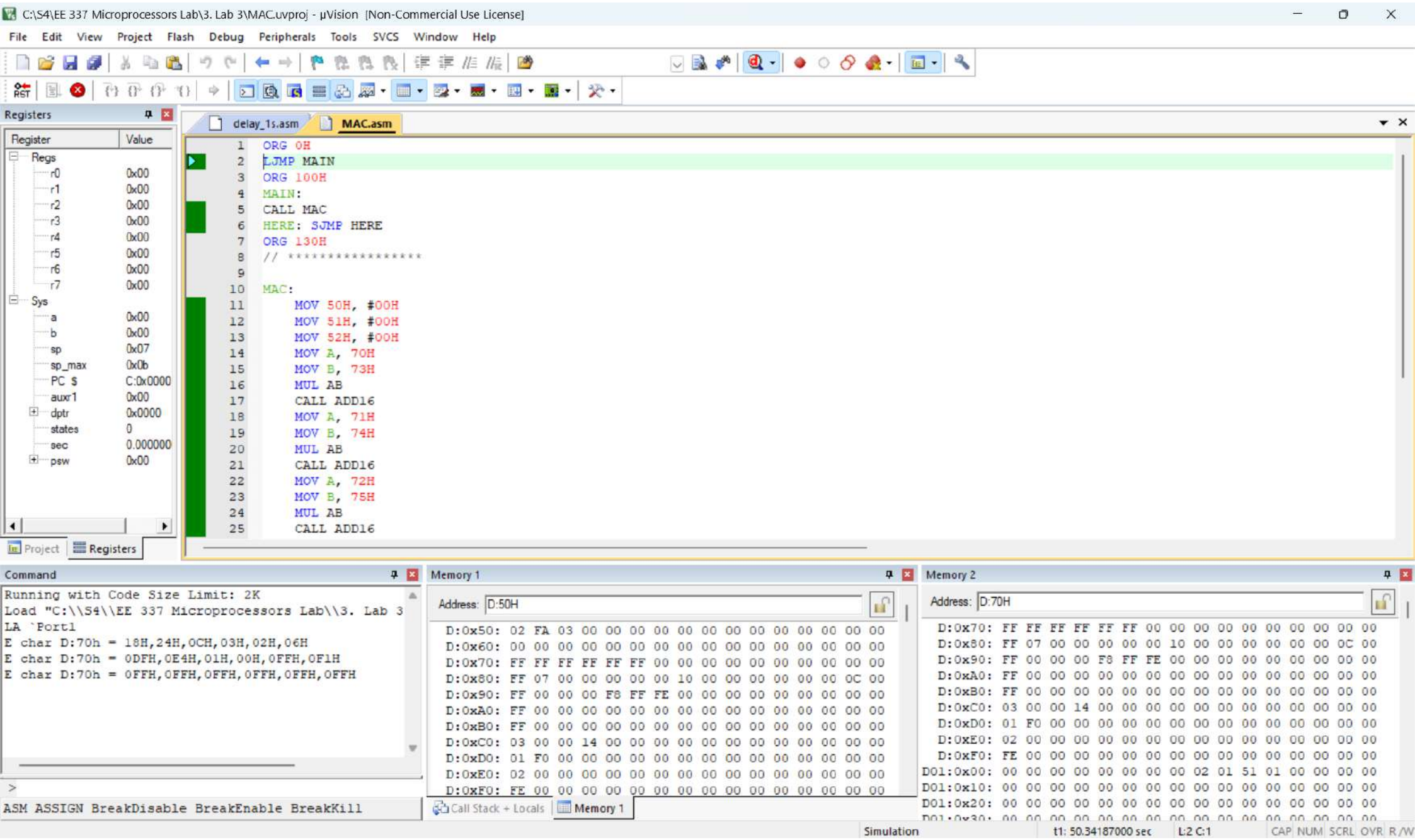
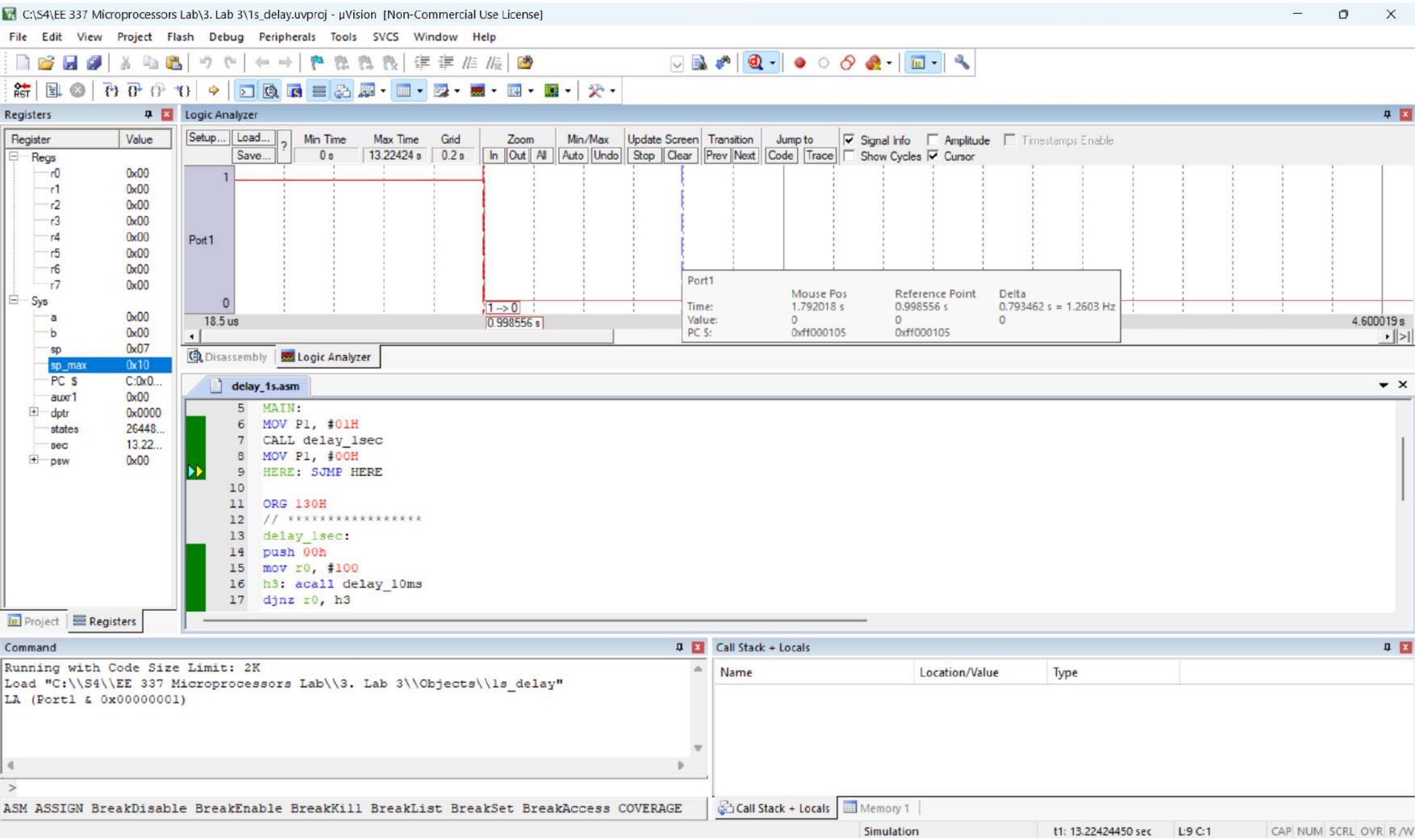
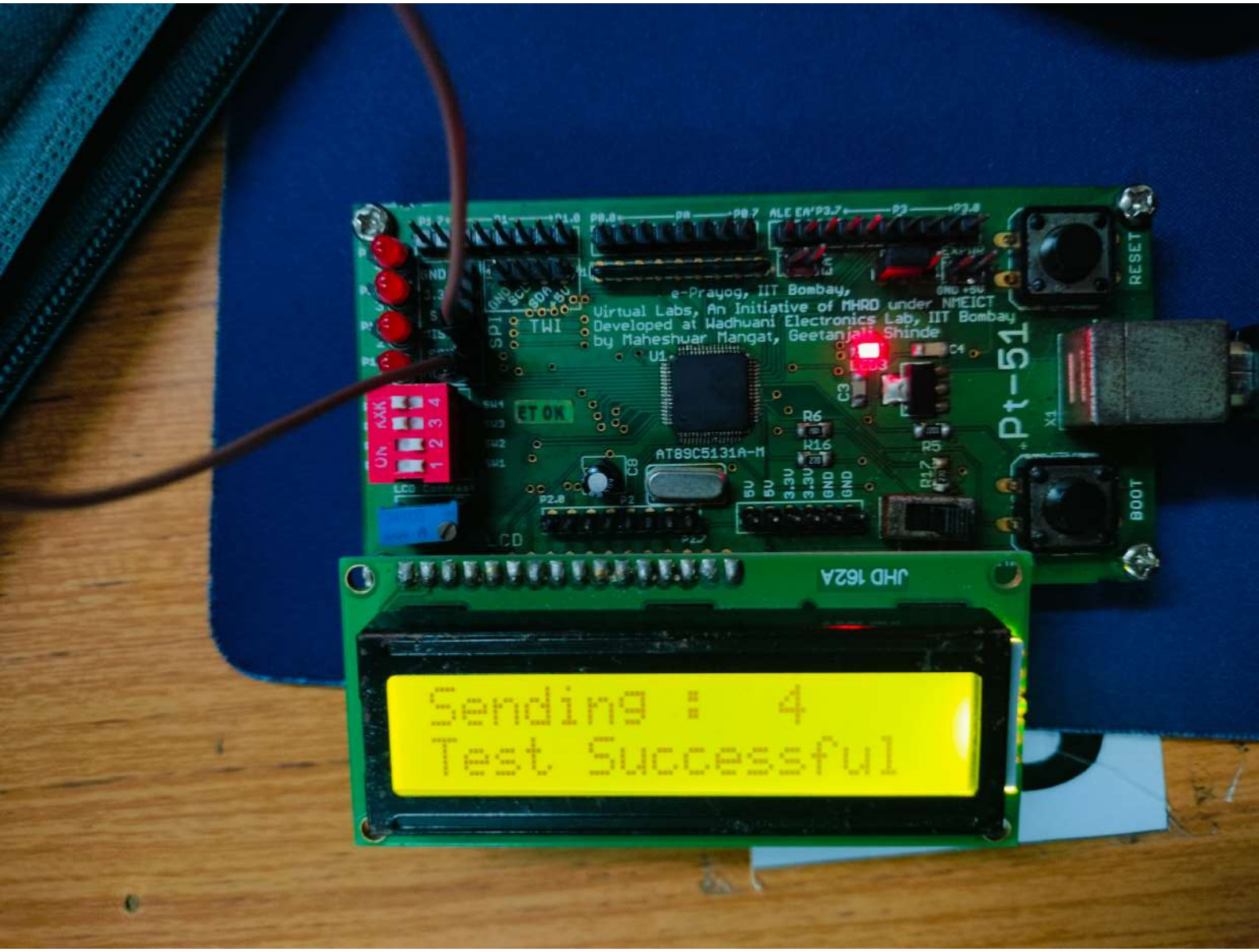

C:\S4\EE 337 Microprocessors Lab\3. Lab 3\MAC.uvproj - µVision [Non-Commercial Use License]
File Edit View Project Flash Debug Peripherals Tools SVCS Window Help
Registers
Register Value
Regs
r0 0x00
r1 0x00
r2 0x00
r3 0x00
r4 0x00
r5 0x00
r6 0x00
r7 0x00
Sys
a 0x00
b 0x00
sp 0x07
sp_max 0x07
PC $ C:0x0000
auxr1 0x00
dptr 0x0000
states 0
sec 0.000000
psw 0x00
Project Registers
delay_1s.asm MAC.asm
1 ORG 0H
2 LJMP MAIN
3 ORG 100H
4 MAIN:
5 CALL MAC
6 HERE: SJMP HERE
7 ORG 130H
8 // ******************
9
10 MAC:
11 MOV 50H, #00H
12 MOV 51H, #00H
13 MOV 52H, #00H
14 MOV A, 70H
15 MOV B, 73H
16 MUL AB
17 CALL ADD16
18 MOV A, 71H
19 MOV B, 74H
20 MUL AB
21 CALL ADD16
22 MOV A, 72H
23 MOV B, 75H
24 MUL AB
25 CALL ADD16
Command
Running with Code Size Limit: 2K
Load "C:\\S4\\EE 337 Microprocessors Lab\\3. Lab 3
LA `Port1
E char D:70h = 18H,24H,0CH,03H,02H,06H
ASM ASSIGN BreakDisable BreakEnable BreakKill
Memory 1
Address: D:50H
D:0x50: 00 00 D8 00 00 00 00 00 00 00 00 00 00 00 00 00
D:0x60: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
D:0x70: 18 24 0C 03 02 06 00 00 00 00 00 00 00 00 00 00
D:0x80: FF 07 00 00 00 00 00 10 00 00 00 00 00 00 0C 00
D:0x90: FF 00 00 00 F8 FF FE 00 00 00 00 00 00 00 00 00
D:0xA0: FF 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
D:0xB0: FF 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
D:0xC0: 03 00 00 14 00 00 00 00 00 00 00 00 00 00 00 00
D:0xD0: 00 F0 00 00 00 00 00 00 00 00 00 00 00 00 00 00
D:0xE0: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
D:0xF0: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
Call Stack + Locals Memory 1
Memory 2
Address: D:70H
D:0x70: 18 24 0C 03 02 06 00 00 00 00 00 00 00 00 00 00
D:0x80: FF 07 00 00 00 00 00 10 00 00 00 00 00 00 0C 00
D:0x90: FF 00 00 00 F8 FF FE 00 00 00 00 00 00 00 00 00
D:0xA0: FF 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
D:0xB0: FF 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
D:0xC0: 03 00 00 14 00 00 00 00 00 00 00 00 00 00 00 00
D:0xD0: 00 F0 00 00 00 00 00 00 00 00 00 00 00 00 00 00
D:0xE0: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
D:0xF0: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
D01:0x00: 00 00 00 00 00 00 00 00 02 01 51 01 00 00 00 00
D01:0x10: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
D01:0x20: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
Simulation
t1: 69.35249200 sec
L:2 C:1
CAP NUM SCRL OVR R /W


C:\S4\EE 337 Microprocessors Lab\3. Lab 3\MAC.uvproj - µVision [Non-Commercial Use License]
File Edit View Project Flash Debug Peripherals Tools SVCS Window Help
Registers
Register Value
Regs
r0 0x00
r1 0x00
r2 0x00
r3 0x00
r4 0x00
r5 0x00
r6 0x00
r7 0x00
Sys
a 0x00
b 0x00
sp 0x07
sp_max 0x0b
PC $ C:0x0000
auxr1 0x00
dptr 0x0000
states 0
sec 0.000000
psw 0x00
Project
Registers
delay_1s.asm
MAC.asm
1 ORG 0H
2 LJMP MAIN
3 ORG 100H
4 MAIN:
5 CALL MAC
6 HERE: SJMP HERE
7 ORG 130H
8 // ******************
9
10 MAC:
11 MOV 50H, #00H
12 MOV 51H, #00H
13 MOV 52H, #00H
14 MOV A, 70H
15 MOV B, 73H
16 MUL AB
17 CALL ADD16
18 MOV A, 71H
19 MOV B, 74H
20 MUL AB
21 CALL ADD16
22 MOV A, 72H
23 MOV B, 75H
24 MUL AB
25 CALL ADD16
Command
Running with Code Size Limit: 2K
Load "C:\\S4\\EE 337 Microprocessors Lab\\3. Lab 3
LA `Port1
E char D:70h = 18H,24H,0CH,03H,02H,06H
E char D:70h = 0DFH,0E4H,01H,00H,0FFH,0F1H
>
ASM ASSIGN BreakDisable BreakEnable BreakKill
Memory 1
Address: D:50H
D:0x50: 00 E4 0D 00 00 00 00 00 00 00 00 00 00 00 00 00
D:0x60: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
D:0x70: DF E4 01 00 FF F1 00 00 00 00 00 00 00 00 00 00
D:0x80: FF 07 00 00 00 00 00 10 00 00 00 00 00 00 0C 00
D:0x90: FF 00 00 00 F8 FF FE 00 00 00 00 00 00 00 00 00
D:0xA0: FF 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
D:0xB0: FF 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
D:0xC0: 03 00 00 14 00 00 00 00 00 00 00 00 00 00 00 00
D:0xD0: 00 F0 00 00 00 00 00 00 00 00 00 00 00 00 00 00
D:0xE0: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
D:0xF0: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
Call Stack + Locals
Memory 1
Memory 2
Address: D:70H
D:0x70: DF E4 01 00 FF F1 00 00 00 00 00 00 00 00 00 00
D:0x80: FF 07 00 00 00 00 00 10 00 00 00 00 00 00 0C 00
D:0x90: FF 00 00 00 F8 FF FE 00 00 00 00 00 00 00 00 00
D:0xA0: FF 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
D:0xB0: FF 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
D:0xC0: 03 00 00 14 00 00 00 00 00 00 00 00 00 00 00 00
D:0xD0: 00 F0 00 00 00 00 00 00 00 00 00 00 00 00 00 00
D:0xE0: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
D:0xF0: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
D01:0x00: 00 00 00 00 00 00 00 00 02 01 51 01 00 00 00 00
D01:0x10: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
D01:0x20: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
Simulation
t1: 50.34596800 sec
L:2 C:1
CAP NUM SCRL OVR R /W


C:\S4\EE 337 Microprocessors Lab\3. Lab 3\MAC.uvproj - µVision [Non-Commercial Use License]
File Edit View Project Flash Debug Peripherals Tools SVCS Window Help
Registers
Register Value
Regs
r0 0x00
r1 0x00
r2 0x00
r3 0x00
r4 0x00
r5 0x00
r6 0x00
r7 0x00
Sys
a 0x00
b 0x00
sp 0x07
sp_max 0x0b
PC $ C:0x0000
auxr1 0x00
dptr 0x0000
states 0
sec 0.000000
psw 0x00
Project
Registers
delay_1s.asm
MAC.asm
1 ORG 0H
2 LJMP MAIN
3 ORG 100H
4 MAIN:
5 CALL MAC
6 HERE: SJMP HERE
7 ORG 130H
8 // ******************
9
10 MAC:
11 MOV 50H, #00H
12 MOV 51H, #00H
13 MOV 52H, #00H
14 MOV A, 70H
15 MOV B, 73H
16 MUL AB
17 CALL ADD16
18 MOV A, 71H
19 MOV B, 74H
20 MUL AB
21 CALL ADD16
22 MOV A, 72H
23 MOV B, 75H
24 MUL AB
25 CALL ADD16
Command
Running with Code Size Limit: 2K
Load "C:\\S4\\EE 337 Microprocessors Lab\\3. Lab 3
LA `Port1
E char D:70h = 18H,24H,0CH,03H,02H,06H
E char D:70h = 0DFH,0E4H,01H,00H,0FFH,0F1H
E char D:70h = 0FFH,0FFH,0FFH,0FFH,0FFH,0FFH
>
ASM ASSIGN BreakDisable BreakEnable BreakKill
Memory 1
Address: D:50H
D:0x50: 02 FA 03 00 00 00 00 00 00 00 00 00 00 00 00 00
D:0x60: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
D:0x70: FF FF FF FF FF FF 00 00 00 00 00 00 00 00 00 00
D:0x80: FF 07 00 00 00 00 00 10 00 00 00 00 00 00 0C 00
D:0x90: FF 00 00 00 F8 FF FE 00 00 00 00 00 00 00 00 00
D:0xA0: FF 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
D:0xB0: FF 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
D:0xC0: 03 00 00 14 00 00 00 00 00 00 00 00 00 00 00 00
D:0xD0: 01 F0 00 00 00 00 00 00 00 00 00 00 00 00 00 00
D:0xE0: 02 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
D:0xF0: FE 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
Call Stack + Locals
Memory 1
Memory 2
Address: D:70H
D:0x70: FF FF FF FF FF FF 00 00 00 00 00 00 00 00 00 00
D:0x80: FF 07 00 00 00 00 00 10 00 00 00 00 00 00 0C 00
D:0x90: FF 00 00 00 F8 FF FE 00 00 00 00 00 00 00 00 00
D:0xA0: FF 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
D:0xB0: FF 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
D:0xC0: 03 00 00 14 00 00 00 00 00 00 00 00 00 00 00 00
D:0xD0: 01 F0 00 00 00 00 00 00 00 00 00 00 00 00 00 00
D:0xE0: 02 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
D:0xF0: FE 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
D01:0x00: 00 00 00 00 00 00 00 00 00 02 01 51 01 00 00 00
D01:0x10: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
D01:0x20: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
Simulation
t1: 50.34187000 sec
L:2 C:1
CAP NUM SCRL OVR R /W


C:\S4\EE 337 Microprocessors Lab\3. Lab 3\1s_delay.uvproj - µVision [Non-Commercial Use License]
File Edit View Project Flash Debug Peripherals Tools SVCS Window Help
Registers
Register Value
Regs
r0 0x00
r1 0x00
r2 0x00
r3 0x00
r4 0x00
r5 0x00
r6 0x00
r7 0x00
Sys
a 0x00
b 0x00
sp 0x07
sp_max 0x10
PC $ C:0x0...
auxr1 0x00
dptr 0x0000
states 26448...
sec 13.22...
psw 0x00
Project Registers
Logic Analyzer
Setup... Load... Save...
Min Time 0 s
Max Time 13.22424 s
Grid 0.2 s
Zoom In Out All
Min/Max Auto Undo
Update Screen Stop Clear
Transition Prev Next
Jump to Code Trace
Signal Info
Amplitude
Timestamps Enable
Show Cycles
Cursor
Port1
1
0
18.5 us
1 --> 0
0.998556 s
4.600019 s
Port1
Mouse Pos
Reference Point
Delta
Time: 1.792018 s 0.998556 s 0.793462 s = 1.2603 Hz
Value: 0 0 0
PC $: 0xff000105 0xff000105
Disassembly
Logic Analyzer
delay_1s.asm
5 MAIN:
6 MOV P1, #01H
7 CALL delay_1sec
8 MOV P1, #00H
9 HERE: SJMP HERE
10
11 ORG 130H
12 // ******************
13 delay_1sec:
14 push 00h
15 mov r0, #100
16 h3: acall delay_10ms
17 djnz r0, h3
Command
Running with Code Size Limit: 2K
Load "C:\\S4\\EE 337 Microprocessors Lab\\3. Lab 3\\Objects\\1s_delay"
LA (Port1 & 0x00000001)
ASM ASSIGN BreakDisable BreakEnable BreakKill BreakList BreakSet BreakAccess COVERAGE
Call Stack + Locals
Name Location/Value Type
Call Stack + Locals
Memory 1
Simulation
t1: 13.22424450 sec
L:9 C:1
CAP NUM SCRL OVR R/W


e-Prayog, IIT Bombay,
Virtual Labs, An Initiative of MHRD under NMEICT
Developed at Wadhuani Electronics Lab, IIT Bombay
by Maheshuar Mangat, Geetanjali Shinde
TWI
SPI
AT89C5131A-M
RESET
BOOT
Pt-51
JHD 162A
Sending : 4
Test Successful


e-Prayog, IIT Bombay
Virtual Labs, An Initiative of MHRD under NMEICT
Developed at Wadhwani Electronics Lab, IIT Bombay
by Maheshwar Mangat, Geetanjali Shinde
AT89C5131A-M
RESET
BOOT
P1-51
JHD 162A
Counter Test....
Finished Test...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Developed at Wadhwani Electronics Lab, IIT Bombay
by Maheshwar Mangat, Geetanjali Shinde
Pt-51
RESET
BOOT
ET OK
AT89C5131A-M
JHD 162A
LCD Contrast
SPI
TWI
SW4
SW3
SW2
SW1
R6
R16
R5
R17
C8
C3
C4
P2
P2.0
P2.7
5V
3.3V
GND
SCL
SDA
SS
MISO
SCK
MOSI


Sending : 4
Finished Testing
JHD 162A
Pt-51
RESET
BOOT
AT89C5131A-M
Virtual Labs, An Initiative of MHRD under NMEICT
Developed at Wadhwani Electronics Lab, IIT Bombay
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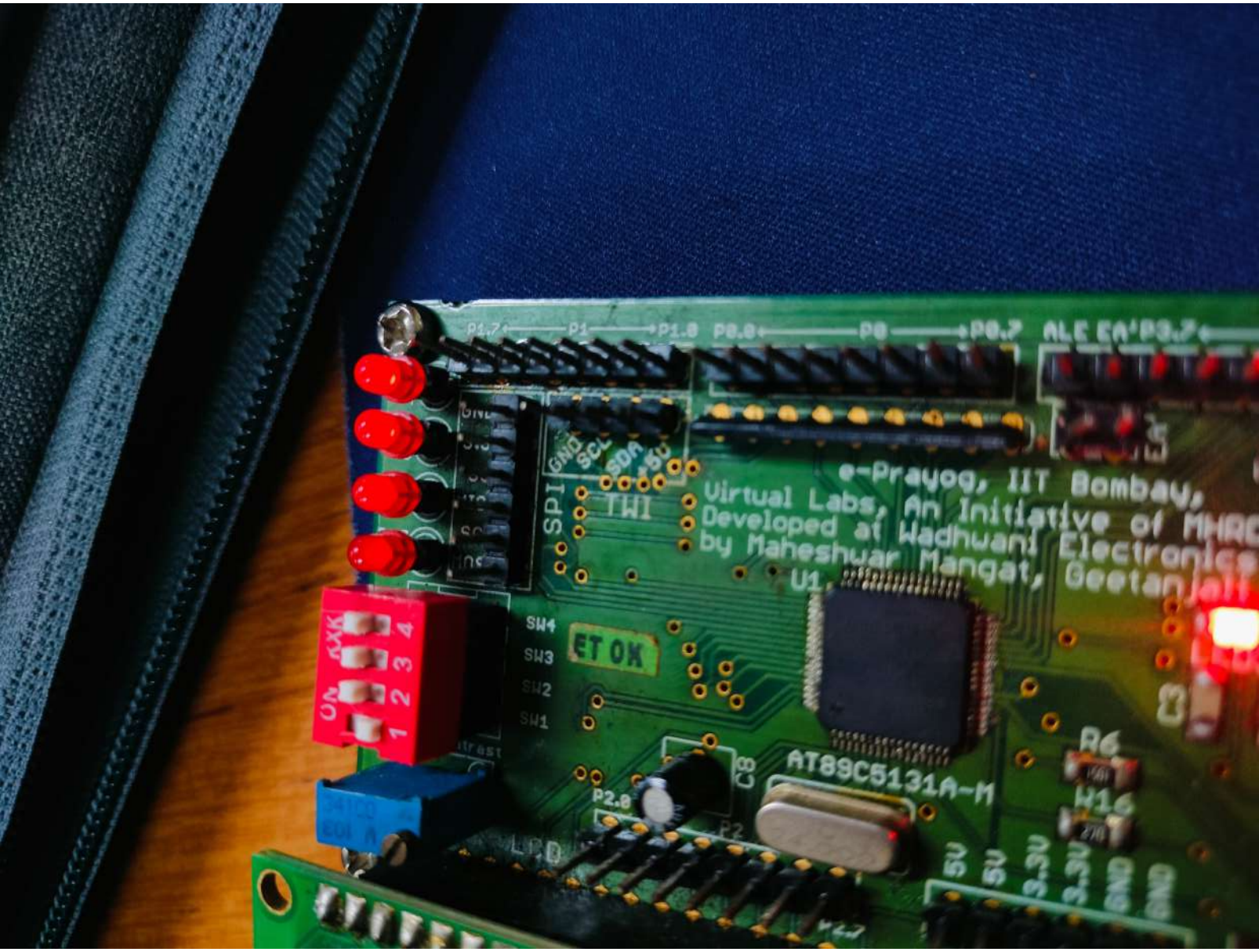
P1.7
P1
P1.0
P0.0
P0
P0.7
ALE
EA
P3.7
GND
SCL
SDA
+5V
SPI
TWI
e-Prayog, IIT Bombay,
Virtual Labs, An Initiative of MHRD
Developed at Wadhwani Electronics
by Maheshwar Mangat, Geetanjali
U1
SW4
SW3
SW2
SW1
ON
ET OK
AT89C5131A-M
P2.0
P2
R6
R16
5V
5V
3.3V
GND
GND