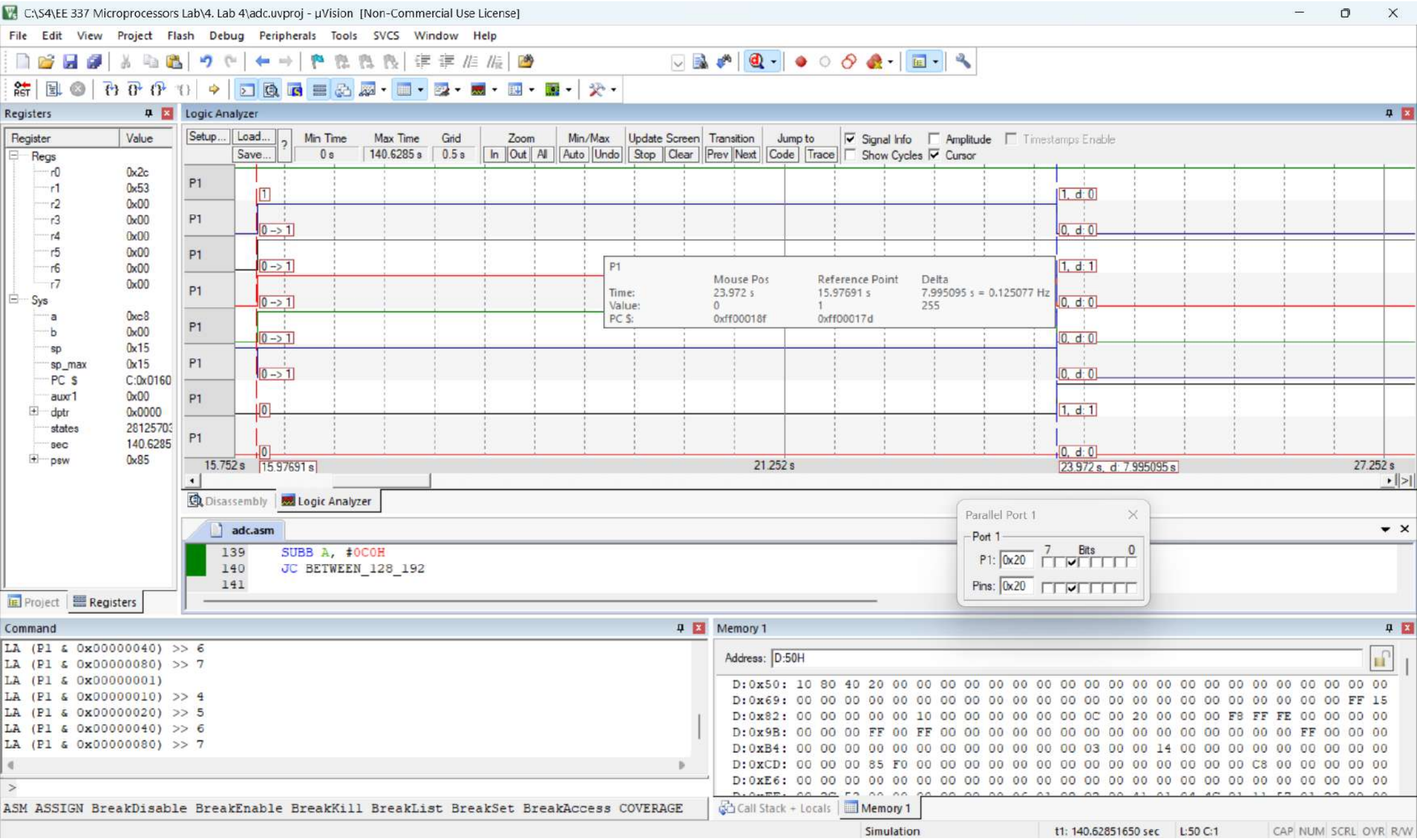
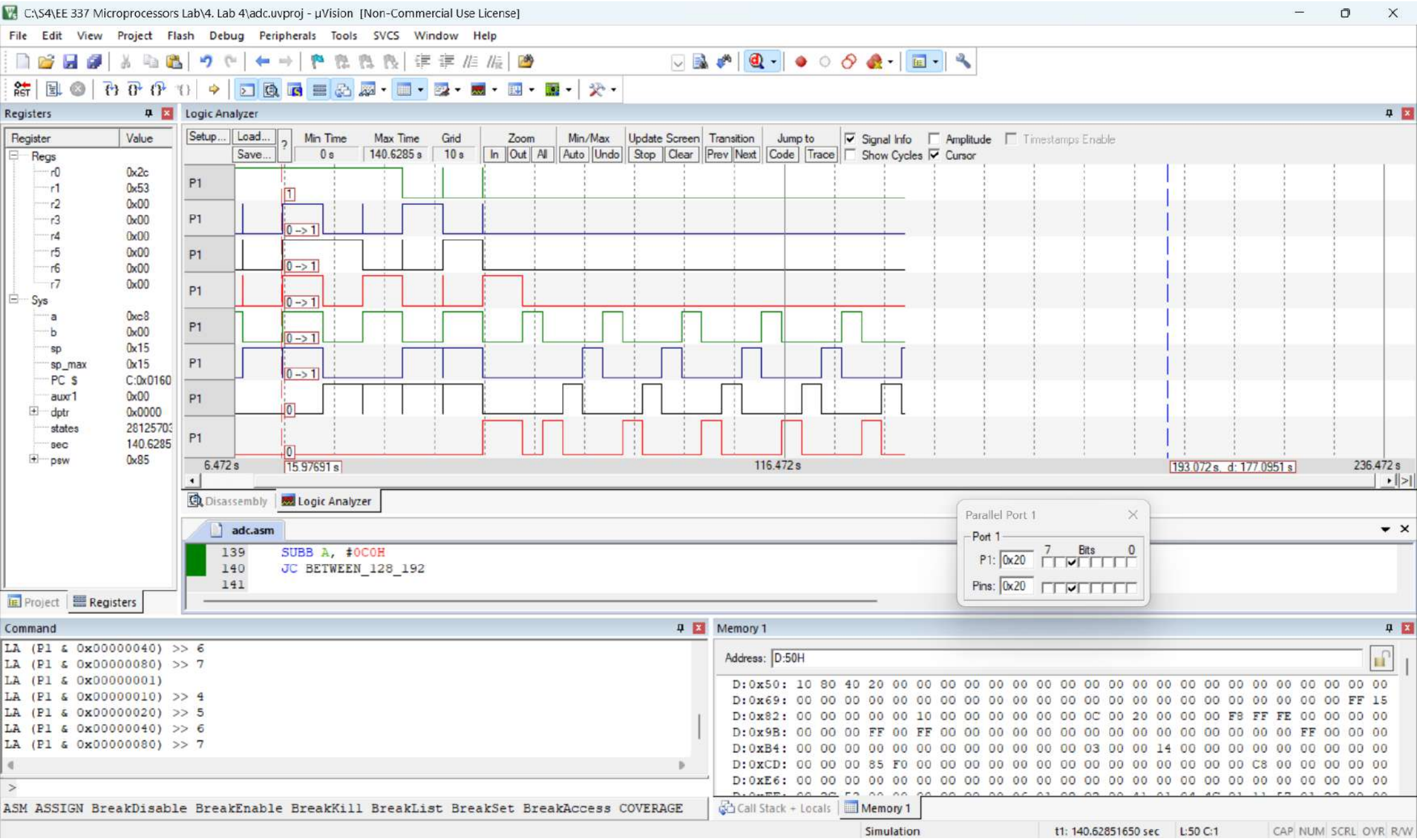

C:\S4\EE 337 Microprocessors Lab\4. Lab 4\adc.uvproj - µVision [Non-Commercial Use License]
File Edit View Project Flash Debug Peripherals Tools SVCS Window Help
Registers
Register Value
Regs
r0 0x2c
r1 0x53
r2 0x00
r3 0x00
r4 0x00
r5 0x00
r6 0x00
r7 0x00
Sys
a 0xc8
b 0x00
sp 0x15
sp_max 0x15
PC $ C:0x0160
auxr1 0x00
dptr 0x0000
states 28125703
sec 140.6285
psw 0x85
Project Registers
Logic Analyzer
Setup... Load... Save...
Min Time 0 s
Max Time 140.6285 s
Grid 0.5 s
Zoom In Out All
Min/Max Auto Undo
Update Screen Stop Clear
Transition Prev Next
Jump to Code Trace
Signal Info
Amplitude
Timestamps Enable
Show Cycles
Cursor
P1
Mouse Pos
Reference Point
Delta
Time: 23.972 s 15.97691 s 7.995095 s = 0.125077 Hz
Value: 0 1 255
PC S: 0xff00018f 0xff00017d
15.752 s
15.97691 s
21.252 s
23.972 s, d: 7.995095 s
27.252 s
Disassembly
Logic Analyzer
adc.asm
139 SUBB A, #0C0H
140 JC BETWEEN_128_192
141
Parallel Port 1
Port 1
P1: 0x20
Pins: 0x20
Bits
Command
LA (P1 & 0x00000040) >> 6
LA (P1 & 0x00000080) >> 7
LA (P1 & 0x00000001)
LA (P1 & 0x00000010) >> 4
LA (P1 & 0x00000020) >> 5
LA (P1 & 0x00000040) >> 6
LA (P1 & 0x00000080) >> 7
ASM ASSIGN BreakDisable BreakEnable BreakKill BreakList BreakSet BreakAccess COVERAGE
Memory 1
Address: D:50H
D:0x50: 10 80 40 20 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
D:0x69: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 FF 15
D:0x82: 00 00 00 00 00 10 00 00 00 00 00 00 0C 00 20 00 00 00 F8 FF FE 00 00 00 00
D:0x9B: 00 00 00 FF 00 FF 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 FF 00 00 00
D:0xB4: 00 00 00 00 00 00 00 00 00 00 00 00 03 00 00 14 00 00 00 00 00 00 00 00 00
D:0xCD: 00 00 00 85 F0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 C8 00 00 00 00 00
D:0xE6: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
Call Stack + Locals
Memory 1
Simulation
t1: 140.62851650 sec
L:50 C:1
CAP NUM SCRL OVR R/W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states 28125703
sec 140.6285
psw 0x85
Project Registers
Logic Analyzer
Setup... Load... Save...
Min Time 0 s
Max Time 140.6285 s
Grid 10 s
Zoom In Out All
Min/Max Auto Undo
Update Screen Stop Clear
Transition Prev Next
Jump to Code Trace
Signal Info Amplitude Timestamps Enable
Show Cycles Cursor
P1
0 -> 1
6.472 s
15.97691 s
116.472 s
193.072 s, d: 177.0951 s
236.472 s
Disassembly Logic Analyzer
adc.asm
139 SUBB A, #0C0H
140 JC BETWEEN_128_192
141
Parallel Port 1
Port 1
P1: 0x20
Pins: 0x20
7 Bits 0
Command
LA (P1 & 0x00000040) >> 6
LA (P1 & 0x00000080) >> 7
LA (P1 & 0x00000001)
LA (P1 & 0x00000010) >> 4
LA (P1 & 0x00000020) >> 5
LA (P1 & 0x00000040) >> 6
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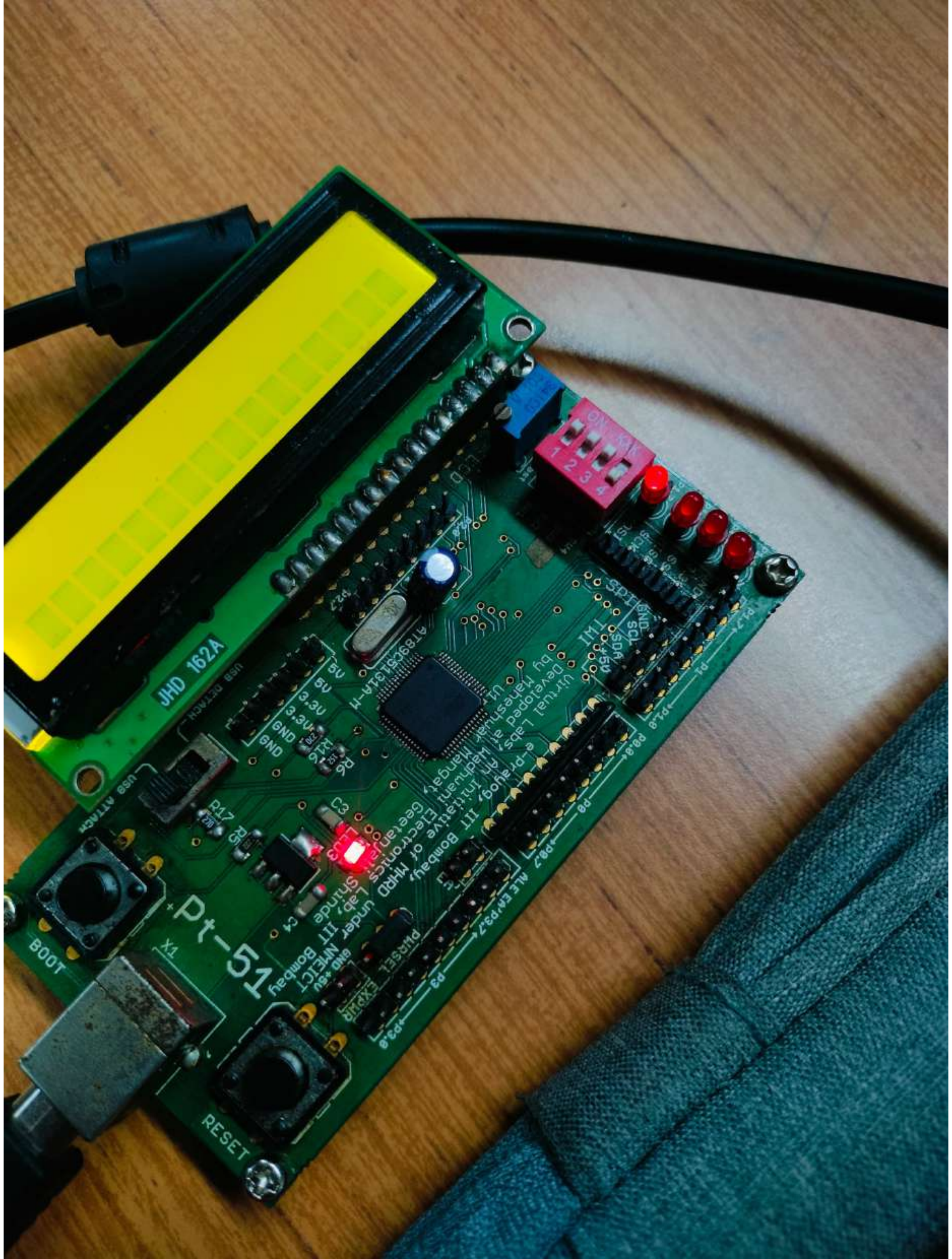
D:0x69: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 FF 15
D:0x82: 00 00 00 00 00 10 00 00 00 00 00 00 0C 00 20 00 00 00 F8 FF FE 00 00 00 00
D:0x9B: 00 00 00 FF 00 FF 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 FF 00 00 00
D:0xB4: 00 00 00 00 00 00 00 00 00 00 00 00 03 00 00 14 00 00 00 00 00 00 00 00 00
D:0xCD: 00 00 00 85 F0 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 C8 00 00 00 00 00
D:0xE6: 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
Call Stack + Locals Memory 1
Simulation t1: 140.62851650 sec L:50 C:1 CAP NUM SCRL OVR R/W


JHD 162A
Pt-51
BOOT
RESET