Mrinank Gaur

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Professional Summary

Highly motivated Electronics and Communication Engineering undergraduate with strong foundations in VLSI, FPGA, full-stack web development, digital design, and robotics. Demonstrated ability to deliver real-world solutions—from embedded systems and SoC architectures to modern MERN applications. Known for a hands-on approach, rapid learning, and collaborative project work. Passionate about system integration, automation, and building tools that bridge hardware and software.

Education

Vellore Institute of Technology *2022–2026*
Bachelor of Technology in Electronics and Communication Engineering **CGPA: 8.94/10**

The Khaitan School *2022*
Class XIIth (CBSE) **Percentage: 89.2%**

Experience

Robotics Engineer Oct 2023 – May 2025
Technocrats Robotics, VIT University *Vellore, India*
- Designed and implemented 8-axis movement control and calibration for an autonomous rover project
- Integrated Arduino and Raspberry Pi with ROS for sensor fusion, motor control, and remote communication
- Collaborated with a team to develop modular software for real-time motion planning and diagnostics

Digital Design Intern May 2024 – July 2024
Maven Silicon *Chennai, India*
- Designed and implemented an APB to AHB bridge as part of a System-on-Chip (SoC) integration project
- Utilized VHDL and Verilog for RTL design and verification of bus protocols
- Worked with Cadence tools for simulation, synthesis, and functional verification of digital designs

Projects

Single-Cycle RISC-V Processor on FPGA | *Verilog, Vivado, FPGA, RISC-V* Nov 2024 – Jan 2025
- Designed a single-cycle RISC-V processor supporting the RV32I subset on Zynq MPSoC FPGA
- Implemented datapath, control unit, and memory modules using Verilog
- Simulated and verified functionality using Xilinx Vivado
- Handled 25+ opcodes and executed each instruction in a single clock cycle
- Analyzed performance in terms of resource utilization and execution accuracy

Number Plate Recognition | *Python, OpenCV, EasyOCR, ESP32, HTML/CSS* Jan 2025 – Mar 2025
- Built a complete number plate recognition system integrating embedded hardware and computer vision
- Used ESP32-CAM to capture vehicle images and send them to a Python-based server via HTTP for processing
- Hosted a custom HTML/CSS web interface on the ESP32 to allow users to trigger image capture with a user-friendly GUI
- Applied OpenCV for image preprocessing and EasyOCR for extracting license plate text from images

MAC Unit with Pipeline Architecture | *Verilog, Cadence, CMOS Design, VLSI* Oct 2024 – Dec 2024
- Designed a performance-centric Multiply-Accumulate (MAC) unit with hyper-pipelining for DNN accelerators
- Implemented custom logic blocks like 4-bit multipliers, 8-bit adders, and deskewing registers in Verilog
- Used only full adders for delay balancing, achieving **5 GHz** clock frequency on 0.18m CMOS
- Simulated and verified design using **Cadence tools** and waveform analysis
- Improved throughput and scalability by distributing computation across parallel pipeline stages

Technical Skills

Languages: Assembly, Python, JavaScript, Java, VHDL, Verilog, C/C++, SQL (Postgres), HTML/CSS
Frameworks: React, Node.js, Express.js, Flask, FastAPI, Material-UI
Developer Tools: Quartus Prime, ModelSim, FPGA, Git, Cadence, ESP32, Raspberry Pi, Arduino, VS Code
Libraries: OpenCV, EasyOCR, Handlebars, pandas, NumPy, Matplotlib
Other Technologies: MongoDB, PostgreSQL, JWT, Nodemailer, Redis, Celery, ROS2