CSE 3203 CT 4 Assignment
Roll No: 1803175

Assignment Problem:
Build CPU based on following requirements:

1. **Word Size of CPU = 5 bit**
2. **ALU Operations = XOR, ADD, SHL**
3. **Register Number = 5**
4. **Size of RAM = 10**
5. **Word size of ISA and RAM = 16 bit**
6. **CPU Instructions = Register mode, Immediate mode, Branching(JMP,JNC)**

Solution:
Simulator Design:

1. **ALU Circuit (Top to Bottom all circuits):**
   5-bit XOR:

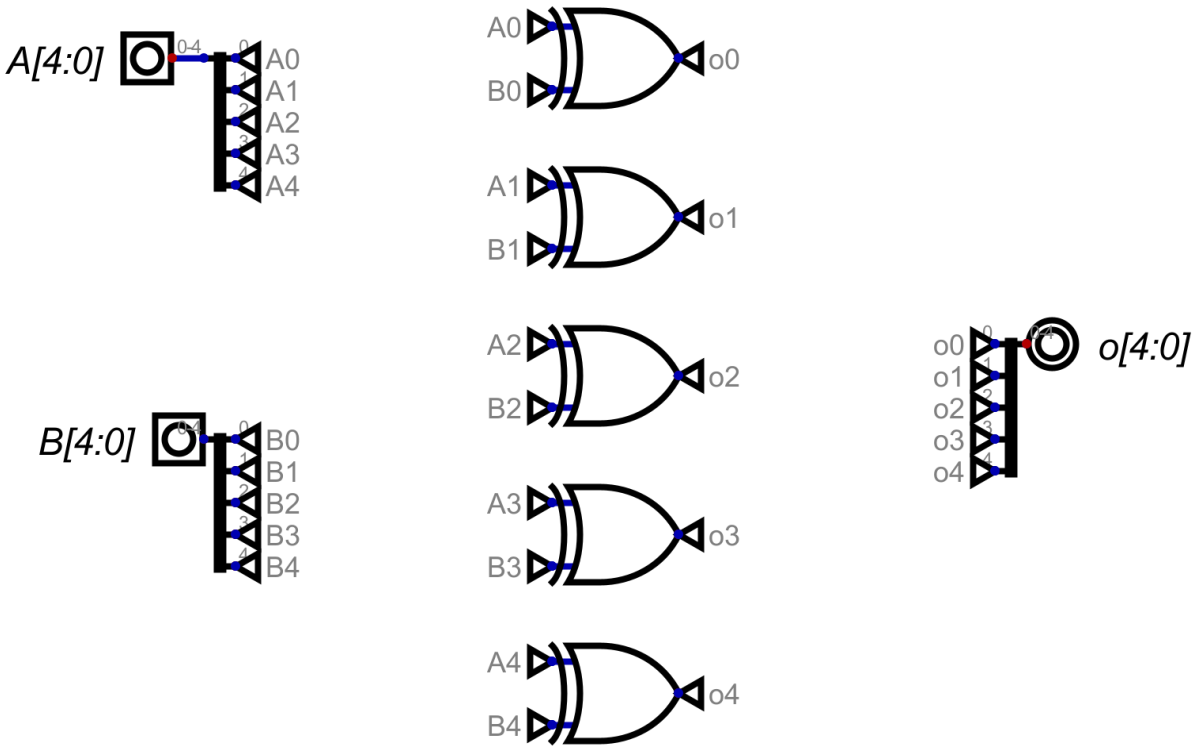


Figure: 5-bit XOR

5-bit Adder:

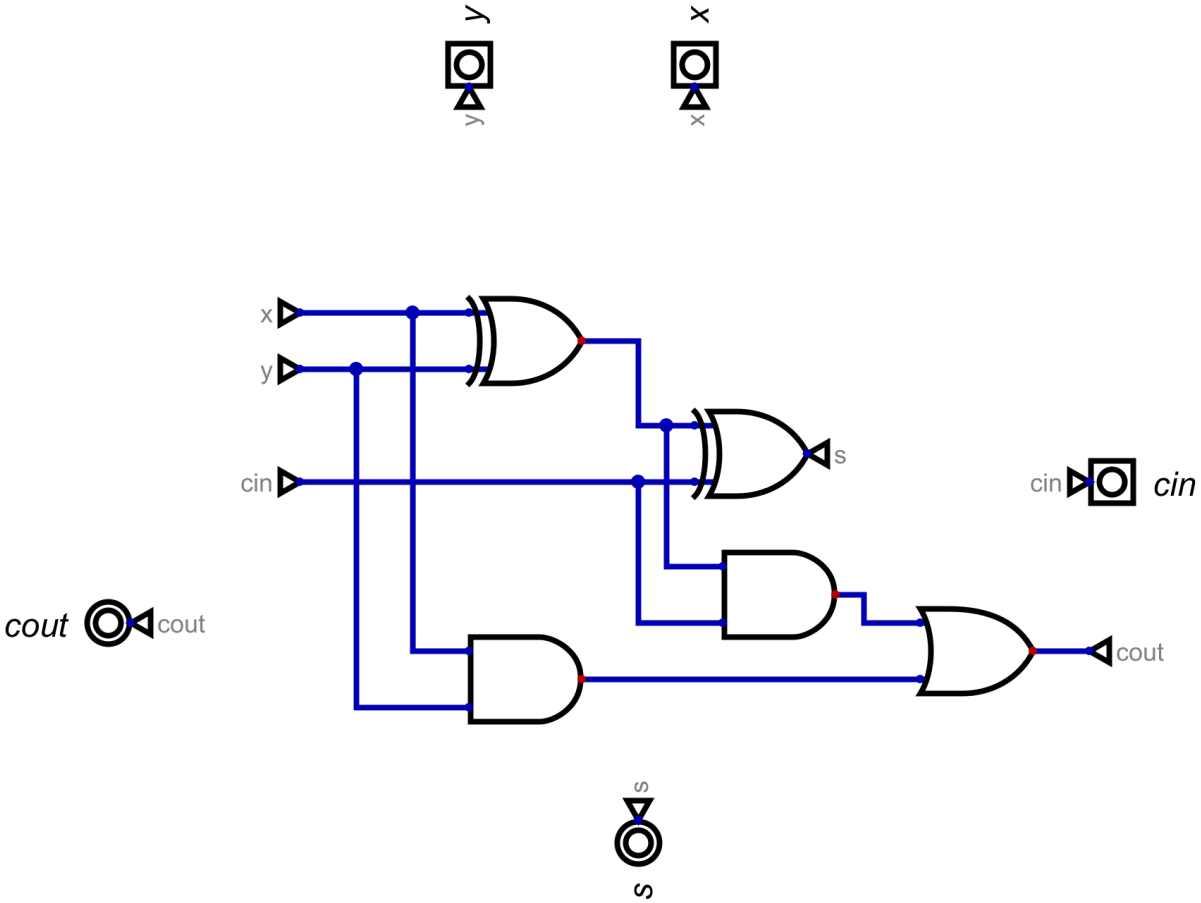


Figure: Full Adder

5-bit Full Adder:

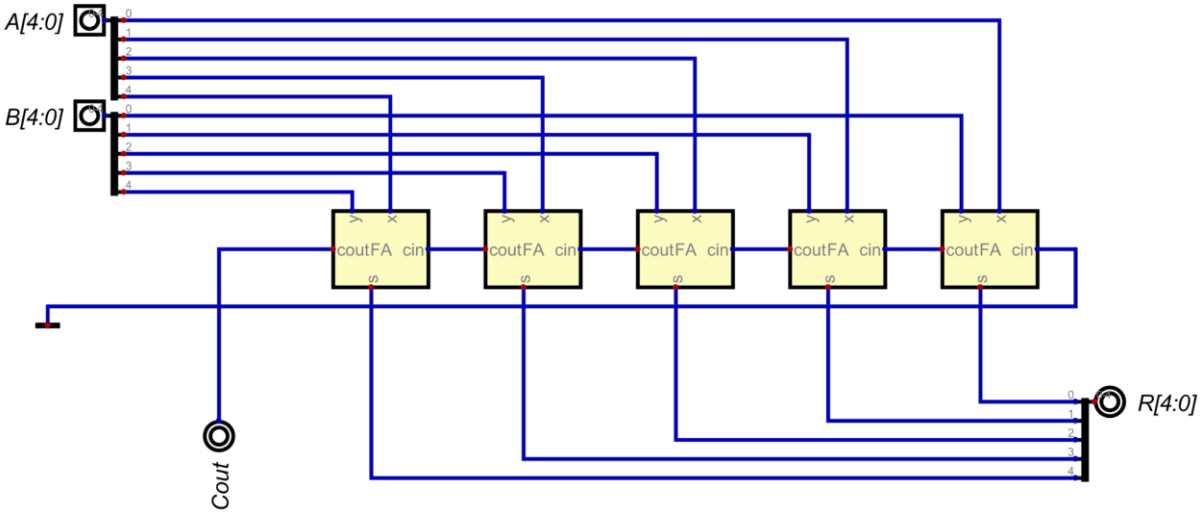


Figure: 5-bit Full Adder

5-bit SHL:

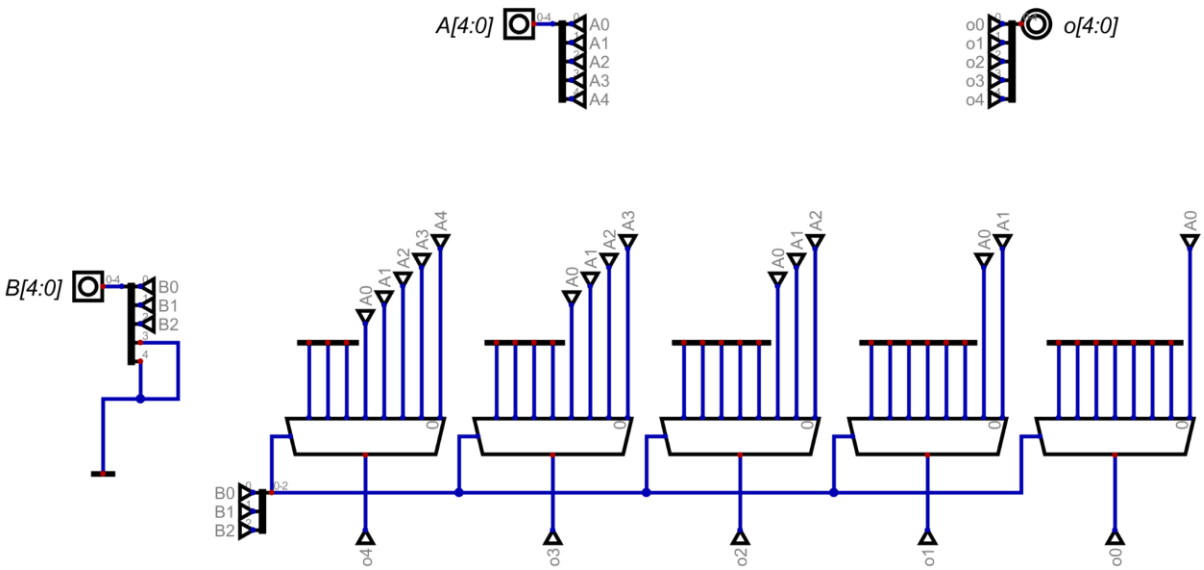


Figure: 5-bit SHL

5-bit ALU:

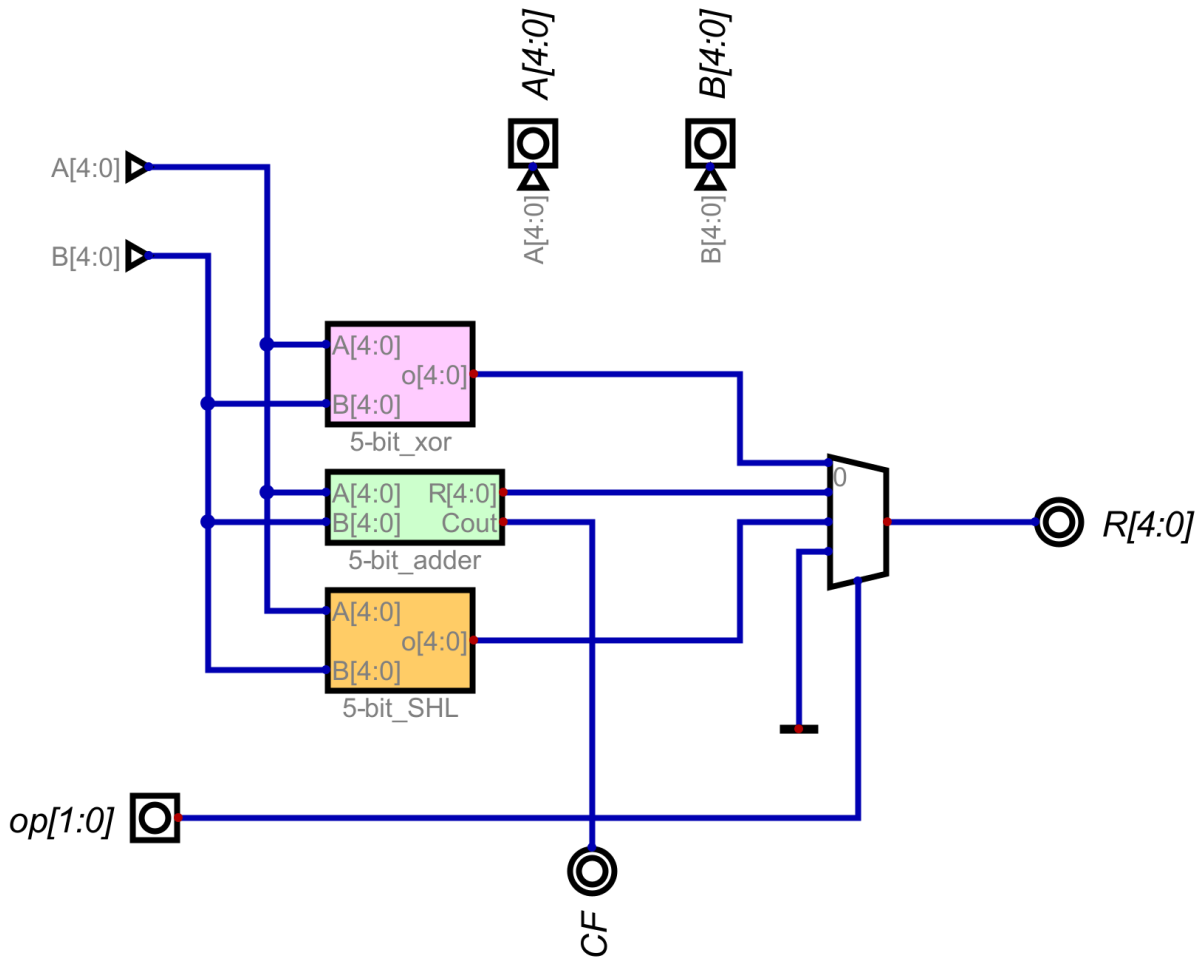


Figure: 5-bit ALU

2. **Register Set Circuit (Top to Bottom all circuits):**
   1-bit Register:

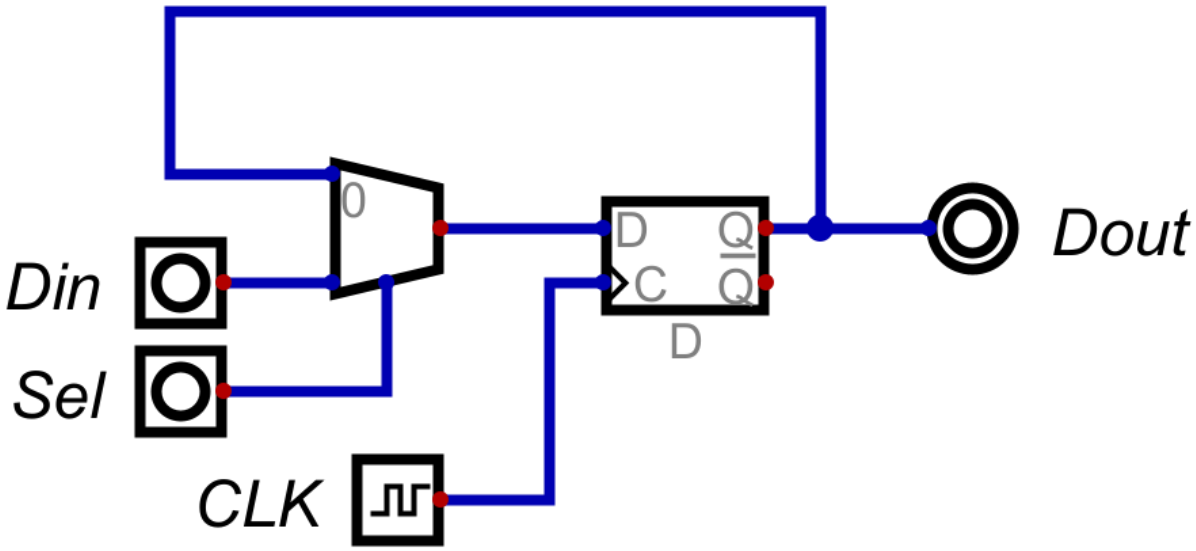


Figure: 1-bit Register

5-bit Register:

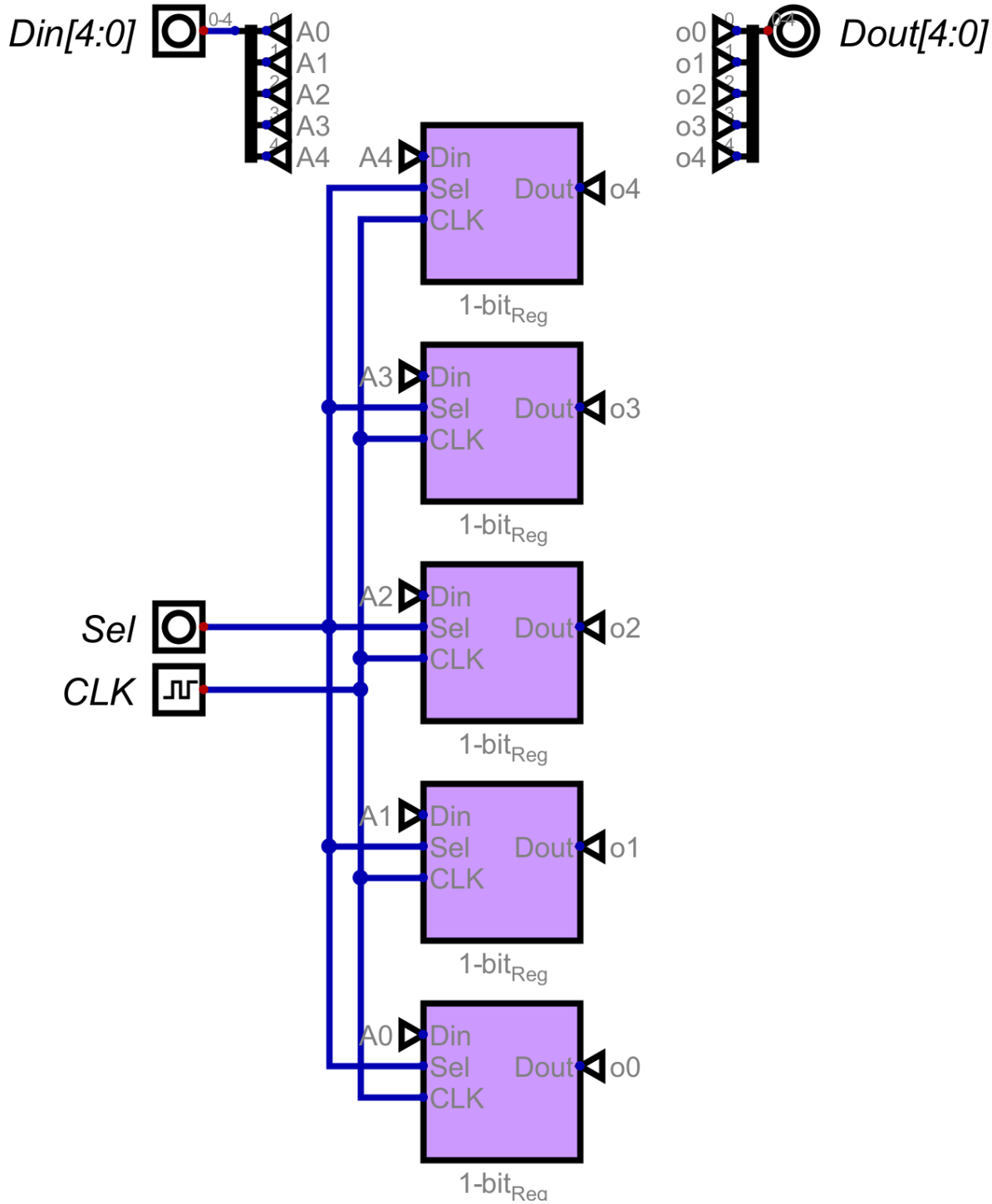


Figure: 5-bit Register

5-bit Register Set:

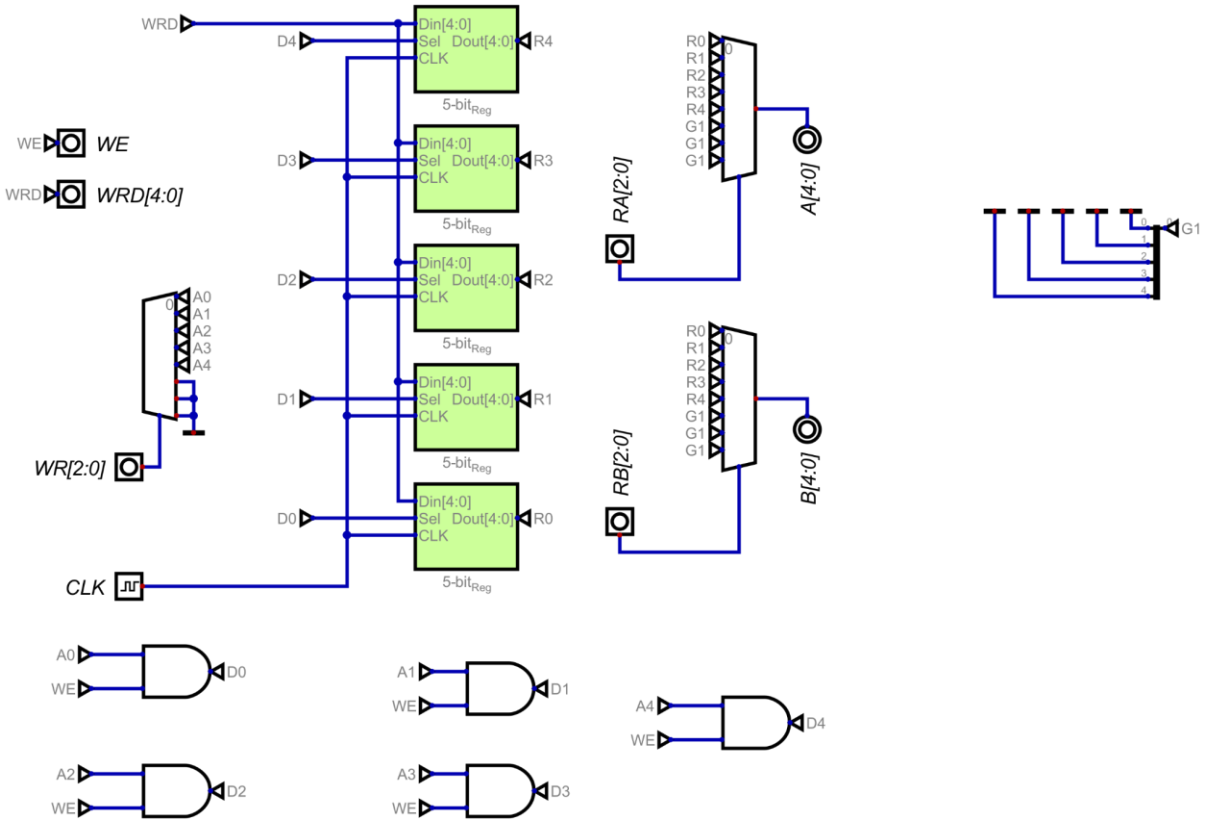


Figure: 5-bit Register Set

3. **RAM Circuit (Top to Bottom all circuits):**

1x1 RAM:

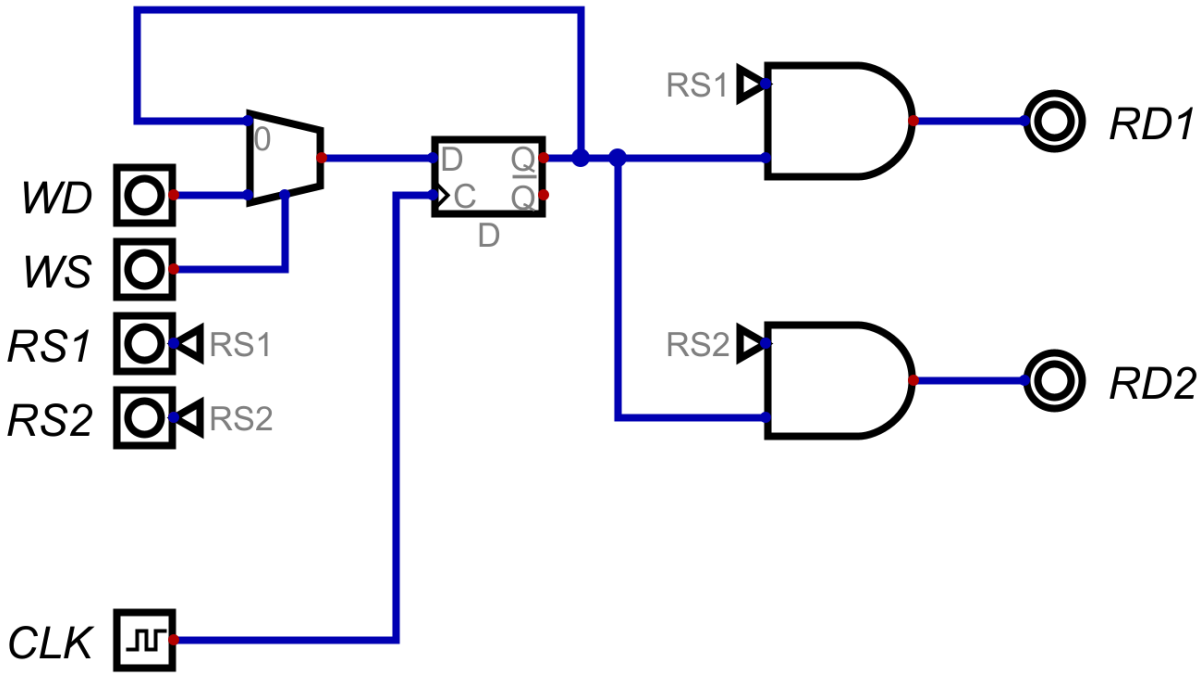


Figure: 1x1 RAM

1x16 RAM:

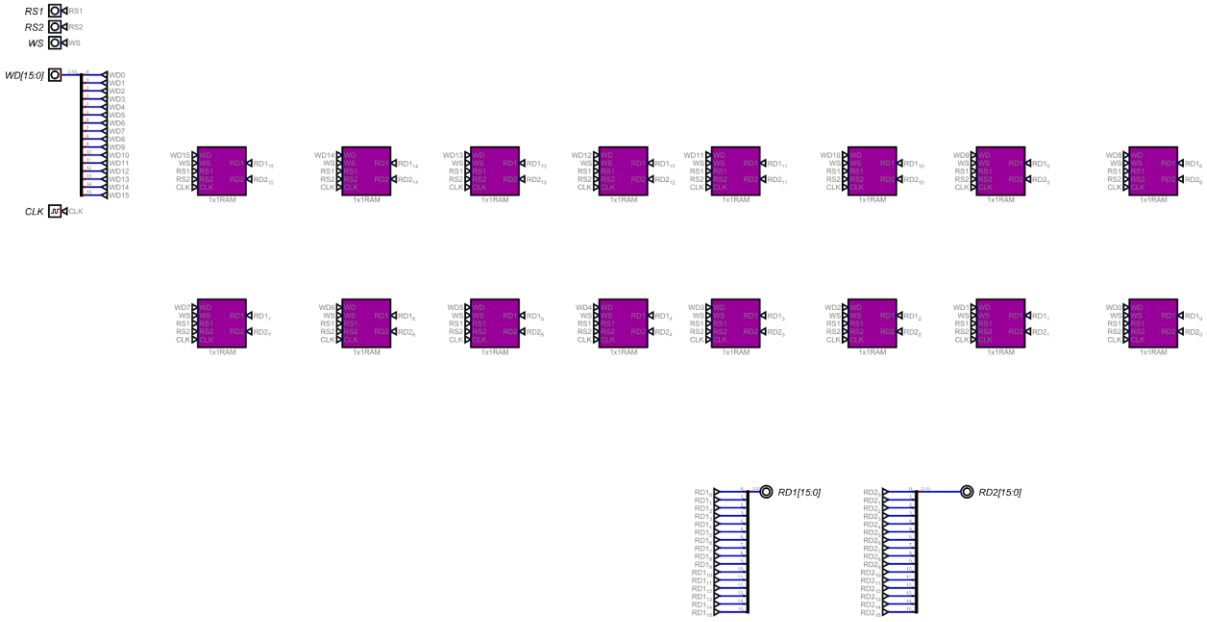


Figure: 1x16 RAM

10x16 RAM:

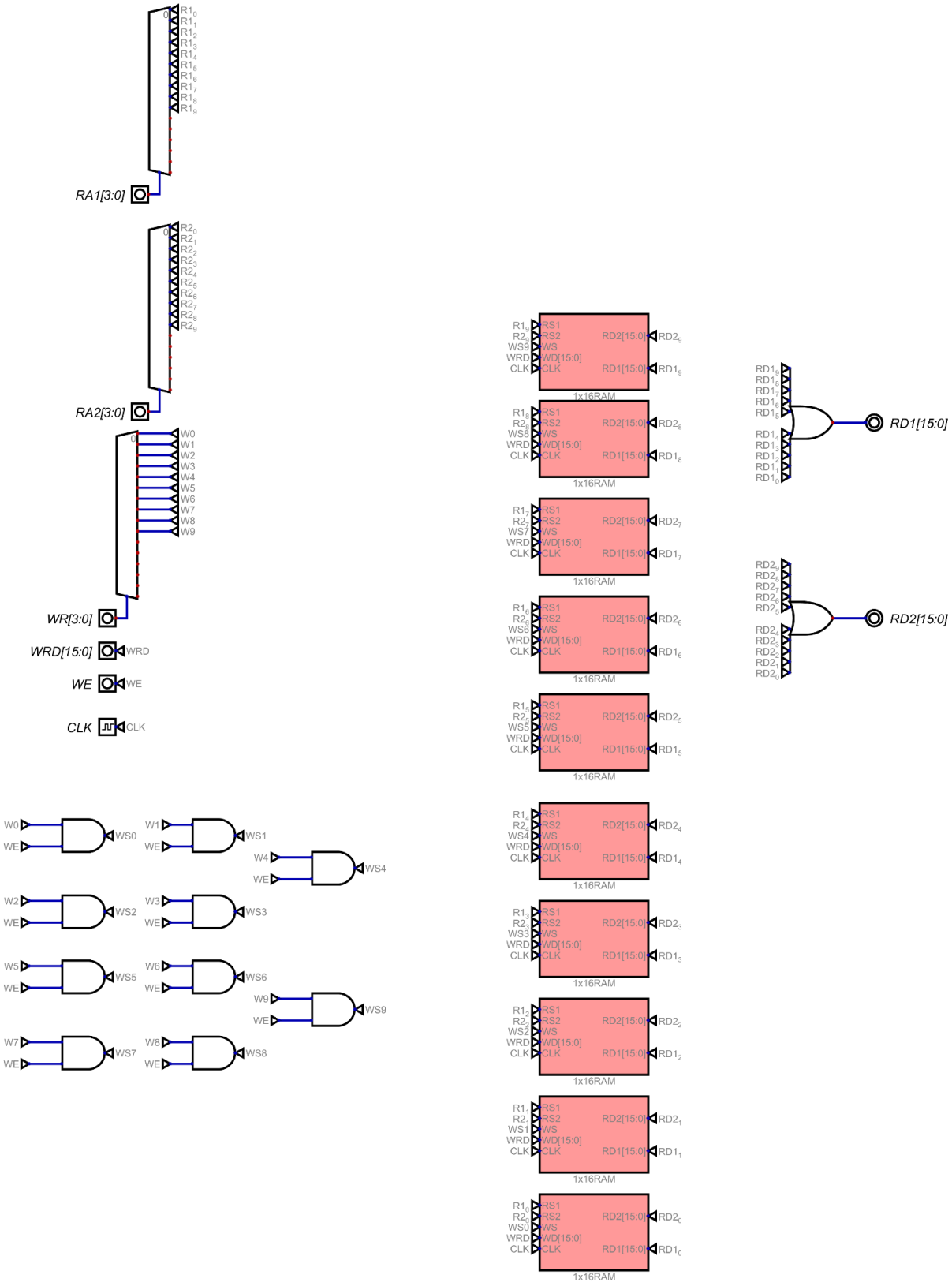


Figure: 10x16 RAM

4. ISA

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Register Mode	Mode of op.(00)		Type of op.		Reg 1			Reg 2			Don’t care					
Immediate Mode	Mode of op.(01)		Type of op.		Reg 1			Immediate Value					Don’t care			
Branching Mode	Mode of op.(10)		Type of op.		Jump Address						Don’t care					

Where, types of operations for register mode and immediate mode are-

XOR(00)

ADD(01)

SHL(10)

And types of operations for brunchong mode are-

JMP(00)

JNC(01)

5. **CPU (Top to Bottom all circuits):**
   Program counter:

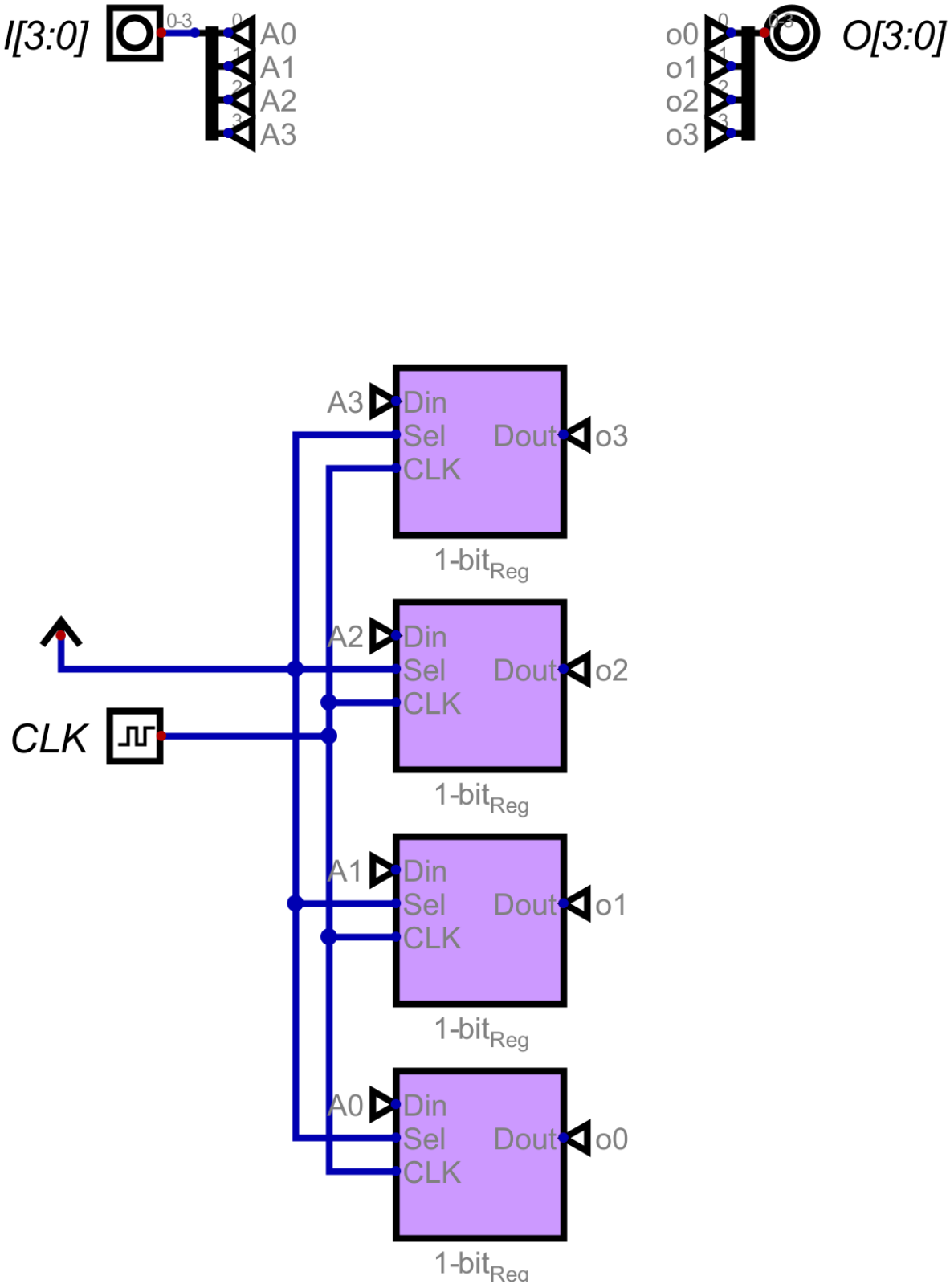


Figure: Program Counter

Program Counter Adder:

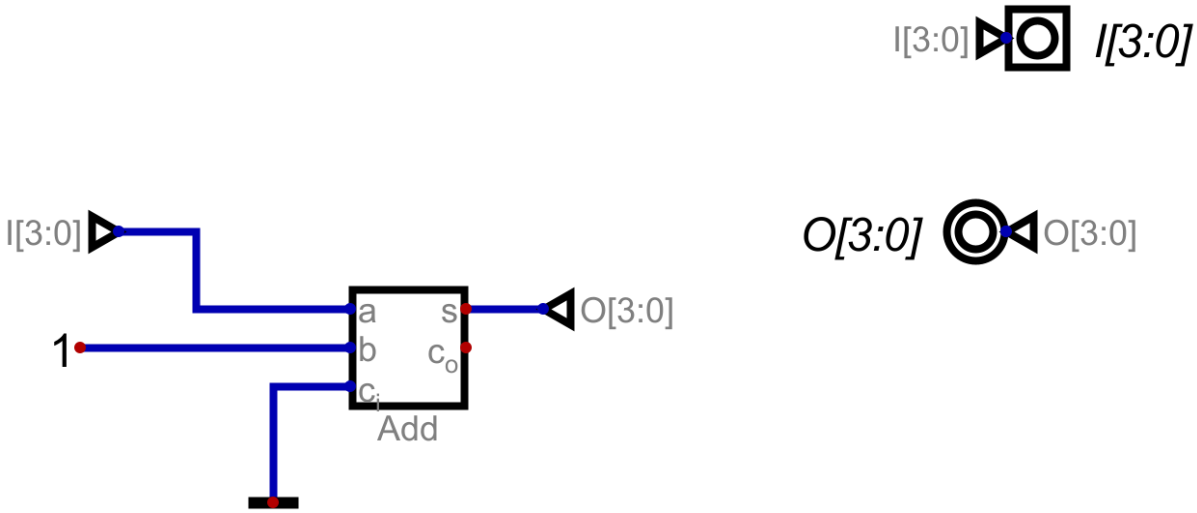


Figure: Program Counter Adder

10x16 RAM:

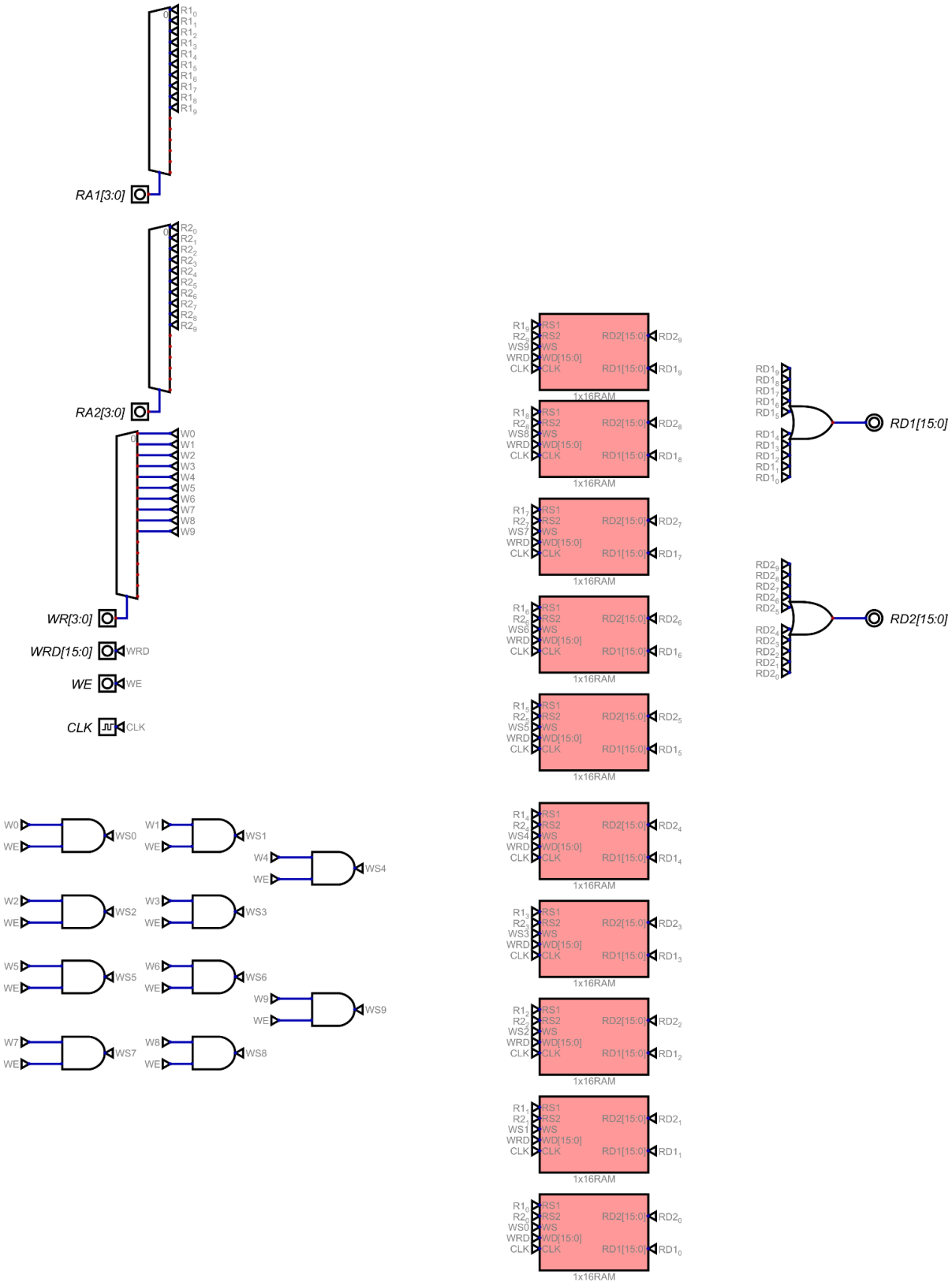


Figure: 10x16 RAM

5 bit Control Unit:

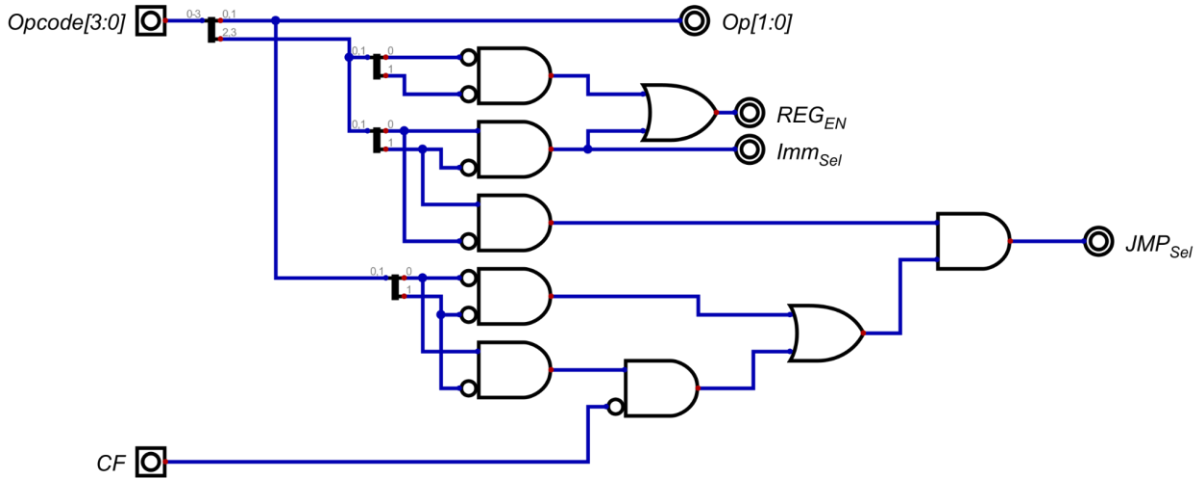
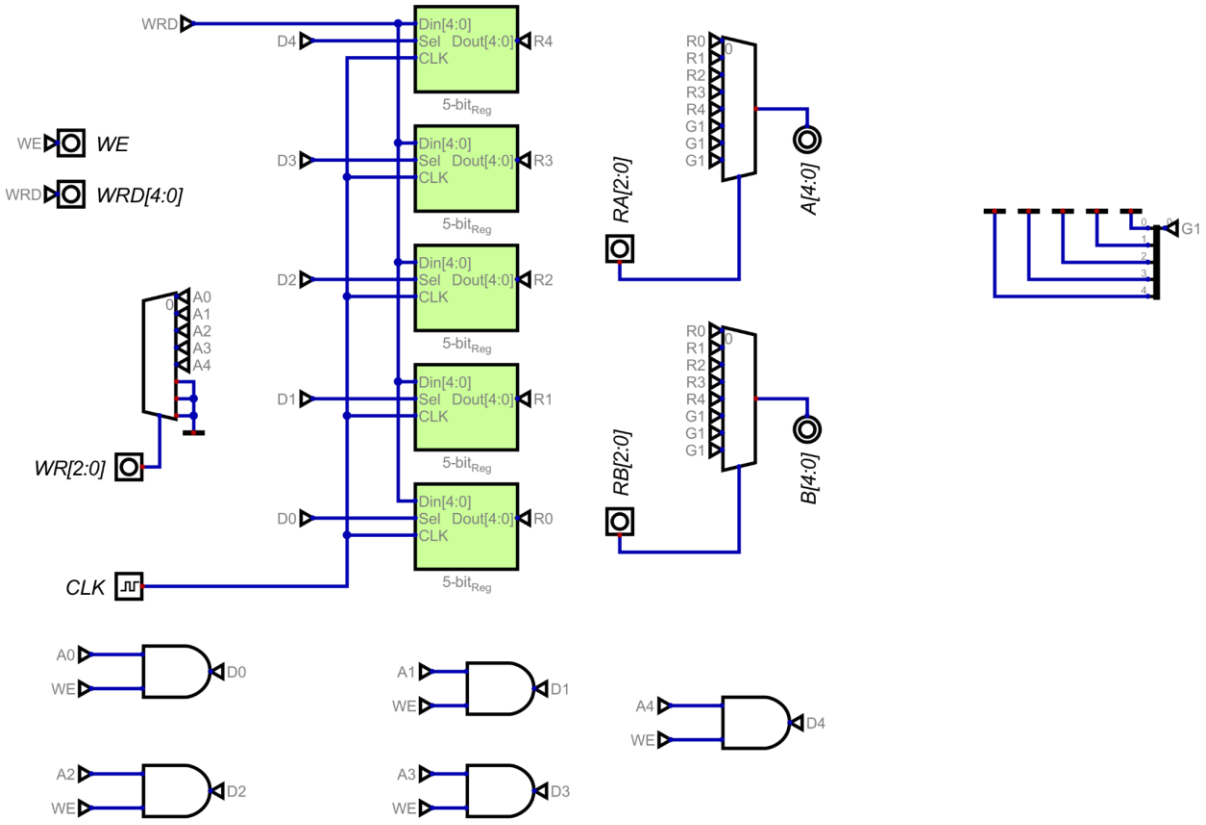


Figure: 5 bit Control Unit

5 bit Register Set:



5 bit ALU:

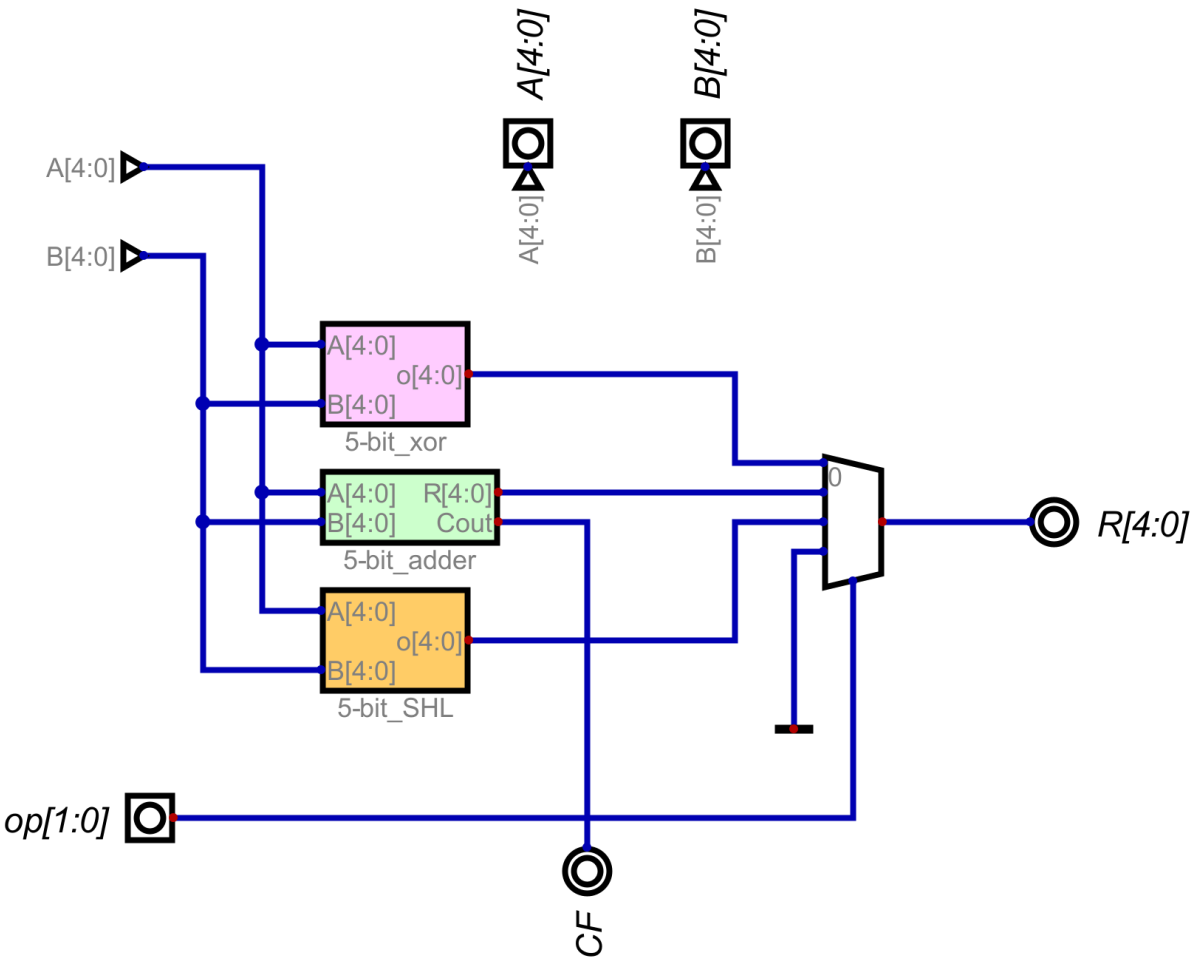


Figure: 5 bit ALU

Flag Register:

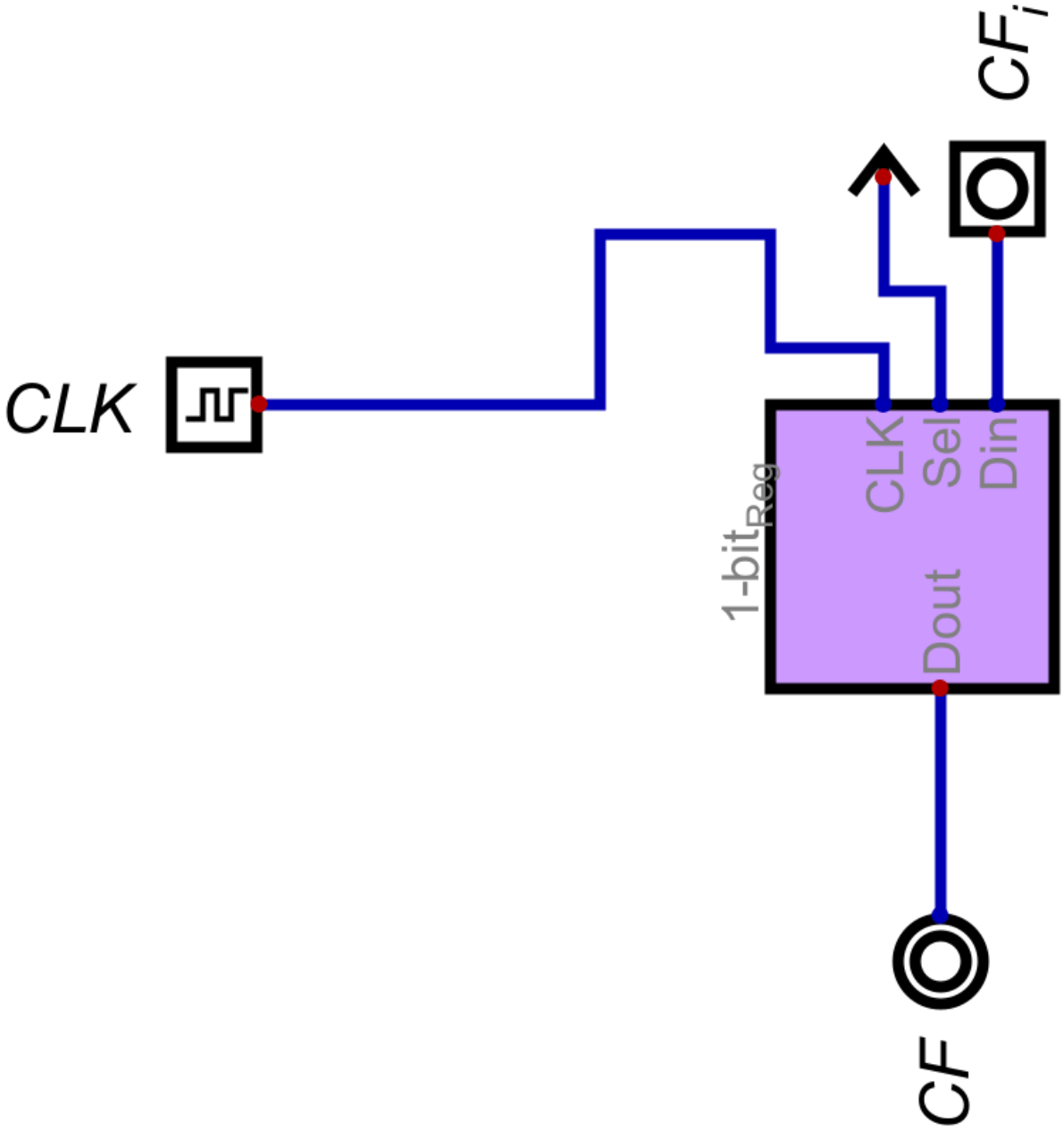


Figure: Flag Register

5 bit CPU:

Register mode: (Type of OP=00)+2bit(Type of operations)+3bit(Reg1)+3bit(Reg2)+6bit(Don't care)
Immediate mode: (Type of OP=01)+2bit(Type of operations)+3bit(Reg1)+5bit(Imm. value)+4bit(Don't care)
Branching mode: (Type of OP=10)+1bit(Type of operations)+4bit(JMP Address)+9bit(Don't Care)
XOR(OP=00) ADD(OP=01) SHL(OP=10) JMP(OP=00) JNC(op=01)
XOR R1, R1(0000001001000000)
ADD R1,5(0101001001010000)

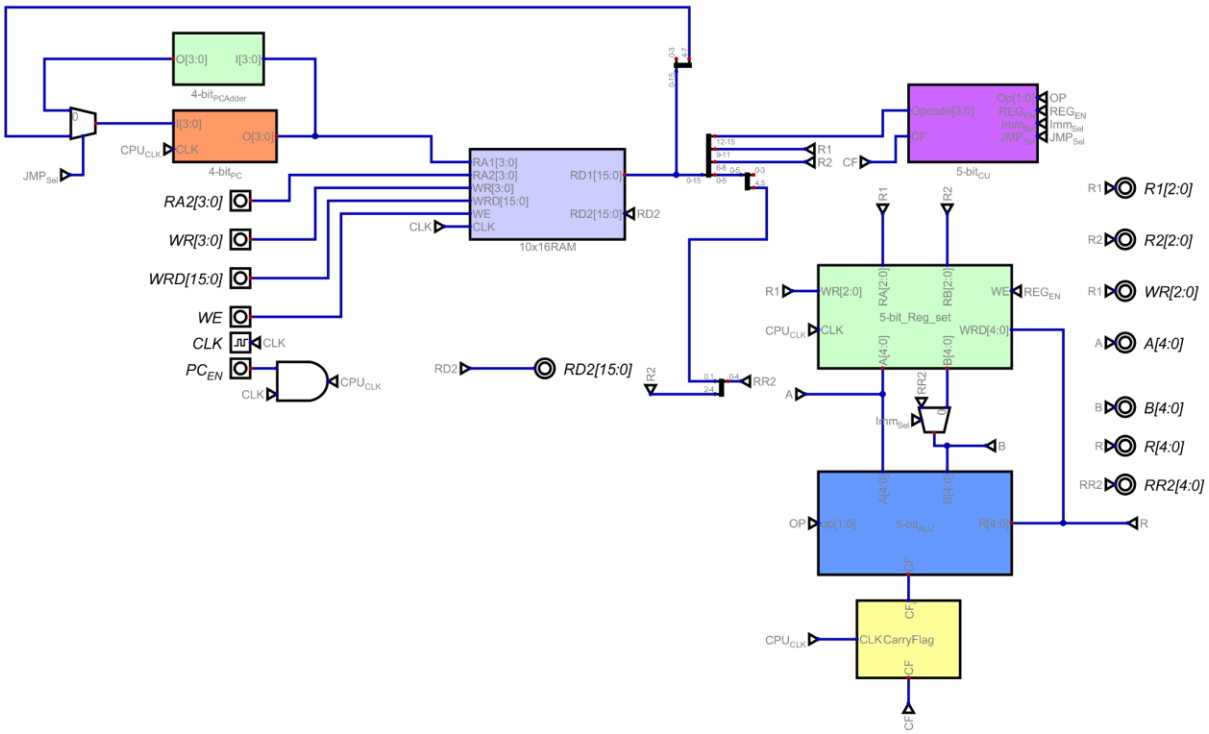


Figure: 5 bit CPU