Rajshahi University of Engineering and Technology

Course Title: Sessional Based on CSE 2203

Course Code: CSE 2204

Lab Report - 05

Submitted to

Md. Zahirul Islam
Lecturer,
Computer Science and Engineering, RUET

Submitted by

Mrittika Roy
Roll: 1803175
Section: C
Computer Science and Engineering, RUET

Date of Submission: 12.07.2021

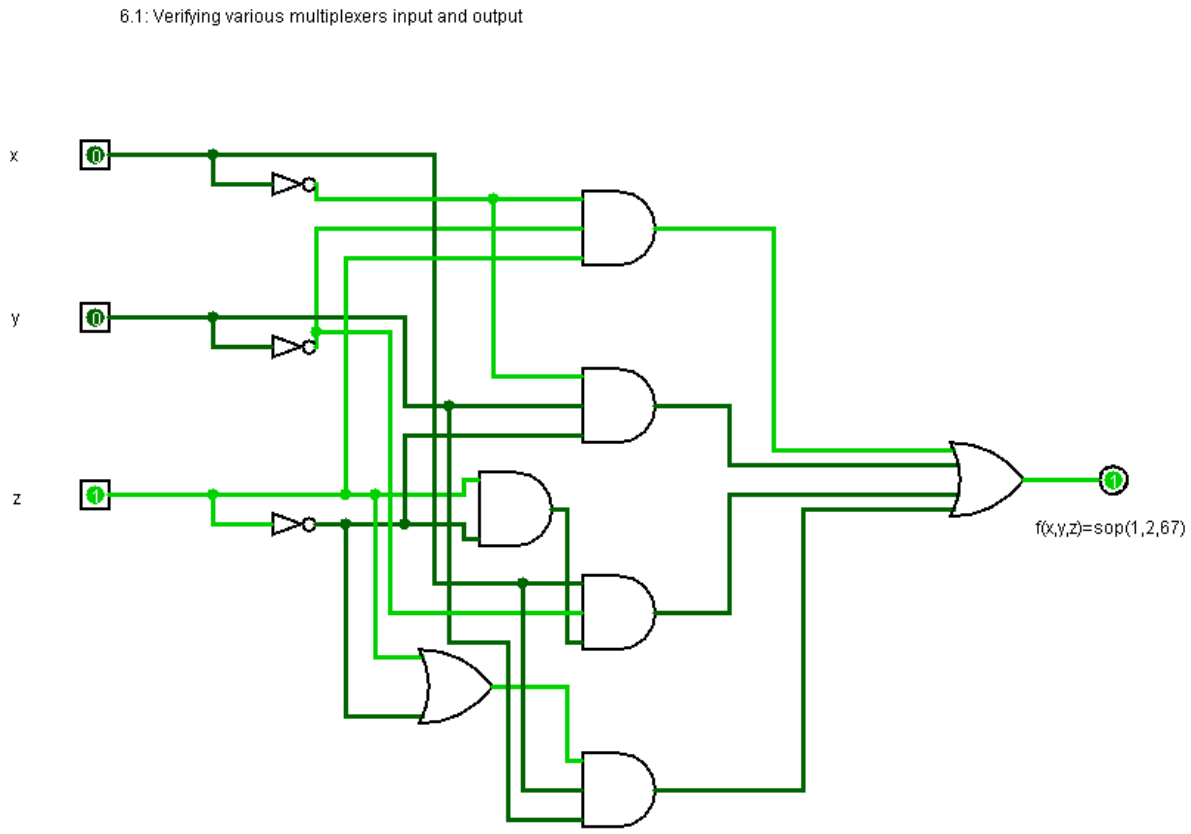
6.1

1. Name of the Experiment:
Verifying Various Multiplexers Input and Output.

2. Objectives:
- To know about multiplexers
- To know how to implement a multiplexer circuit
- To verify its input and output

3. Theory:
A multiplexer is a combinational circuit that selects an input from several inputs then it is transmitted in the form of a single line. An alternative name of the multiplexer is MUX or data selector.
In this experiment, we will implement a multiplexer of f(x,y,z) = SOP(1,2,6,7),where x is MSB and z is LSB.

4. Experimental Analysis:
i. Circuit:



ii. Truth Table:

x	y	z	f
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

5. Conclusion:

From the above experiment, it is verified that the implemented circuit shows the expected output as the truth table.

6.2

1. Name of the Experiment:
Verifying Various Encoders Input and Output.

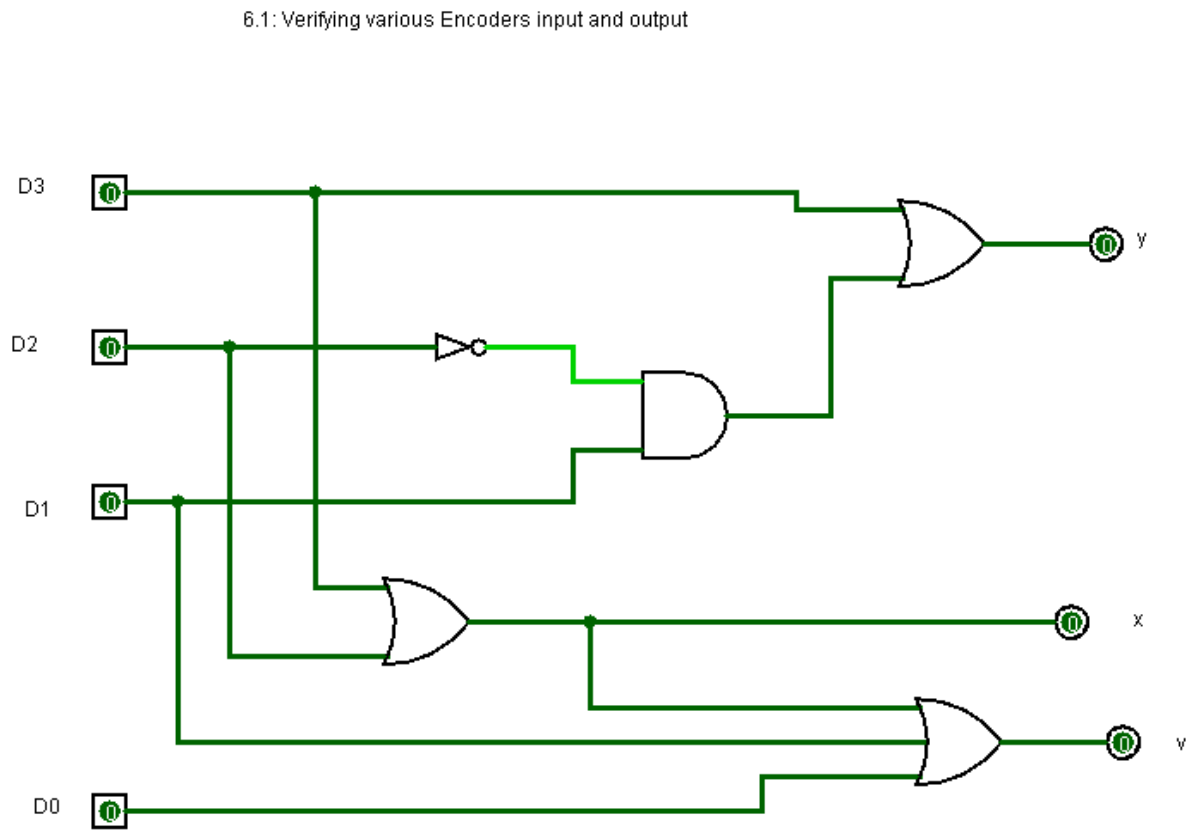
2. Objectives:
- To know about encoders
- To know how to implement an encoder
- To verify its input and output

3. Theory:
An encoder is a combinational circuit that converts binary information in the form of a 2^N input lines into N output lines, which represent N bit code for the input. For simple encoders, it is assumed that only one input line is active at a time.
In this experiment, we will implement a 4-input priority encoder.Let D0,D1,D2 and D3 are the input variables, x and y are the output variables and v in the validity pin. If v=0, the output is not valid and if v=1, the output is valid. The expressions for its outputs are:
x = D2 + D3
y = D3 + D1D2'
v = D0 + D1 + D2 + D3
The truth table for 4-input encoder is:

D0	D1	D2	D3	x	y	v
0	0	0	0	x	x	0
1	0	0	0	0	0	1
x	1	0	0	0	0	1
x	x	1	0	1	0	1
x	x	x	1	1	1	1

4. Experimental Analysis:

i. Circuit:



ii. Truth Table:

D0	D1	D2	D3	x	y	v
0	0	0	0	x	x	0
1	0	0	0	0	0	1
x	1	0	0	0	0	1
x	x	1	0	1	0	1
x	x	x	1	1	1	1

5. Conclusion:

From the above experiment, it is verified that the implemented circuit shows the expected output as the truth table.