Rajshahi University of Engineering and Technology

Course Title: Sessional Based on CSE 2203

Course Code: CSE 2204

Lab Report - 02

Submitted to

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3.1

1. Name of the Experiment:
Verify the Basic NOR gate (up to 5 Inputs) for all input combinations.

2. Objectives:

- To know about NOR gate
- To generate the truth table of NOR gate
- To generate the logic circuit of NOR gate

3. Theory:
The NOR gate is a combination of the OR gate and a NOT gate connected together in series. The logical expression for NOR gate for 2 inputs is F = ~(X+Y). The output of NOR gate is 1/on when all inputs are 0. Otherwise if any of the input is 1/ on, the output will be 0. This is one of the universal gates. This gate can be used to implement any basic or complex gate.

4. Experimental Result Analysis:

i. Circuit:

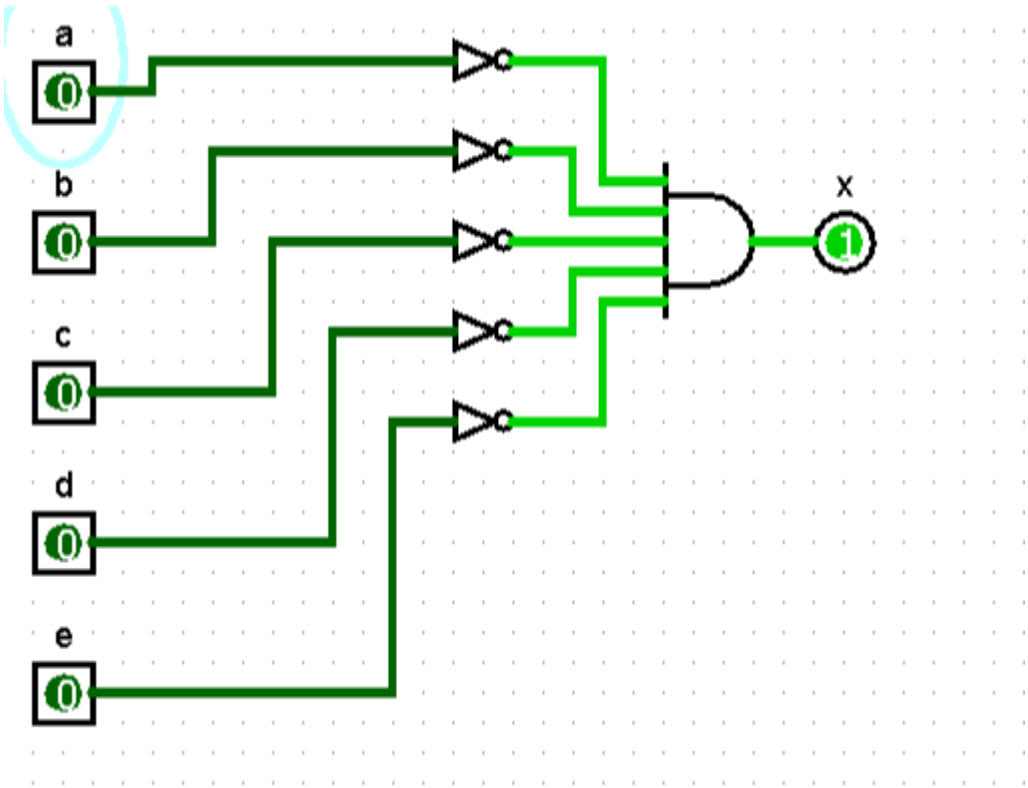

Figure: Circuit Diagram of NOR gate (When the output is on)

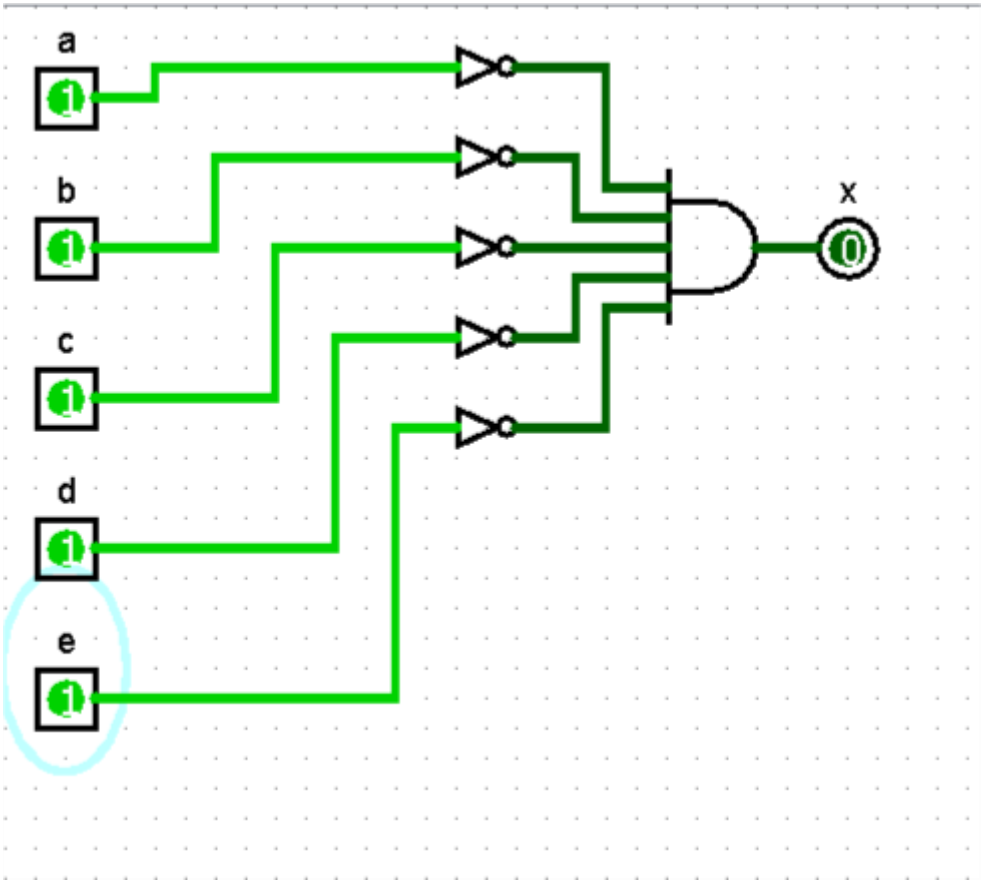

Figure: Circuit Diagram of NOR gate (When the output is off)

ii. Truth Table:

a	b	c	d	e	x
0	0	0	0	0	1
0	0	0	0	1	0
0	0	0	1	0	0
0	0	0	1	1	0
0	0	1	0	0	0
0	0	1	0	1	0
0	0	1	1	0	0
0	0	1	1	1	0
0	1	0	0	0	0
0	1	0	0	1	0
0	1	0	1	0	0
0	1	0	1	1	0
0	1	1	0	0	0
0	1	1	0	1	0
0	1	1	1	0	0
0	1	1	1	1	0
1	0	0	0	0	0
1	0	0	0	1	0
1	0	0	1	0	0
1	0	0	1	1	0
1	0	1	0	0	0
1	0	1	0	1	0
1	0	1	1	0	0
1	0	1	1	1	0
1	1	0	0	0	0
1	1	0	0	1	0
1	1	0	1	0	0
1	1	0	1	1	0
1	1	1	0	0	0
1	1	1	0	1	0
1	1	1	1	0	0
1	1	1	1	1	0

5. Conclusion:

From the above experiment, we came to a conclusion that the output of the 5 inputs NOR gate is 1 when all the inputs are 0 and the output is 0 when one or more outputs are 1.

3.2

1. Name of the Experiment:
Verify the Basic NAND gate (up to 5 Inputs) for all input combinations.

2. Objectives:

- To know about NAND gate
- To generate the truth table of NAND gate
- To generate the logic circuit of NAND gate

3. Theory:
The NAND gate is a combination of the AND gate and a NOT gate connected together in series. The logical expression for NAND gate for 2 inputs is F = ~(XY). The output of NAND gate is 0/off when all inputs are 1. Otherwise if any of the input is 0/ off, the output will be 1. This is another universal gate. This gate can be used to implement any basic or complex gate.

4. Experimental Result Analysis:

i. Circuit:

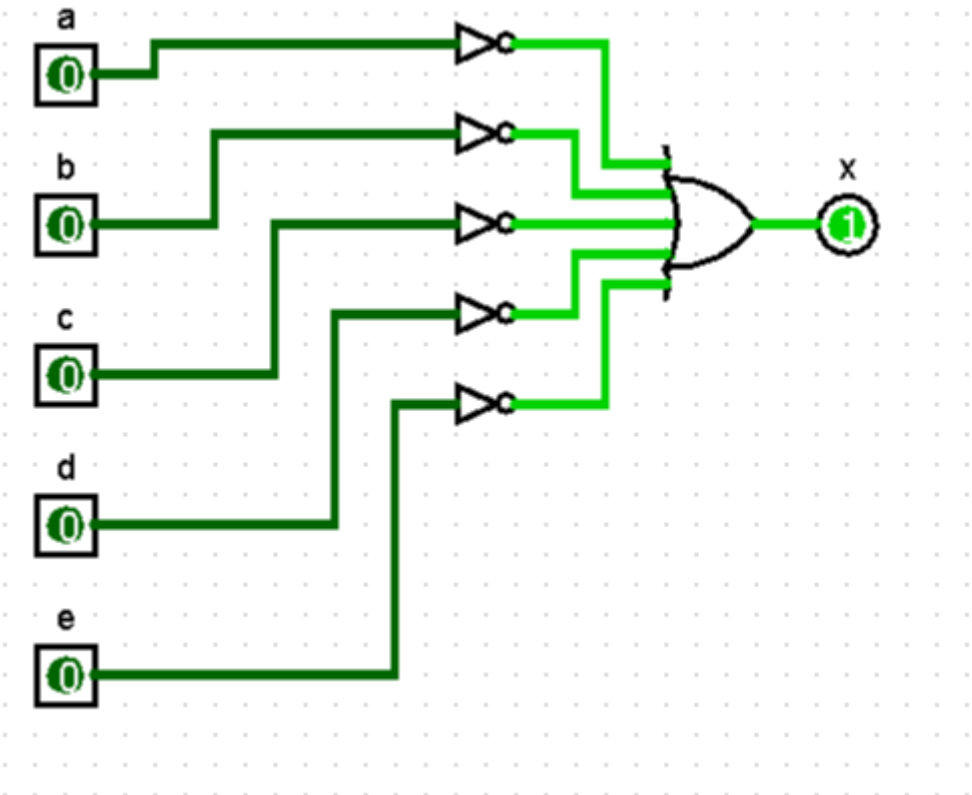

Figure: Circuit Diagram of NAND Gate (When the the output is on)

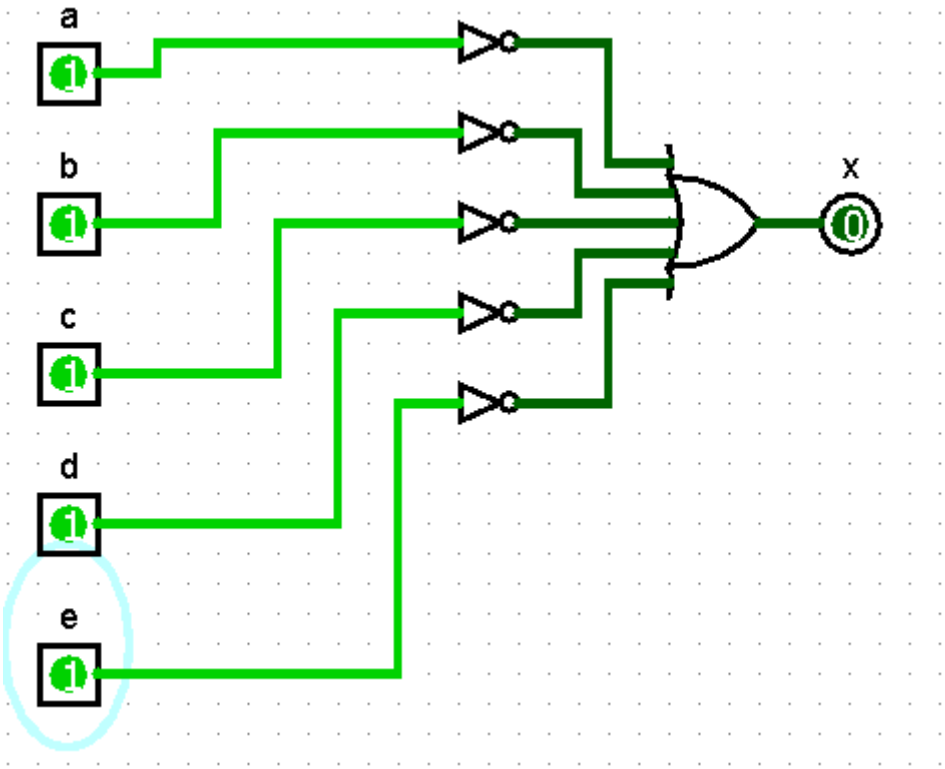

Figure: Circuit Diagram of NAND Gate (When the output is off)

ii. Truth Table:

a	b	c	d	e	x
0	0	0	0	0	1
0	0	0	0	1	1
0	0	0	1	0	1
0	0	0	1	1	1
0	0	1	0	0	1
0	0	1	0	1	1
0	0	1	1	0	1
0	0	1	1	1	1
0	1	0	0	0	1
0	1	0	0	1	1
0	1	0	1	0	1
0	1	0	1	1	1
0	1	1	0	0	1
0	1	1	0	1	1
0	1	1	1	0	1
0	1	1	1	1	1
1	0	0	0	0	1
1	0	0	0	1	1
1	0	0	1	0	1
1	0	0	1	1	1
1	0	1	0	0	1
1	0	1	0	1	1
1	0	1	1	0	1
1	0	1	1	1	1
1	1	0	0	0	1
1	1	0	0	1	1
1	1	0	1	0	1
1	1	0	1	1	1
1	1	1	0	0	1
1	1	1	0	1	1
1	1	1	1	0	1
1	1	1	1	1	0

5. Conclusion:

From the above experiment, we came to a conclusion that the output of the 5 inputs NAND gate is 0 when all the inputs are 1 and the output is 1 when one or more outputs are 1.

3.3

1. Name of the Experiment:
Verify the Basic XOR gate (up to 5 Inputs) for all input combinations.

2. Objectives:
- To know about XOR gate
- To generate the truth table of XOR gate
- To generate the logic circuit of XOR gate

3. Theory:
The XOR gate is also called Exclusive OR. The output of XOR gate is 1/on when the odd number of inputs are 1/on otherwise the output is 0/off. The logical expression of two inputs XOR gate is represented as F = (~A)B + A(~B).

4. Experimental Analysis:

i. Circuit:

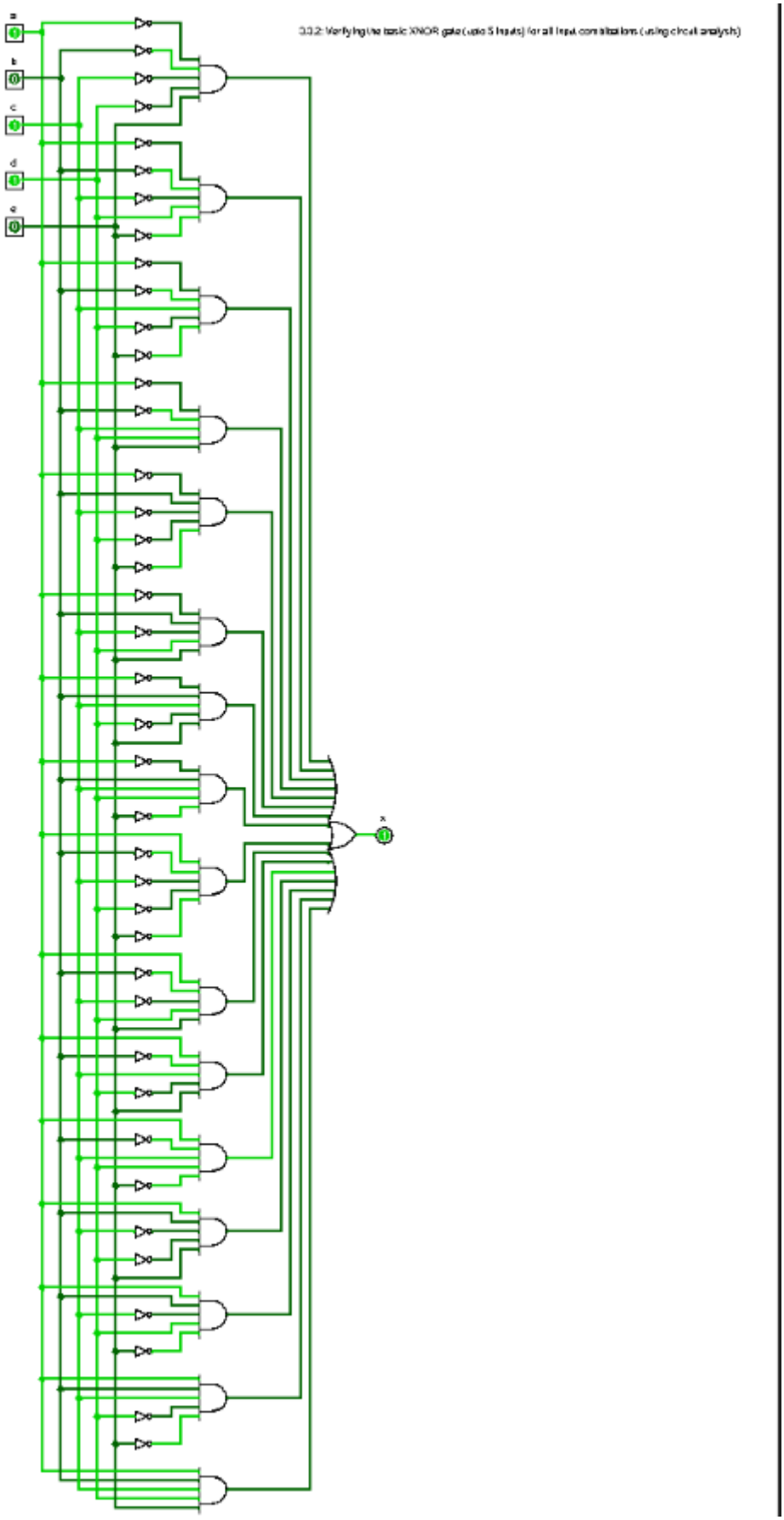

Figure: Circuit Diagram of XOR Gate(When the output is on)

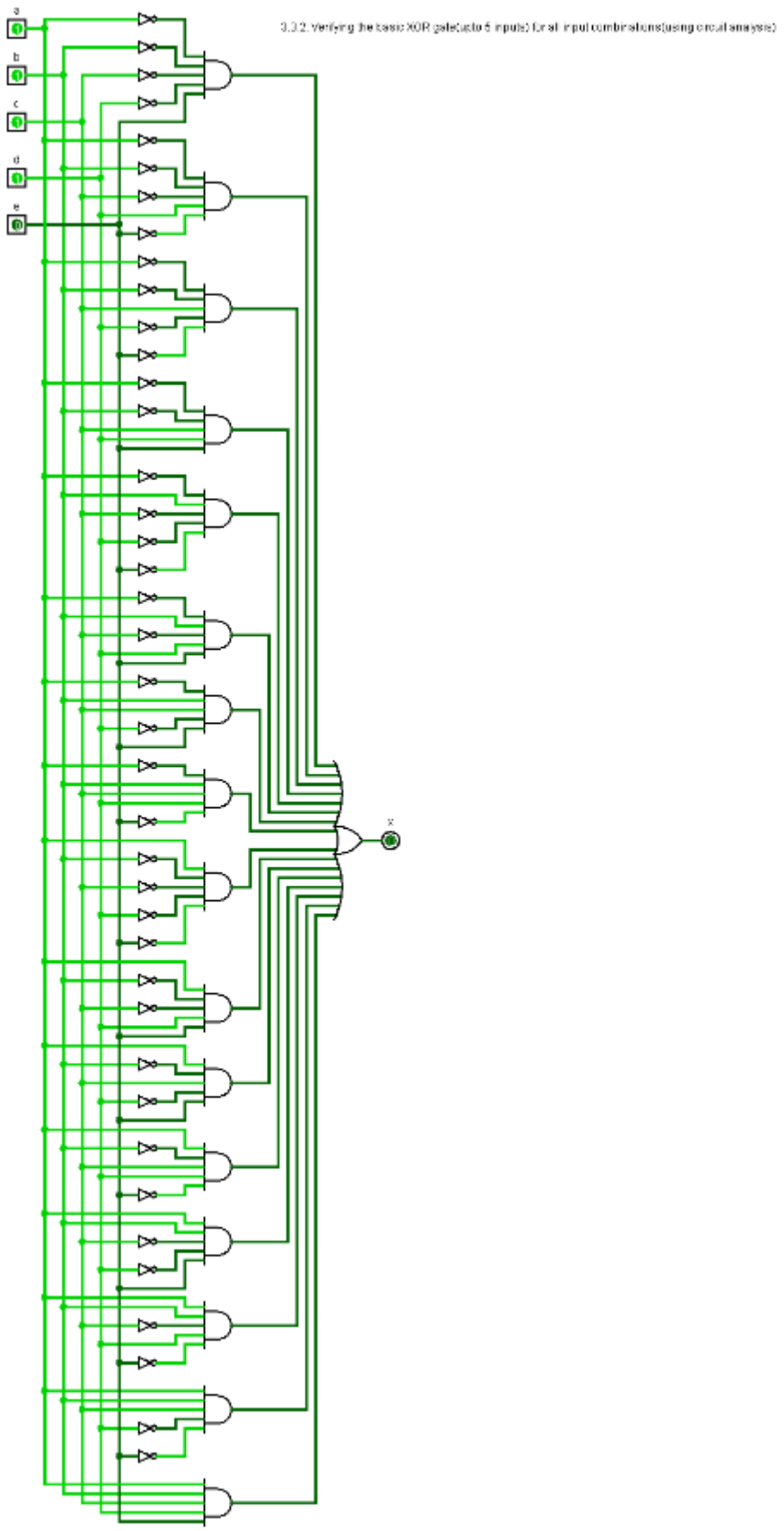

Figure: Circuit Diagram of XOR Gate(When the output is off)

ii. Truth Table:

a	b	c	d	e	x
0	0	0	0	0	0
0	0	0	0	1	1
0	0	0	1	0	1
0	0	0	1	1	0
0	0	1	0	0	1
0	0	1	0	1	0
0	0	1	1	0	0
0	0	1	1	1	1
0	1	0	0	0	1
0	1	0	0	1	0
0	1	0	1	0	0
0	1	0	1	1	1
0	1	1	0	0	0
0	1	1	0	1	1
0	1	1	1	0	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	0	0	1	0
1	0	0	1	0	0
1	0	0	1	1	1
1	0	1	0	0	0
1	0	1	0	1	1
1	0	1	1	0	1
1	0	1	1	1	0
1	1	0	0	0	0
1	1	0	0	1	1
1	1	0	1	0	1
1	1	0	1	1	0
1	1	1	0	0	1
1	1	1	0	1	0
1	1	1	1	0	0
1	1	1	1	1	1

5. Conclusion:

From the above experiment, we came to a conclusion that the output of a 5 input XOR gate 1/on, when the odd number of inputs are 1/on otherwise the output is 0/off.

3.4

1. Name of the Experiment:
Verify the Basic XNOR gate (up to 5 Inputs) for all input combinations.

2. Objectives:

- To know about XNOR gate
- To generate the truth table of XNOR gate
- To generate the logic circuit of XNOR gate

3. Theory:
The XOR gate is also called Exclusive XNOR. The output of XNOR gate is 1/on when the even number of inputs are 1/on otherwise the output is 0/off. The logical expression of two inputs XNOR gate is represented as F = AB + ~(AB).

4. Experimental Analysis:

i. Circuit:

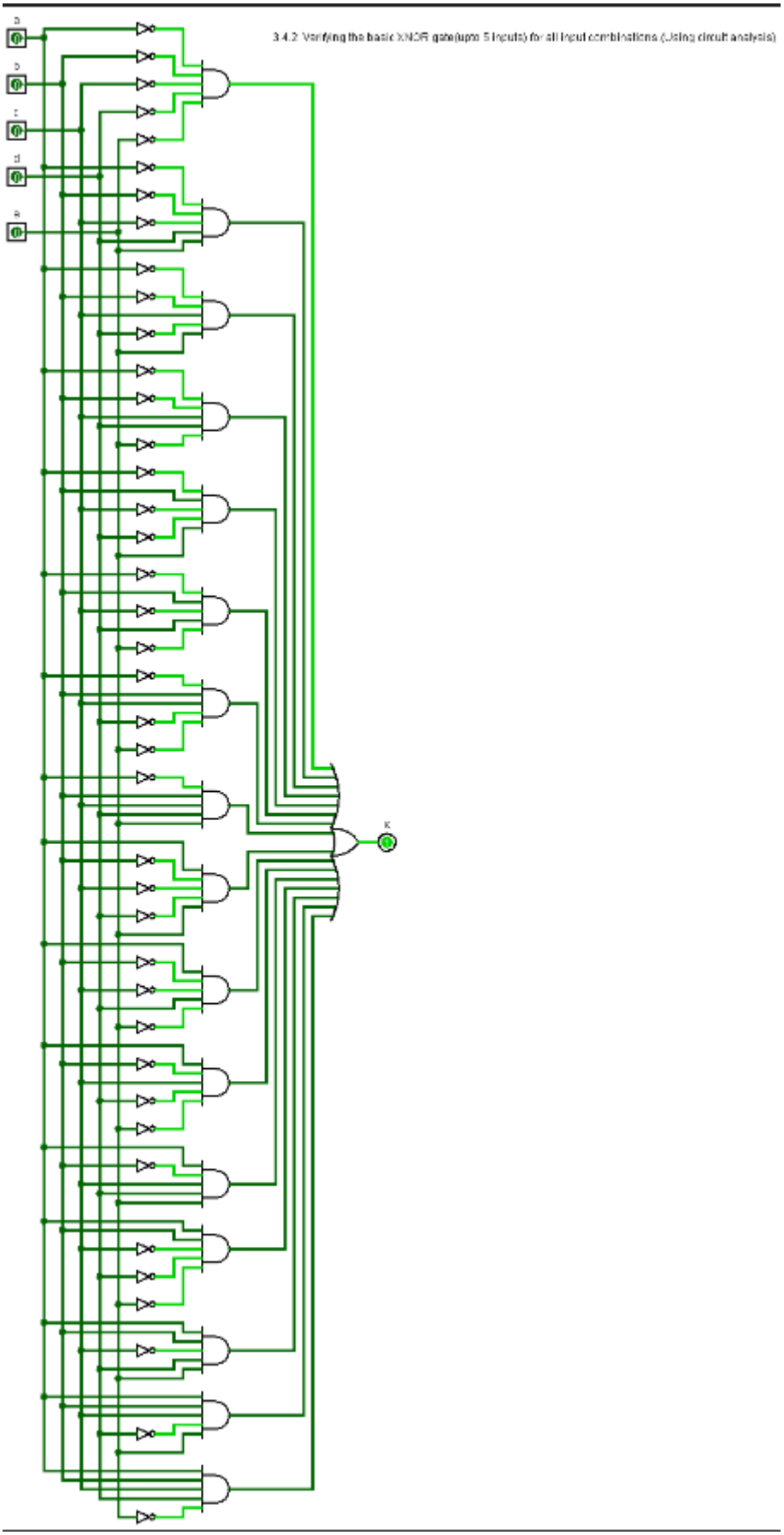

Figure: Circuit Diagram of XNOR Gate (When the output is on)

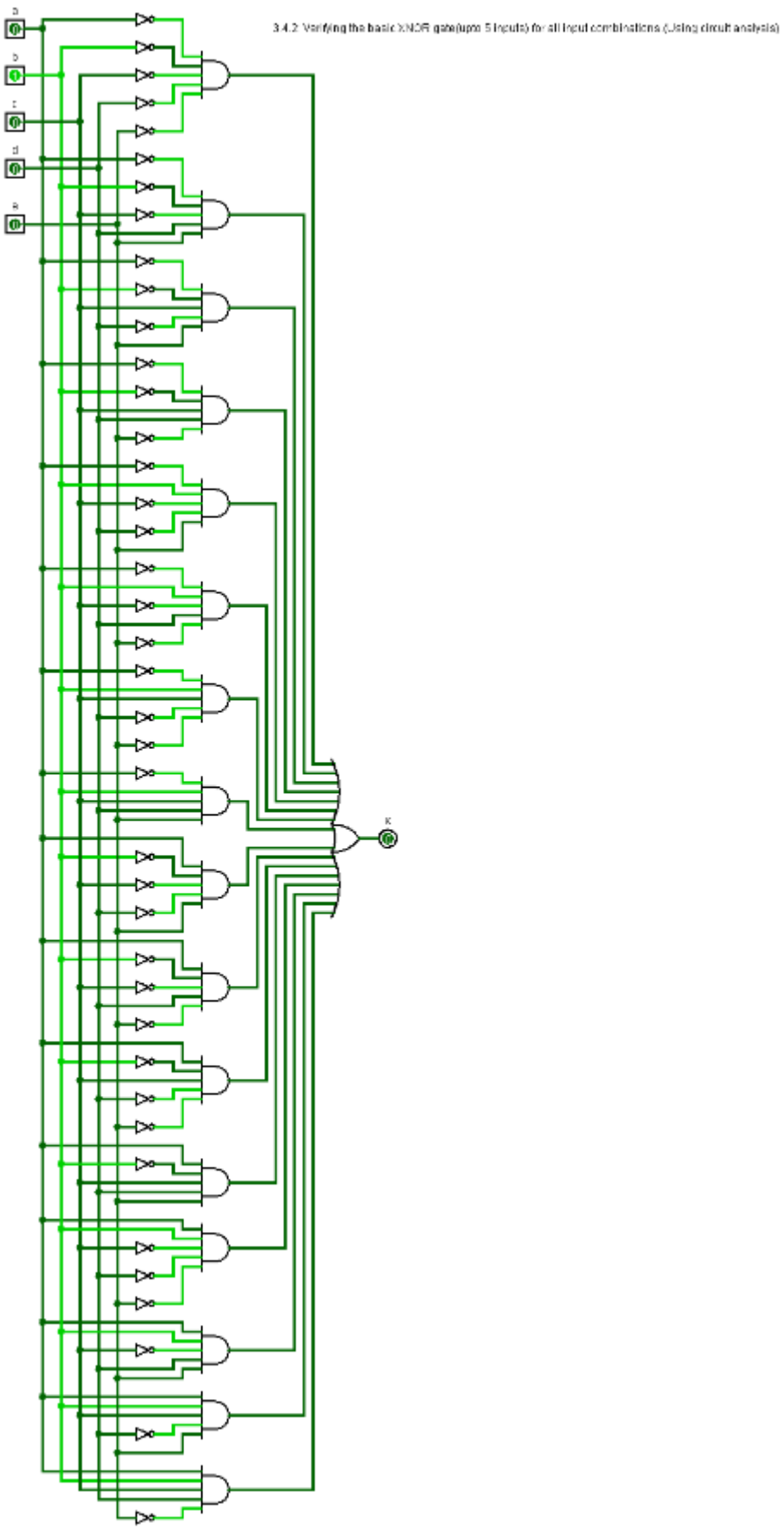

Figure: Circuit diagram of XNOR Gate(When the output is off)

ii. Truth Table:

a	b	c	d	e	x
0	0	0	0	0	1
0	0	0	0	1	0
0	0	0	1	0	0
0	0	0	1	1	1
0	0	1	0	0	0
0	0	1	0	1	1
0	0	1	1	0	1
0	0	1	1	1	0
0	1	0	0	0	0
0	1	0	0	1	1
0	1	0	1	0	1
0	1	0	1	1	0
0	1	1	0	0	1
0	1	1	0	1	0
0	1	1	1	0	0
0	1	1	1	1	1
1	0	0	0	0	0
1	0	0	0	1	1
1	0	0	1	0	1
1	0	0	1	1	0
1	0	1	0	0	1
1	0	1	0	1	0
1	0	1	1	0	0
1	0	1	1	1	1
1	1	0	0	0	1
1	1	0	0	1	0
1	1	0	1	0	0
1	1	0	1	1	1
1	1	1	0	0	0
1	1	1	0	1	1
1	1	1	1	0	1
1	1	1	1	1	0

5. Conclusion:

From the above experiment, we came to a conclusion that the output of a 5 input XNOR gate is 1/on, when the even number of inputs are 1/on otherwise the output is 0/off.