Rajshahi University of Engineering and Technology

Course Title: Sessional Based on CSE 2203

Course Code: CSE 2204

Lab Report - 04

Submitted to

Md. Zahirul Islam
Lecturer,
Computer Science and Engineering, RUET

Submitted by

Mrittika Roy
Roll: 1803175
Section: C
Computer Science and Engineering, RUET

Date: 03.07.2021

5.1

1. Name of the Experiment:
Verifying the Half Adder Circuit.

2. Objectives:

- To know about the Half Adder Circuit
- To know the different processes of implementing a Half Adder circuit
- To verify the Half Adder circuits implemented in different ways

3. Theory:
A half adder circuit is a combinational circuit that is able to add two single binary digits and provide the output and a carry value. It has two inputs and two outputs. The outputs are the sum and the carry. This half adder circuit can be implemented using the basic gates and also using the universal gates. The expressions are:
Let x and y are input variables and s(sum) and c(carry) are the output variables.
Using basic gates:
$s = x'y + xy'$
$c = xy$
Using the universal gates:
$s = x \oplus y$
$c = xy$

4. Experimental Analysis:

i. Circuit:

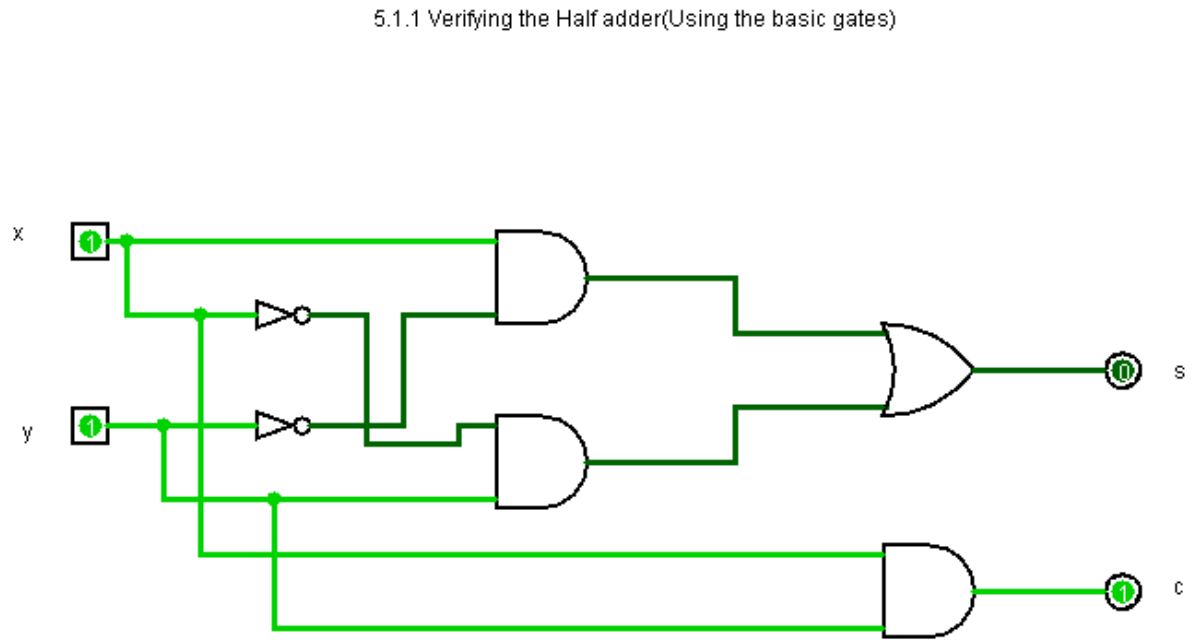

Figure: Verifying the Half Adder Circuit(using the basic gates)

5.1.2 Verifying HAlf adder (Using the universal gates)

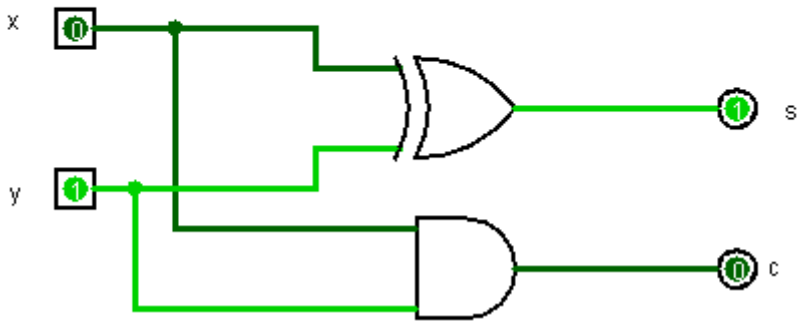

Figure:Verifying the Half Adder Circuit(using a XOR gate and an AND gate)

ii. Truth Table:

x	y	c	s
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

5. Conclusion:

From the above experiment, it is verified that in case of carry, the truth table shows the same result in both processes of implementation. In case of sum, the truth table shows the same result in both processes of implementation.

5.2

1. Name of the Experiment:
Verifying the Full Adder Circuit.

2. Objectives:
- To know about the Full Adder Circuit
- To know the different processes of implementing a Full Adder circuit
- To verify the Full Adder circuits implemented in different ways

3. Theory:
A full adder circuit is a combinational circuit that is able to add three single binary digits and provide the output and a carry value. It has three inputs and two outputs. The outputs are the sum and the carry. This full adder circuit can be implemented using the basic gates and also using the universal gates. The expressions are:
Let x, y and z are input variables and s(sum) and c(carry) are the output variables.
Using basic gates:
$s = x'y'z + x'yz' + xy'z' + xyz$
$c = xy + xz + yz$
Using the universal gates:
$s = (x \oplus y) \oplus z$
$c = xy + yz + zx$

4. Experimental Analysis:

i. Circuit:

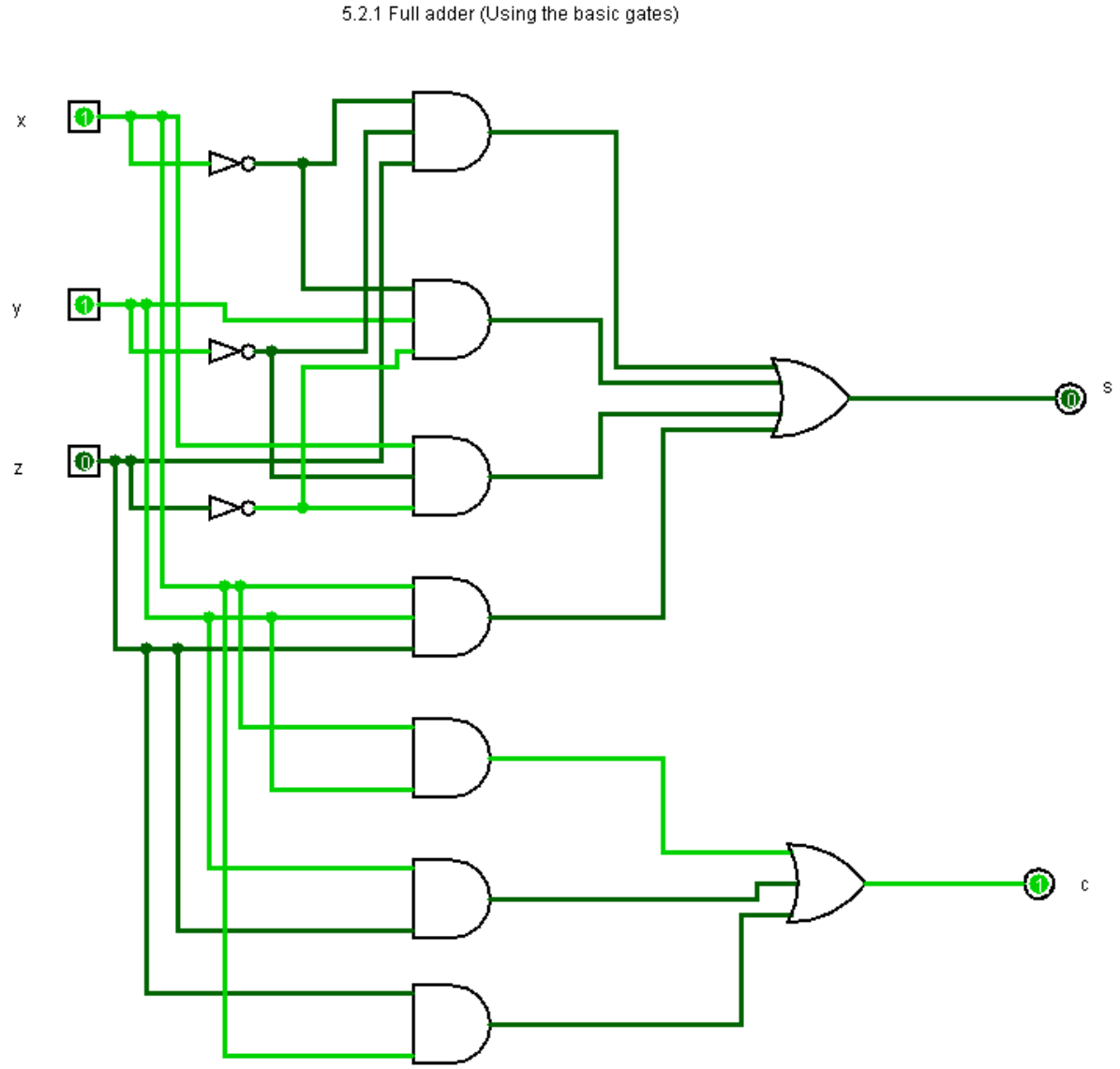

Figure: Verifying the Full Adder Circuit(using the basic gates)

5.2.2 Full adder (Using the universal gates)

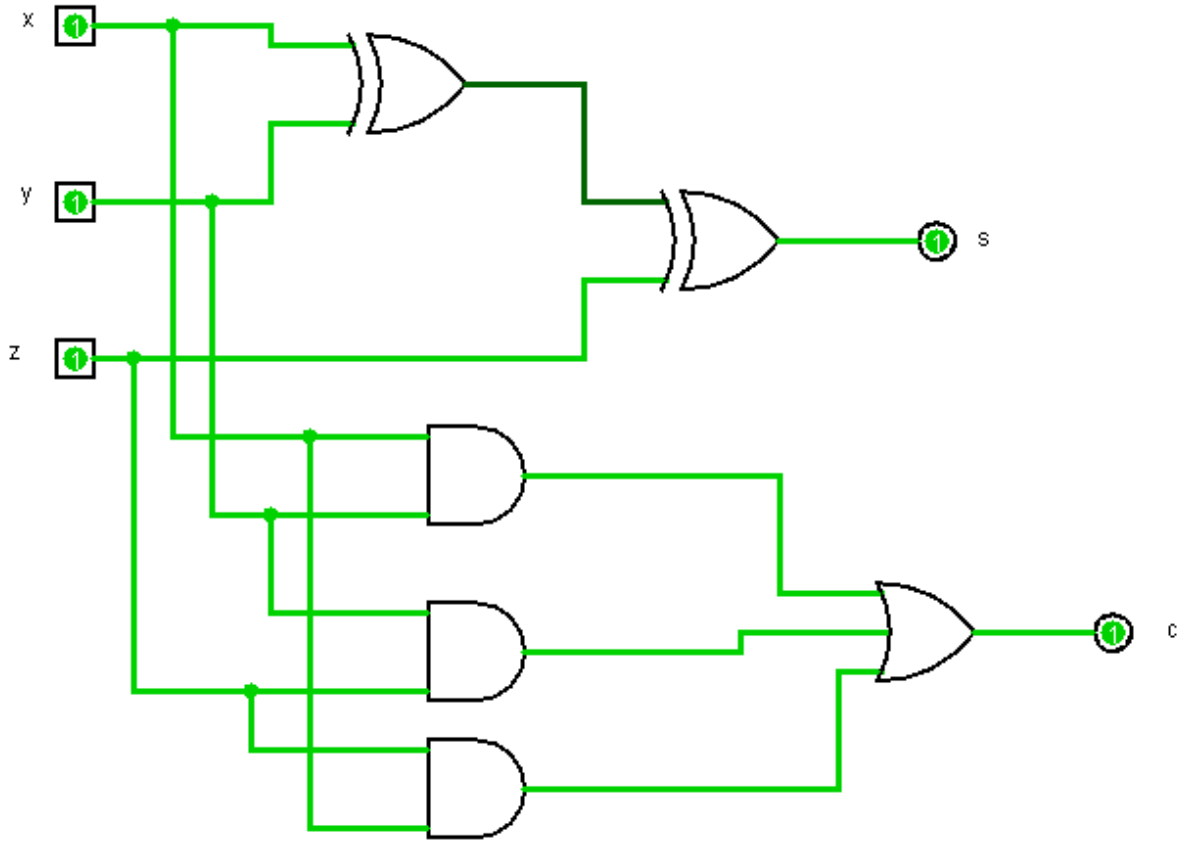

Figure:Verifying the Full Adder Circuit(using two XOR gates and three AND gates)

ii. Truth Table:

x	y	z	c	s
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

5. Conclusion:

From the above experiment, it is verified that in case of carry, the truth table shows the same result in both processes of implementation. In case of sum, the truth table shows the same result in both processes of implementation.

5.3

1. Name of the Experiment:
Implementing the Full Adder Circuit by using Half Adder Circuit and verifying the result.

2. Objectives:
- To know how to implement the Full Adder Circuit using the Half Adder Circuit
- To verify the result with the basic implementation of Full adder Circuit

3. Theory:
The Full Adder Circuit can be implemented using two half adder circuits and an additional two input OR gate.
Expressions:
Let x, y and z are input variables and s(sum) and c(carry) are the output variables.
$s = z'(xy' + x'y) + z(xy' + x'y)'$
$c = z(xy' + x'y) + xy$

4. Experimental Analysis:

i. Circuit:

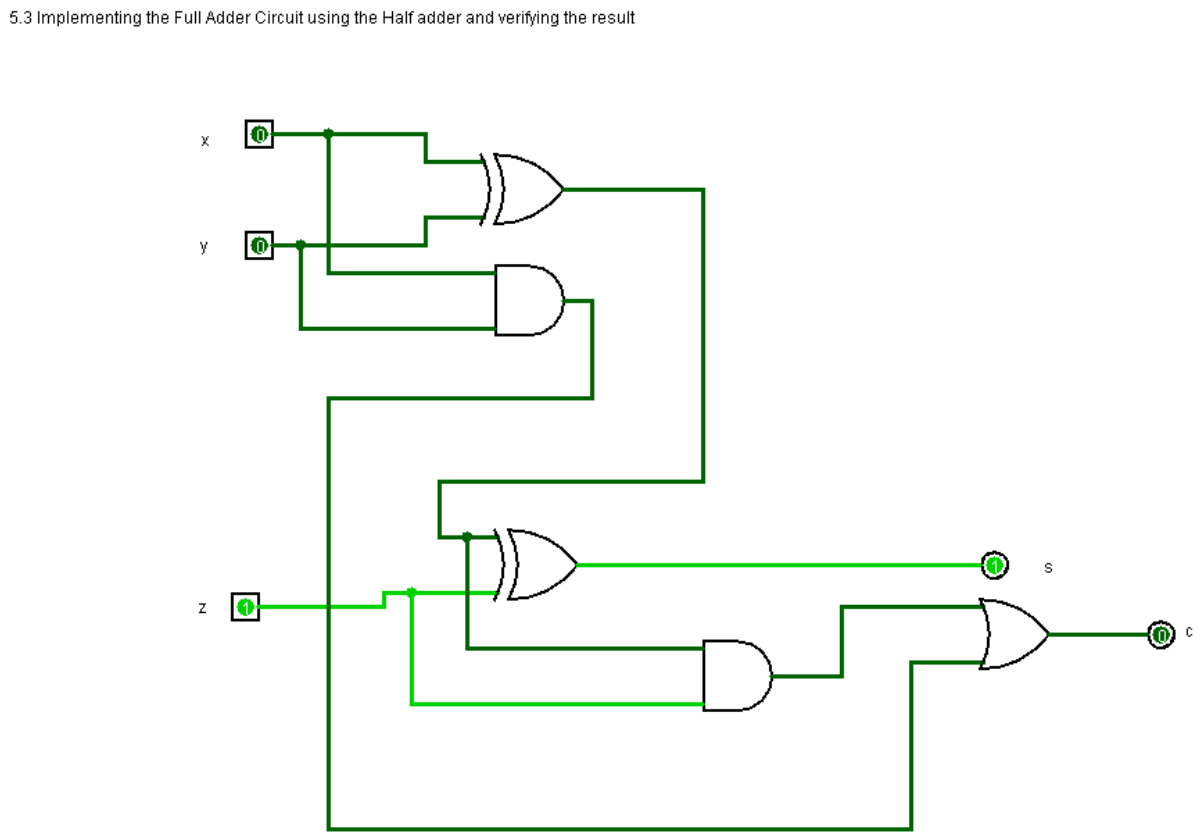

Figure: Implementing the Full Adder Circuit using Half Adder

ii. Truth Table:

x	y	z	c	s
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	0

5. Conclusion:

From the above experiment, it is shown that a full adder circuit can be implemented using two half adders circuit and an additional OR gate. It is also verified that the truth table of this implementation is the same as the truth table of the implementation of full adder in the formal process. So the result is verified.