Rajshahi University of Engineering and Technology
Course Title: Sessional Based on CSE 2203
Course Code: CSE 2204
Lab Report - 08

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9.1

1. Name of the Experiment:
Designing a 3-bit Asynchronous Counter by using JK Flip-Flops.

2. Objectives:

- To know how an asynchronous counter works
- To know how to design a 3 bit asynchronous counter using JK Flip-flop

3. Theory:
Asynchronous counters are those counters which do not operate on simultaneous clocking. In an asynchronous counter, only the first flip-flop is externally clocked using a clock pulse while the clock input for the successive flip-flops will be the output from a previous flip-flop. For designing a 3-bit asynchronous counter, three JK flip-flops are needed.

4. Experimental Analysis:
i. Circuit:

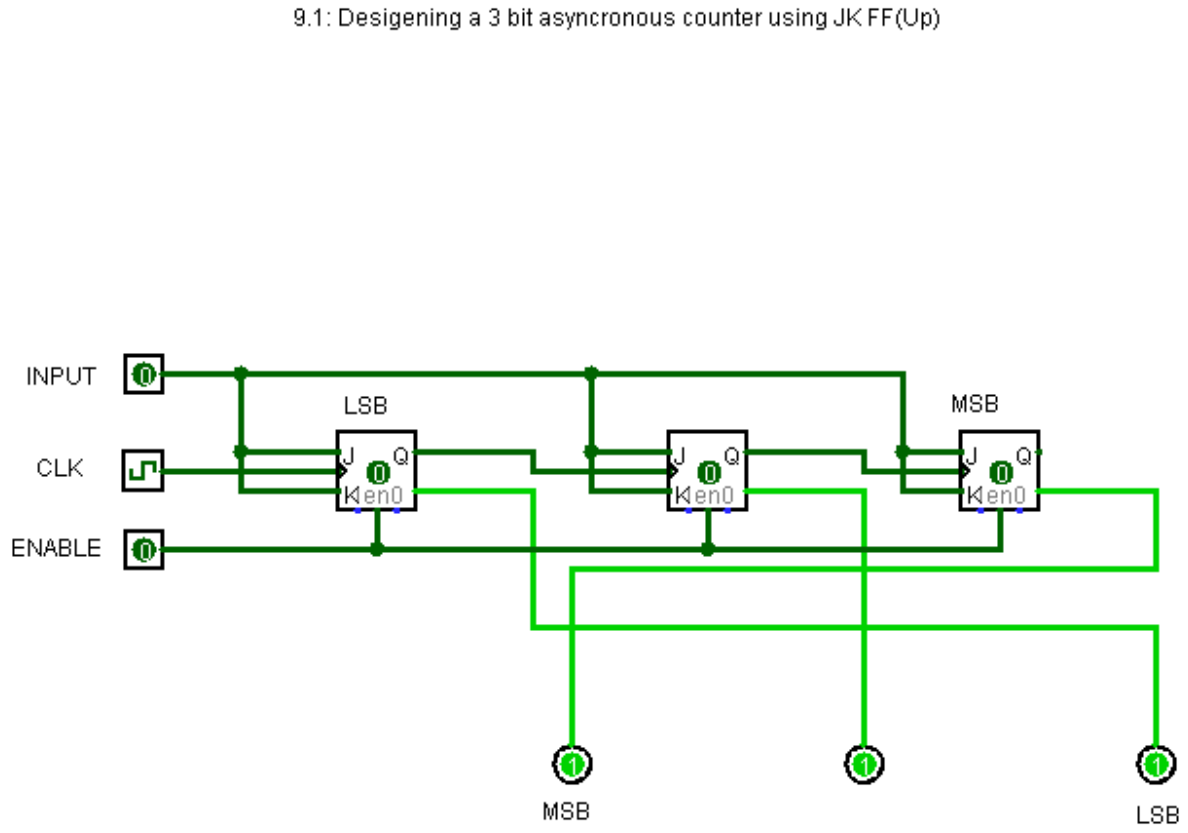

Figure: 3 bit asynchronous up counter

ii. Circuit Excitation Table:

Present state			Next state			Flip flop Input					
Q_c	Q_B	Q_A	Q_{C+1}	Q_{B+1}	Q_{A+1}	J_C	K_C	J_B	K_B	J_A	K_a
0	0	0	0	0	1	×	0	0	×	1	×
0	0	1	0	1	0	×	1	1	×	×	1
0	1	0	0	1	1	×	×	×	0	1	×
0	1	1	1	0	0	×	×	×	1	×	1
1	0	0	0	0	0	1	0	0	×	0	×
1	0	1	×	×	×	×	×	×	×	×	×
1	1	0	×	×	×	×	×	×	×	×	×
1	1	1	×	×	×	×	×	×	×	×	×

5. Conclusion:

In the above experiment, a 3 bit asynchronous up counter is designed using 3 JK flip flops. They are used as frequency dividers, as divide by "N" counters.They are used for low noise emission and low power application. They are used in designing asynchronous decade counter. It is also used in Ring counter and Johnson counter. Asynchronous counters are used in Mod N ripple counters. i.e. Mod 3, Mod 4, Mod 8, Mod 14, Mod 10 etc.

9.2

1. Name of the Experiment:

Designing a 3-bit Synchronous Counter by using various Flip-Flops.

2. Objectives:

- To know how an synchronous counter works
- To know how to design a 3 bit synchronous counter using various Flip-flops

3. Theory:

In a synchronous counter, the clock input across all the flip-flops use the same source and create the same clock signal at the same time. So, a counter which is using the same clock signal from the same source at the same time is called Synchronous counter.

4. Experimental Analysis:

i. Circuit:

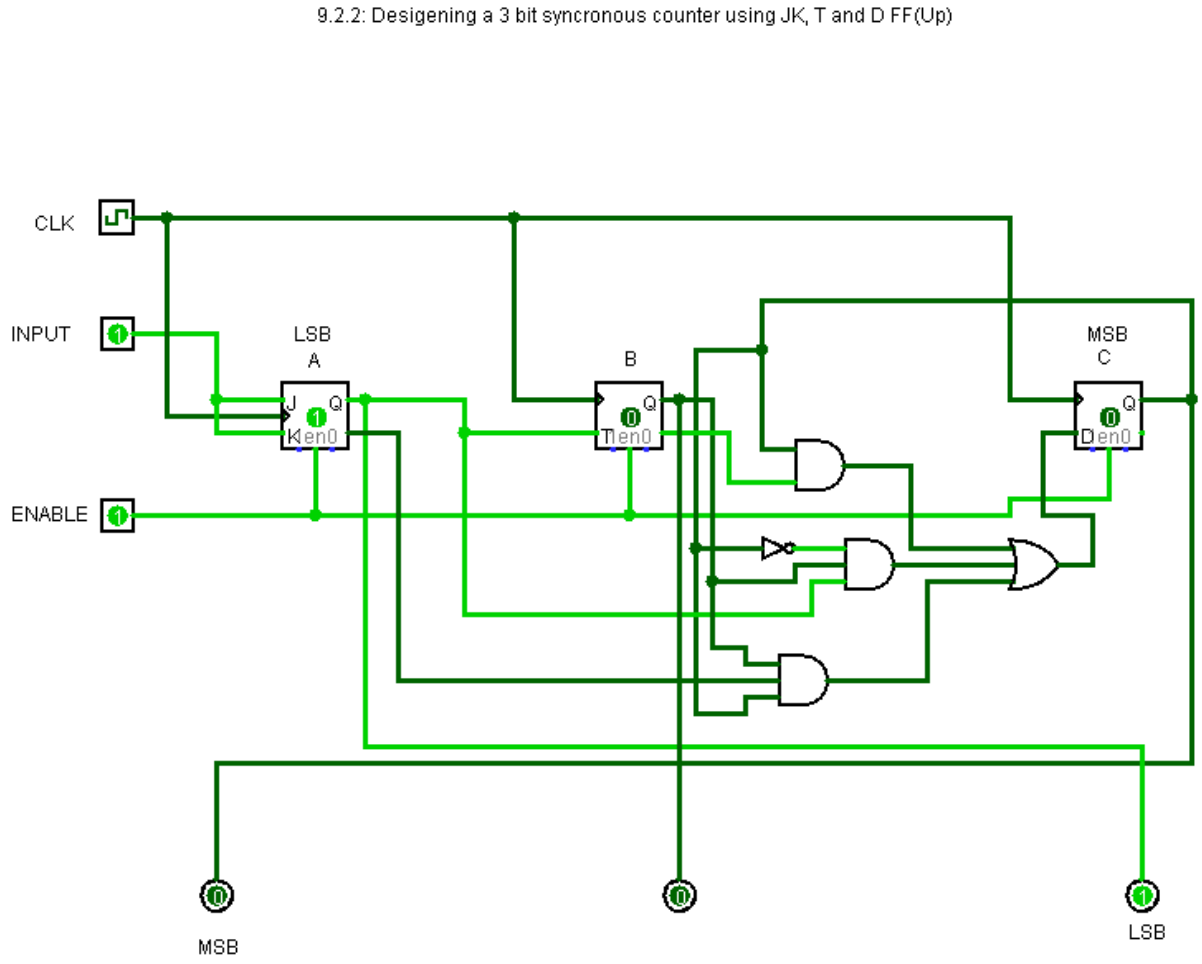

Figure: 3 bit synchronous up counter

ii. Circuit Excitation Table:

Present State			**Next State**			**Flip-Flop Input**			
Q_C	Q_B	Q_A	Q_{C+1}	Q_{B+1}	$Q_{A+!}$	D_C	T_B	J_A	K_A
0	0	0	0	0	1	0	0	1	X
0	0	1	0	1	0	0	1	X	1
0	1	0	0	1	1	0	0	1	X
0	1	1	1	0	0	1	1	X	1
1	0	0	1	0	1	1	0	1	X
1	0	1	1	1	0	1	1	X	1
1	1	0	1	1	1	1	0	1	X
1	1	1	0	0	0	0	1	X	1

5. Conclusion:

In the above experiment, a 3-bit synchronous up counter is implemented.Here at LSB position, JK FF is used, at middle T FF is used and at MSB position D FF is used. This counter counts from 0 to 7 . It is a UP counter.