Rajshahi University of Engineering and Technology

Course Title: Sessional Based on CSE 2203

Course Code: CSE 2204

Lab Report - 07

Submitted to

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8.1

1. Name of the Experiment:
Verify SR Flip-Flop by using Module.

2. Objectives:
- To know the SR flip flop and its output
- To verify the outputs using module

3. Theory:
In a SR flip-flop module in Logisim, when the clock triggers, the value remembered by the flip-flop remains unchanged if R and S are both 0, becomes 0 if the R input (*Reset*) is 1, and becomes 1 if the S input (*Set*) is 1. If both inputs are 1, the value in the flip flop remains unchanged in logisim. But usually this case produces invalis condition in the flip-flop.

4. Experimental Analysis:
i. Circuit:

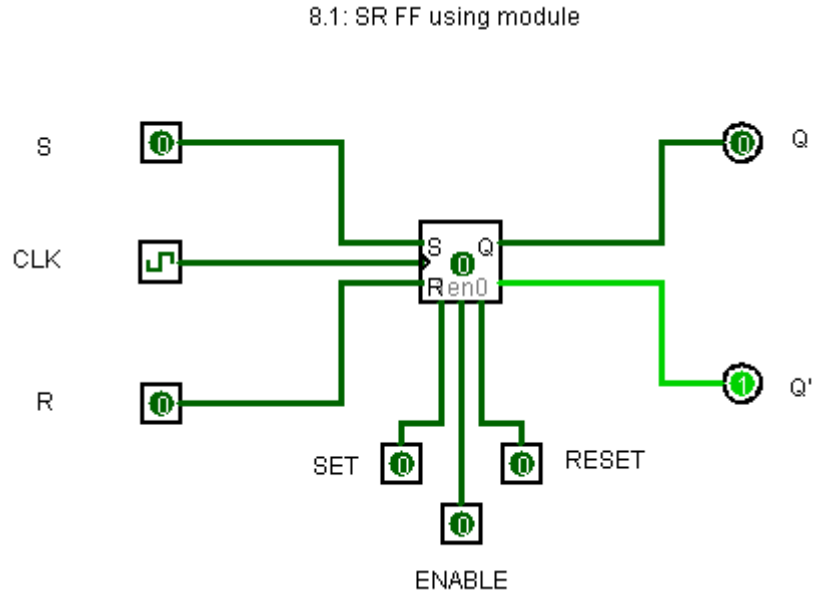

Figure: SR flip-flop using module

ii. Truth Table: For SR module

S	R	Q
0	0	Unchanged
0	1	0
1	0	1
1	1	Invallid(unchanged in Logisim)

5. Conclusion:
From the above experiment, it is verified that the output is the same as the implemented flip-flop using logic gates.

8.2

1. Name of the Experiment:
Verify JK Flip-Flop by using Module.

2. Objectives:
- To know the JK flip flop and its output
- To verify the outputs using module

3. Theory:
In a SR flip-flop module in Logisim, when the clock triggers, the value remembered by the flip-flop toggles if the J and K inputs are both 1, remains the same if they are both 0; if they are different, then the value becomes 1 if the J (*Jump*) input is 1 and 0 if the K (*Kill*) input is 1.

4. Experimental Analysis:
i. Circuit:

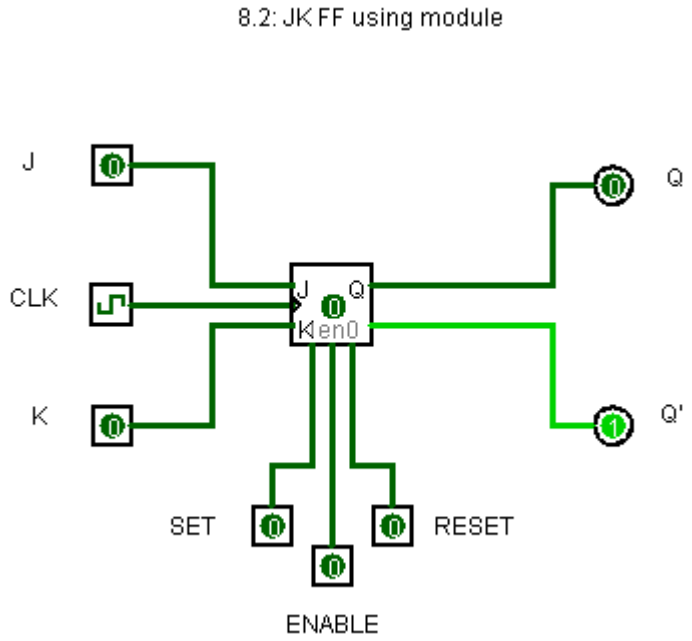

Figure: JK flip-flop using module

ii. Truth Table: For JK module

J	K	Q
0	0	Unchanged
0	1	0
1	0	1
1	1	Q'(Toggle)

5. Conclusion:
From the above experiment, it is verified that the output is the same as the implemented flip-flop using logic gates.

8.3

1. Name of the Experiment:
Verify D Flip-Flop by using Module.

2. Objectives:
- To know the D flip flop and its output
- To verify the outputs using module

3. Theory:
In a D flip-flop module in Logisim, when the clock triggers, the value remembered by the flip-flop becomes the value of the D input (*Data*) at that instant.

4. Experimental Analysis:

i. Circuit:

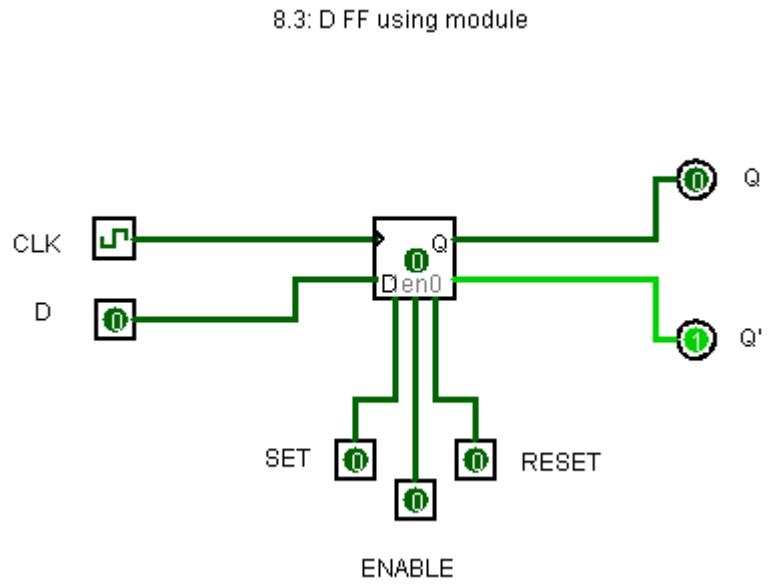

Figure: D flip-flop using module

ii. Truth Table: For D module

D	Q
0	0
1	1

5. Conclusion:

From the above experiment, it is verified that the output is the same as the implemented flip-flop using logic gates.

8.4

1. Name of the Experiment:

Verify D Flip-Flop by using Module.

2. Objectives:

- To know the D flip flop and its output
- To verify the outputs using module

3. Theory:

In a T flip-flop module in Logisim, when the clock triggers, the value remembered by the flip-flop either toggles or remains the same depending on whether the T input (*Toggle*) is 1 or 0.

4. Experimental Analysis:

i. Circuit:

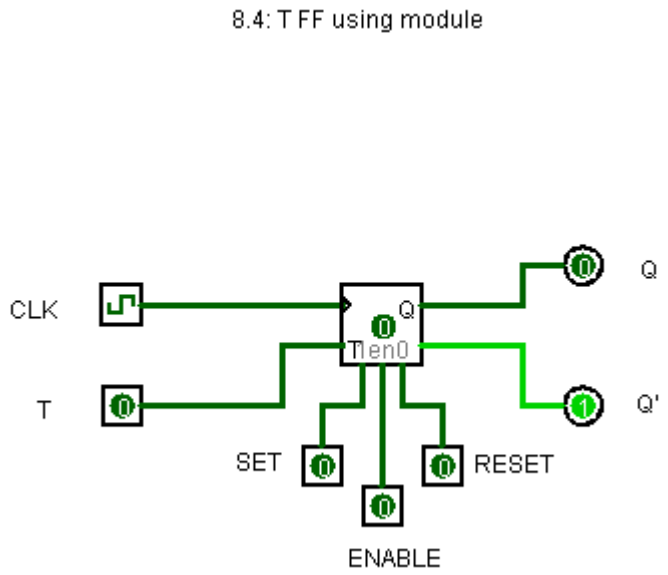

Figure: T flip-flop using module

ii. Truth Table: For T module

T	Q
0	Q
1	Q’

5. Conclusion:

From the above experiment, it is verified that the output is the same as the implemented flip-flop using logic gates.