Rajshahi University of Engineering and Technology

Course Title: Sessional Based on CSE 2203

Course Code: CSE 2204

Lab Report - 06

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Date of Submission: 07.08.2021

7.1

1. Name of the Experiment:
Verifying SR Flip-Flop by using NOR & NAND Latch.

2. Objectives:
- To know the nature of SR flip-flop
- To know how to implement SR flip-flop using NOR and NAND latch
- To verify the output of SR flip-flop

3. Theory:
SR flip-flop stands for SET-RESET flip-flops. Its two inputs are S and R. It also has a clock pulse. The outputs are denoted by Q and Q'. It can be implemented using NOR latch or NAND latch. There is a limitation in SR flip-flop. It has an invalid condition. At S=1, R=1, the output is ambiguous.

4. Experimental Analysis:
i. Circuit:
For NOR Gate:

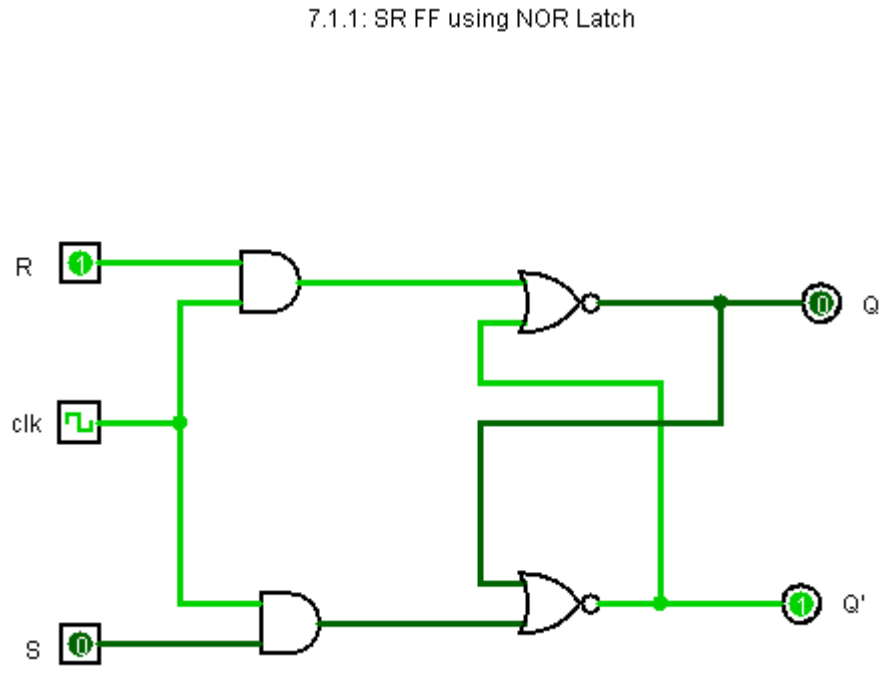

Figure: SR flip-flop using NOR gate

For NAND Gate:

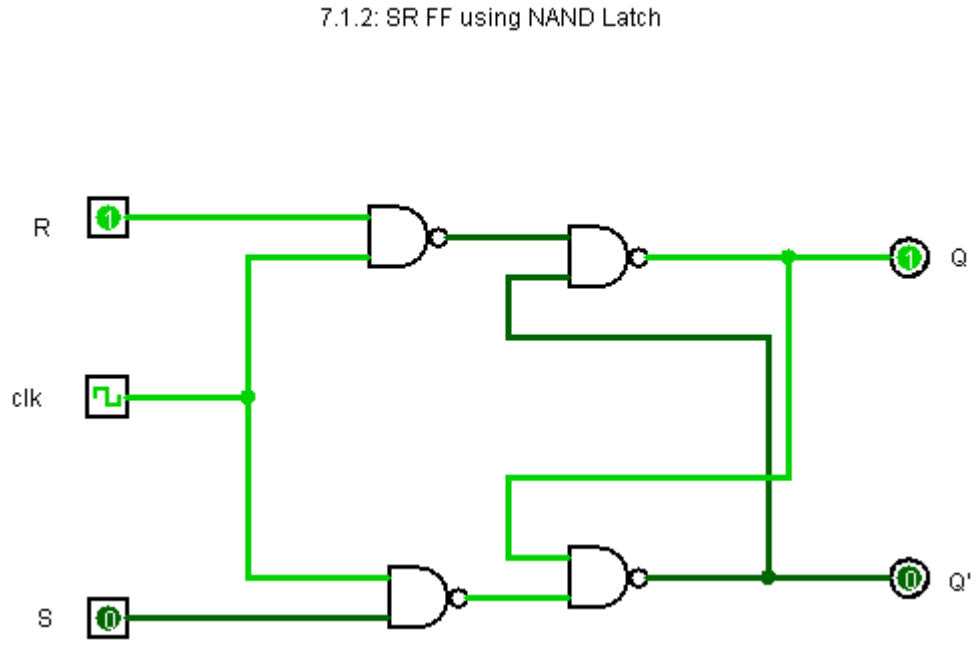

Figure: SR flip-flop using NAND gate

ii. Truth Table:

S	R	Q
0	0	Unchanged
0	1	0
1	0	1
1	1	Invallid

5. Conclusion:

In the above experiment, the SR flip-flop is verified. It is used to keep a record of different values of variable state like intermediate, input or output.It is mainly used to store data or information.Wherever operations, storage and sequencing are required these signal circuits are used.They are also used for excising control over the way the circuit has to function, like for changing the operation of a circuit to a different state.

7.2

1. Name of the Experiment:
Verifying JK Flip-Flop by using NOR & NAND Latch.

2. Objectives:
- To know the nature of JK flip-flop
- To know how to implement JK flip-flop using NOR and NAND latch
- To verify the output of JK flip-flop

3. Theory:
The JK flip flop is a universal flip flop having two inputs 'J' and 'K'. It also has a clock pulse. The outputs are denoted by Q and Q'. It can be implemented using NOR latch or NAND latch. The JK flip flop works in the same way as the SR flip flop works. But the only difference is the output is toggled in the invalid condition of SR flip-flop.

4. Experimental Analysis:
i. Circuit:
For NOR Gate:

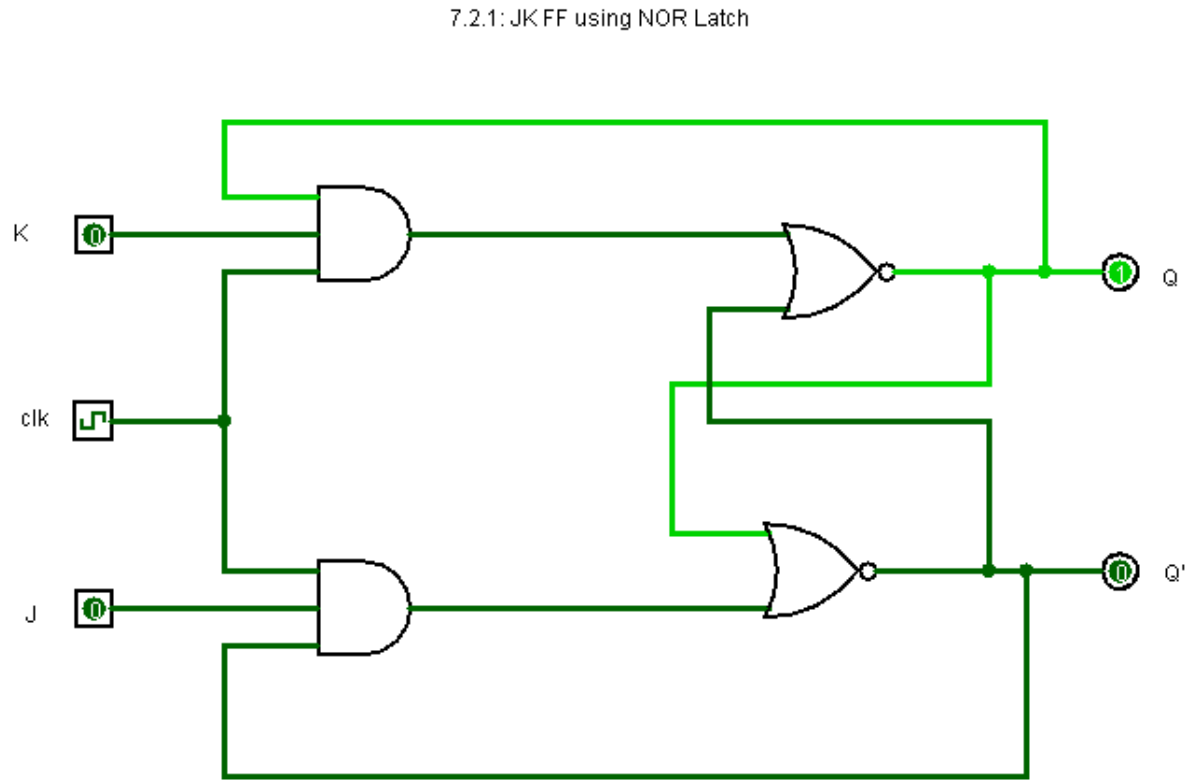

Figure: JK flip-flop using NOR gate

For NAND gate:

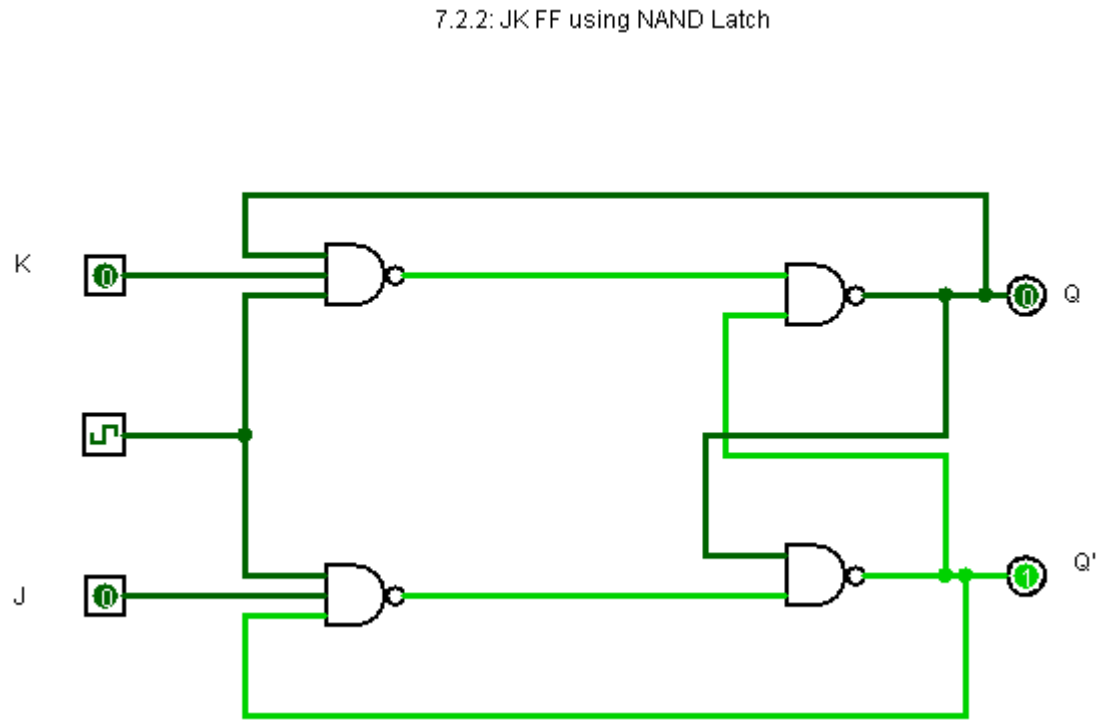

Figure: JK flip-flop using NAND gate

ii. Truth Table:

J	K	Q
0	0	Unchanged
0	1	0
1	0	1
1	1	Toggled

5. Conclusion:

In the above experiment, the JK flip-flop is verified. It is widely used as a sequence detector.The major use of this circuit occurs in the binary counter.It is also used as a frequency divider.The circuit is also applied for calculating the shift register.And, with the help of this sequential circuit we can also calculate serial data transfer values.It is also used for calculating the parallel data transfer values.

7.3

1. Name of the Experiment:
Verifying D Flip-Flop by using NOR & NAND Latch.

2. Objectives:

- To know the nature of D flip-flop
- To know how to implement D flip-flop using NOR and NAND latch
- To verify the output of D flip-flop

3. Theory:
It has one data input. Its output changes to the value of the input at either the positive- or negative-going clock trigger. It may be implemented with a J-K FF by tying the J input to the K input through an inverter. By setting J = D, K = D' in JK flip-flop D flip-flop can be implemented.It is useful for parallel data transfer.

4. Experimental Analysis:
i. Circuit:
For NOR Gate:

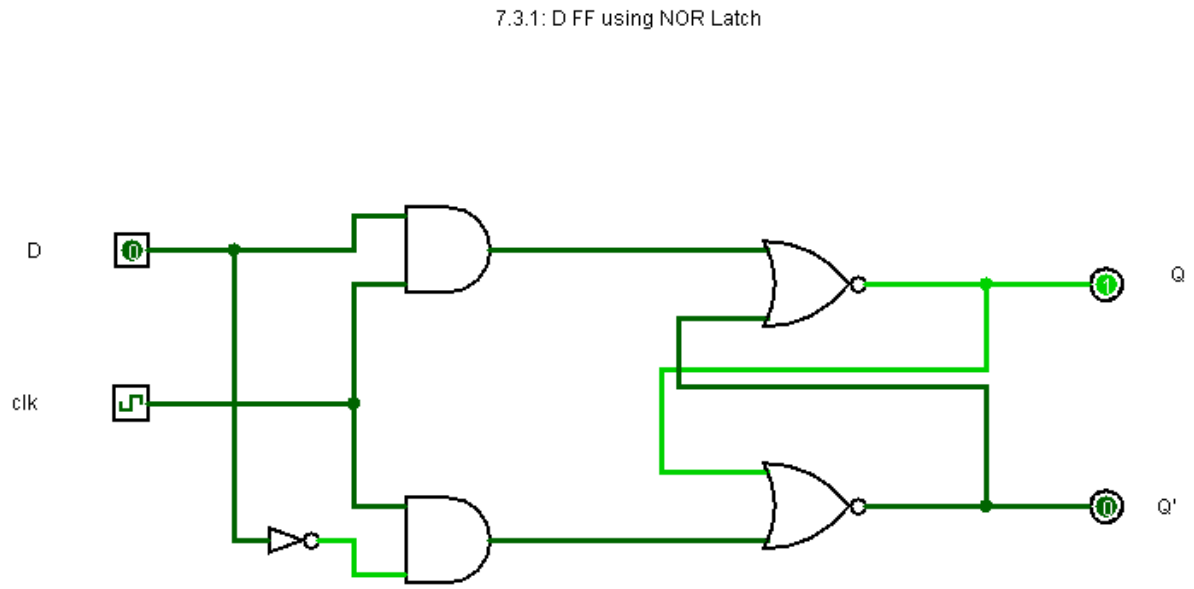

Figure: D flip-flop using NOR gate

For NAND Gate:

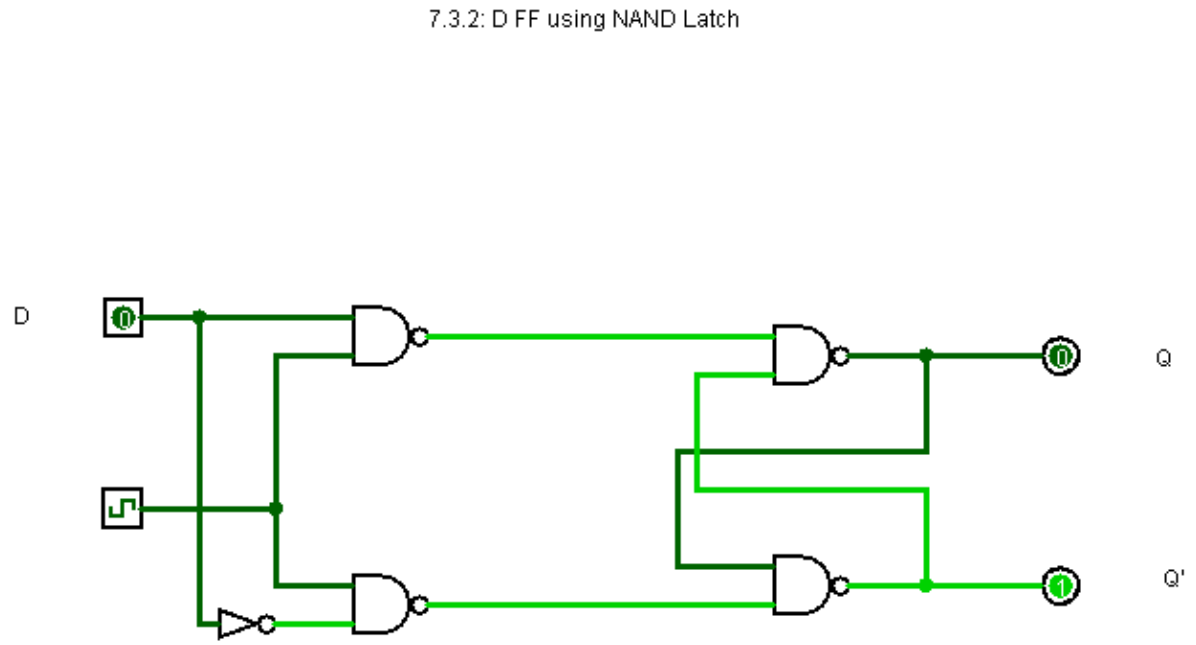

Figure: D flip-flop using NAND gate

ii. Truth Table:

D	Q
0	0
1	1

5. Conclusion:

In the above experiment, the D flip-flop is verified. The main use of a D flip flop is as a Frequency Divider. D flip-flop can be used to create delay-lines which are used in digital signal processing systems. D flip-flop can be used as event detectors.

7.4

1. Name of the Experiment:
Verifying T Flip-Flop by using NOR & NAND Latch.

2. Objectives:

- To know the nature of T flip-flop
- To know how to implement T flip-flop using NOR and NAND latch
- To verify the output of T flip-flop

3. Theory:
T flip-flop A clocked flip-flop whose output "toggles", i.e. changes to the complementary logic state, on every active transition of the clock signal (see clock). It can be considered as being equivalent to a JK flip-flop whose J and K inputs are held at logic 1.

4. Experimental Analysis:
i. Circuit:
For NOR Gate:

7.4.1: T FF using NOR Latch

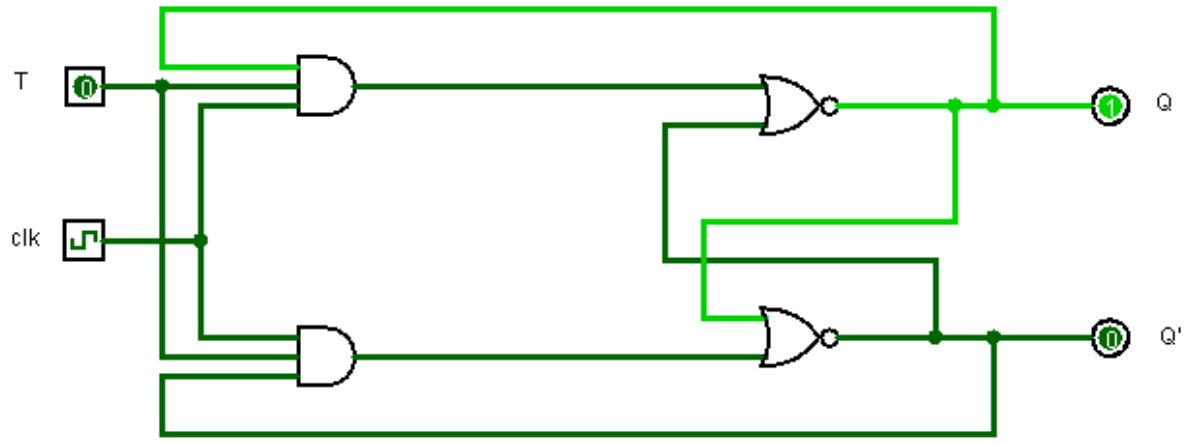

Figure: T flip-flop using NOR gate

For NAND Gate:

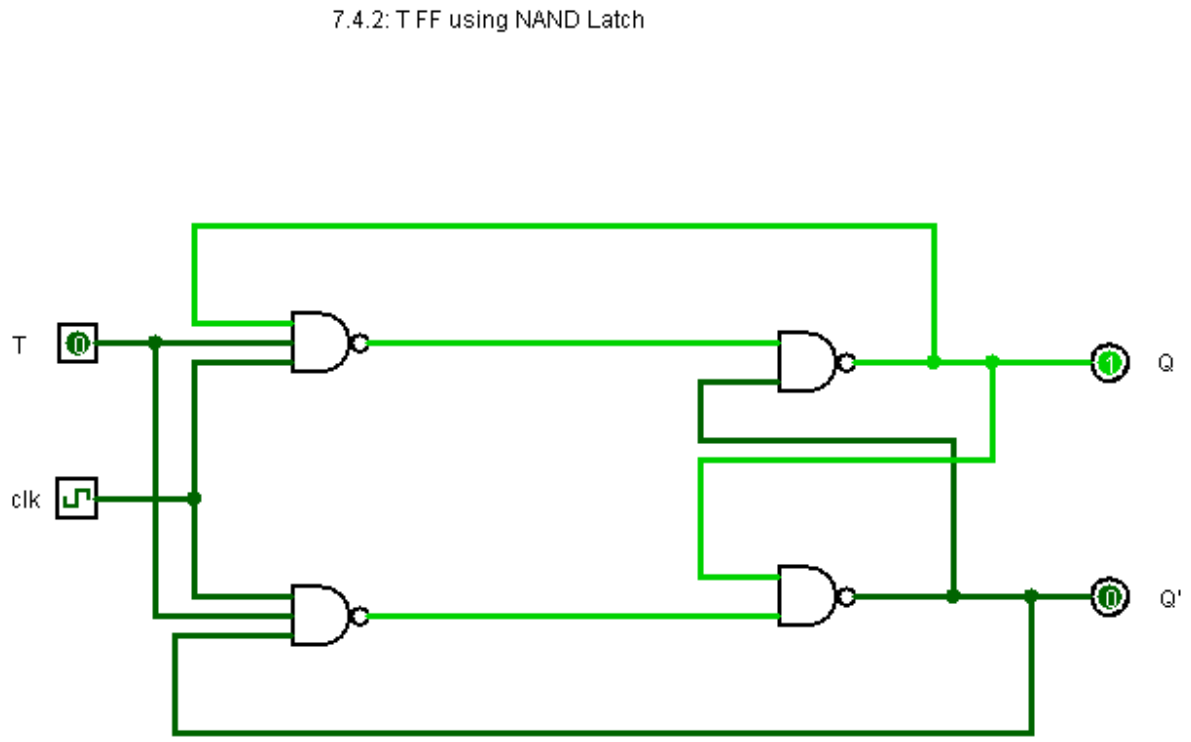

Figure: T flip-flop using NAND gate

ii. Truth Table:

T	Q
0	Unchanged
1	Toggled

5. Conclusion:

In the above experiment, the D flip-flop is verified. It is used in counter designs.These flip flops are used for constructing binary counters. They are used in frequency dividers.This type of sequential circuits is also present in binary addition devices. It is also used in 2-bit parallel load registers. It is also used in shift registers.