Mrityunjay Kumar

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OBJECTIVE

Growing by delivering best of my services to the organization's growth and keep improving by learning and experience.

PROFESSIONAL SUMMARY

An experienced software engineer with specialization in designing and development of highly secure operating system based on java card and global platform technology.

Java Card Virtual Machine:
- Design and development of **interpreter**
- Development of **Stack frame**
- Garbage collection redesigning
- Native to java and java to native calling

Memory Management:
- Heap management (Paged and Linear)
- Memory **Defragmentation**
- Software **wear levelling**
- High Stress Memory (**HSM**) for secure element
- Development of **cache mechanism**
- Designing atomic and tearing protection mechanism for smart card operating system
- Merging of java and native stack frame to save RAM memory

Others:
- Hands on experience of working on CCC (**Car Connectivity Consortium**) standards
- Java card applet development
- Representing IDEMIA in Car Connectivity Consortium (CCC).
- Good understanding of cryptography(symmetric & Asymmetric), PKI and certificate management
- Anti-roll back solution for integrated secure element
- Designed Factory reset solution for integrated secure element
- Designed startup routine to integrate Java card OS with BSP (Board support package)
- Performance improvement by **reducing NVM writings**
- Designed and developed proof of concept for **simulator** of integrated secure element platform
- Designed memory manager for a smart card OS and managed to achieve atomicity without any overhead of transaction buffer
- Bootloader area utilization
- Smart card production

PATENT

- Applied for patent of "**A SYSTEM AND METHOD FOR RECORDING TRANSACTION ASSOCIATED WITH A PAGE-ORIENTED NON-VOLATILE MEMORY**".
- Applied for patent of " **A SYSTEM AND METHOD TO UPDATE ATOMIC AND NON ATOMIC MEMORY**"

PROFESSIONAL AWARDS

- Member of IDEMIA Global Technical Expert Network.
- Awarded as "**Morpheus 2017**" award at **Syscom Corporation Limited (A Safran group Company)** India for the idea which brings value to the organization in terms of significant saving (Cost, Time).
- Awarded as "**High Flyer 2014**" award at **Safran Engineering Services** for the best performance in year 2014.

COMPUTER SKILLS

Operating Systems: Windows, Linux
Languages: Core Java, Java Card, C, C++
Protocols: SCP02, UART, T=0,SPI
CM&RM Tools: CM Synergy, DOORs 9.3, Perforce, GIT
Change Mgmt. Tool: Redmine (Open Source), JIRA
Other Tool: CBS (CPIOM based Simulator), SCADE
Avionic Guideline: DO178B
Smart card standards: ISO 7816 -3, ISO 7816 -4, GP2.3, GP221, GP211
Java Card: 3.0.4, 3.0.5
Others: Six Sigma project experience

PROFESSIONAL EXPERIENCE

04/2019–Present   Associate System Architect at IDEMIA, India
- Defining PKI infrastructure for digital key applets
- Involved in designing of high performance Java card operating system with small footprint
- Monitoring KPIs on regular basis
- Code review
- Support and guide development team in converting design into Code
- Defining Test Strategy
- Manage bugs reported by Customer
- Defining steps for smart card production

10/2017–03/2019   Technical Lead at IDEMIA, India
- Acting as a system architect for a project team
- Requirement refinement with customer
- Support and guide development team in converting Design into Code
- Defining Test Strategy

10/2016–10/2017   Senior Software Engineer at **Syscom Corporation Limited (A Safran group Company) India**
- Played a major role in the exploration of ideas to improve an efficiency of platform for java card Operating System.
- Developing major parts of Smart card operating system core components like Microkernel, Java Card, and Card Management.

02/2015–10/2016   Software Engineer at **Syscom Corporation Limited (A Safran group Company) India**
- Feature development for smart cards as per java card and global platform standards
- Bug Fixing
- Debugging defects
- Performance tuning
- Helping team members to reach sprint goal

08/2011-02/2015   Software Engineer at **SAFRAN Engineering Services India, Bangalore (A Safran group Company)**
- High Level Requirement Analysis
- Bug Fixing
- Debugging defects
- Review of the products deliverable to customer.
- DOORs 9.3 (Requirement Management tool) **handling and Training.**
- Training team members.
- Mentoring team of 10+ members in **Agile/Scrum methodology.**

PROJECTS & RESPONSIBILITIES

Dec 20 to Present **Soft SimOS**— Project is to develop secure element OS for IOT device based on Qualcomm board (QC9206) to provide cellular connectivity.
Role:
- Design and develop **FOTA** to upgrade secure element OS
- Designing and development secure element OS initialization process
- Designing and development of memory management for the utilization of Trust Zone(TZ)
- Designing and development of memory management based on POSIX apis provided by master OS
- Integrating secure element with BSP (Board support package) of master OS.
- Development of OS personalization process

Technologies Used: C, C++11, Java card, Data structure, Algorithm
Team Size: 7
Tools used: VS 2015, JIRA, GIT

Aug 20 to Dec20 **Connected Car** — Project is to use smart devices like mobile phones to access vehicle. Driven by use cases, this project focuses on accessing the vehicle lock/unlock, engine start/stop etc… based on **CCC** (**Car connectivity consortium**) standard.
Role:
- Java card applet development as per CCC use cases
- Certification management for secure element and CCC applet
- Designing low level design of CCC controller based on SPI interface
- Defining proprietary commands for personalizing embedded secure element
- Designing LLDs for standard commands

Technologies Used: C, Java card, Data structure, Algorithm
Team Size: 15
Tools used: VS 2010, JCIDE,JCOP, JIRA, GIT

Aug 19 to Jul20 **Java card operating system for Integrated Secure Element** -- Project is to provide secure payment solution for an integrated secure element based on ARM CortexM architecture, which has limited volatile memory (RAM) but does not have persistent memory (NVM).
Role:
- Providing Solution for key features like
  - Memory Management (Overlays, Extended RAM Heap ...)
  - Factory Reset
  - Anti-Roll Back
  - Startup routine with BSP
  - CGM(Cumulative granted memory) as per global platform
- Designing simulator for integrated secure element
- Monitoring KPIs (Key performance Index)
- Support Development team in converting Design into Code
- Defining Test strategy
- Code Review
- Requirement discussion with customer

Technologies Used: C, Data structure, Algorithm
Team Size: 20
Tools used: MORPHO Eclipse, VS 2008, Perforce, JIRA

Oct 18 to Jul 19 **Native JCOS**— A pure native platform which provides complete java card services with smallest possible foot print and high performance.
Role:
- Designing memory manager
- Development of Stack frame for interpreter
- Designing native to java and java to native calling
- Performance tuning for garbage collection
- Defining test scenarios

Technologies Used: C, Data structure, Algorithm
Team Size: 20
Tools used: VS 2010, JIRA, GIT

Jun 18 to Sep 18   **Redesigning of memory architecture for Java card operating system--** This project is to redesign and implement a memory architecture to reduce buffer overheads from memory. The main goal is to remove the buffers like transaction buffer, tearing buffer.
    Role:
- Designing page memory management algorithm to **reutilize Transaction buffer** for multiple purpose
- Development of proof of concept

    Technologies Used: C, Data structure, Algorithm
    Team Size: 3
    Tools used: VS 2010, GIT, JIRA

Jan 18 to May 18   **Remodeling of low-level design for Java card operating System --** This project is to redesign and implement the low-level architecture of operating system to improve performance with less NVM and RAM consumption. Therefore, it can be ported on small/less-efficient chips with same feature and performance.
    Role:
- RAM Cache design and implantation to reduce NVM writing
- Design and developed proof of concept for Bootloader area utilization
- Developed proof of concept to merge java and native stack.
- Managing team of 5 members
- Code Review

    Technologies Used: Java card 3.0.4 classic, Java card 3.0.5 classic, C, Core Java, Data structure, Algorithm
    Team Size: 6
    Tools used: Morpho Eclipse, VS 2008, Perforce, JIRA

Aug16 to Dec17   **Transaction Management algorithm for Java card operating system** – The algorithm is designed to implement atomicity with minimum overhead in terms of performance and code size.
    Role:
- Designing an algorithm.
- Development of POC
- Support and guide development team in converting design into Code
- Code review
- Defining test plan

    Technologies Used: C, Data structure, Algorithm
    Team Size: 4
    Tools used: Morpho Eclipse, VS 2008, Perforce, JIRA

Jan16 to Jul 16   **Software wear leveling for Java card operating System -** This project is to improve endurance of smart card, which does not provide chip wear leveling. A software wear leveling is concept to arrange data so that write/erase cycles are distributed evenly among all of the blocks (Pages) in the microchip.
    Role:
- Designing software wear leveling concept
- Implementation of swapping mechanism
- Implantation of Defragmentation algorithm
- Defining development and test plan

    Technologies Used: C, Data structure, Algorithm
    Team Size: 7
    Tools used: MORPHO Eclipse, VS 2008, Perforce, JIRA

Jun15 to Dec15 **Java card Operating System --** This is a Java card operating system project implemented using C (native) and java, it provides the platform for global platform java card applications. This OS provide fully support for Global platform 2.1.1, Global platform 2.2.1, Amendment A, Amendment B, Amendment D, Amendment E, Global platform 2.3(some features),UICC and SIM applications on JC222,3.0.1,3.0.2,3.0.4 and 3.0.5 platform.

Role:
- Updated Install command process for better performance and less memory consumption.
- Adapted put key command as per GP2.3
- Implementation some features of Java Card 3.0.4 and Java Card 3.0.5
- Bug Fixing
- Code Optimization
- Performance tuning

Technologies Used: Java card 3.0.4 classic, Java card 3.0.5 classic, C, Core Java, Data structure, Algorithm
Team Size: 22+
Tools used: Morpho Eclipse, VS 2008, Perforce, JIRA

Aug 11 to Feb 15 **A350XWB Landing Gear System (Client: Messier-Bugatti-Dowty) --**

The project is to realize a campaign of High Level Testing for A350XWB Landing Gear System composed of following four sub-systems
1. Landing Gear Extension & Retraction System (LGERS)
2. Braking Control System (BCS)
3. Wheel Steering Control System (WSCS)
4. Landing Gear Monitoring System (LGMS)

LGS (Landing Gear System) is design to control the different functionalities required for Takeoff, Landing and Taxing of the Aircraft during each flight. LGS ensure the safe Takeoff and Landing of Aircraft during Each Flight. The Software HLR Testing Activity of A350 is limited to verification activity of high-level requirements of A350XWB Landing Gear System i.e. verifying all systems (LGERS, BCS, WSCS and LGMS).

Role:
- Inputs Verification.
- High Level Requirement Analysis.
- Sampling of products.
- Doors 9.3 (Requirement management tool) handling and Training related activity.
- Acted as a software developer to implement new features as per requirements.
- Acted as a Responsible engineer for understanding the behavior of test bench and to debug and solve the identified issues.
- Tracking and fixing of the defect found during V&V and communicate the solution to team through defect tracking tool (Redmine).
- Review of the products deliverable to customer.
- Written some of the automation tools for the effective use of simulator.
- Provided training to the team members on system requirement flow and its interface.
- Effectively Involved Preparation and review of technical documents like Test Procedure (TP), Test Library (TL), Test Report (TR), and Test Summary Report (TSR) during project delivery.
- SCADE Analysis
- Mentoring team of 10 + members.

Technologies Used: Embedded C, C++, Data structure
Team Size: 100+
Tools used:
Telelogic DOORS 9.3 for requirement management. SCADE for code development, Python for the Test Script development, CBS Test Bench for the Test Script Execution, CM Synergy for configuring the artifacts and version control, Redmine for defect tracking.

EDUCATION

| 2007–2011 | **BE** in **Computer Science** and **Engineering** from **S.J.C Institute of Technology, Chickballapur** affiliated to **VTU Belgaum** |

DECLARATION

The above statements are true to the best of my knowledge and belief.

Date: 21-03-2021
Place: Noida