* Cat2b
  + Takes two bits and concatenates them. This is used to generate a MUX signal for selecting which way had a hit.
* CatOWord
  + This unit concatenates 8 words into an oword. CatOWord is needed for concatenating all the split words back together for a cache write.
* CatWord
  + This unit concatenates two byes into a word. CatWord is used extensively to splice in a byte or word for writing to a small part of a cache line.
* CatADDR
  + Takes a tag, index, and offset and outputs the address. This is used to reconstruct an address for writing back a cache line to memory.
* SplitOWord
  + Takes an oword and splits it into words. This feature is used for selecting which word to output, based off the offset.
* SplitWord
  + Takes a word and splits it into two bytes. This unit is used for breaking apart a word in a cache line in order to splice in one byte.
* SplitADDR
  + SplitADDR takes an address as input and splits it into the tag, index, and offset bits.
* Splitoffset
  + Takes of offset bits and removes the LSB in order to select which word from a cache line to output.
* Delay6
  + Takes an input signal and buffers by 6ns. This component is used to ensure that the input to dirty, valid, and data arrays are valid while the write signal is propagating through logic gates. This matters when a write is disabled by leaving a control state, but the input to the array changes before the write signal goes low.
* Delay21
  + This unit buffers the input signal by 21ns. This component is used to ensure that the “hit” signal is not generated until the tag has time to propagate through the compare unit. The amount of time corresponds to 5ns for the MDR register, 20ns for the tag array, and 4ns for the compare unit, then that minus the 6ns delay before MREAD\_L or MWRITEX\_L goes low and 2ns for the 3-input AND gate (RW).
* X16b
  + Outputs 16 bits of ‘X’ for debugging purposes. It also serves as a “blank” input because only three of four are used for some four-input MUXs.
* X128b
  + This unit outputs 128 bits of ‘X’ signal in order to facilitate debugging (if two hit lines are high) and cause the wave diagram to be easier to read in regards to DATAIN.
* BitNOT1
  + Takes an input signal and outputs the complement. This is used to get the LRU’ signal for selecting which way to write to, evict, or write back.
* BitAND2
  + This unit outputs the logical AND of two bits. This gate is used in many places to generate control signals.
* BitAND3
  + This unit outputs the logical AND of three bits. This gate is used in many places to generate control signals.
* BitOR2
  + This unit takes a word input and outputs the least significant bit. Its purpose is for choosing between high/low byte for STB and LDB instructions.
* BitNOR2
  + This unit outputs the logical NOR of two bits. This gate is used in many places to generate control signals.
* BitNAND3
  + This unit outputs the logical NAND of three bits. This gate is used in many places to generate control signals.