Lab Experiment 7

Simplification of Logic Circuit Using Karnaugh Map

COMPONENT

Multisim

INTRODUCTION

The basic procedure for combinational logic circuit design is to first develop the truth table that defines the desired function and then from the table, write a simplified SOP expression. The expression can be simplified using various techniques such as Boolean algebra and Karnaugh Mapping. Karnaugh Mapping is a simple and fast procedure for reducing SOP logic expressions and thereby also reducing the implemented circuit's complexity and cost. In Karnaugh mapping, the function is defined graphically. The relationship between the function's inputs and the output are plotted in a Karnaugh Map (K-Map). This will be the same information that would be listed in the truth table for the function. If the K-Map is not properly labeled, the function cannot be correctly simplified and the resulting design will be wrong. With K-Mapping, the function reduction is accomplished by forming appropriate groupings of adjacent 1s in the output. In connection to it, the number of one that each group can have must be in a base of 2, for example, group of $2^4 = 16$, $2^3 = 8$, $2^2 = 4$ 1s, $2^1 = 1$, or $2^0 = 1$ 1's. Then identify the common input variables for the group and write the indicated product term.

Karnaugh Mapping can best be applied to functions with 5 or fewer input variables. There are different ways that a K-Map is organized. Some of the organization of a 3-input K-Map is shown below.

	$\overline{B}\overline{C}$	$\overline{B}C$	BC	$B\overline{C}$
$\overline{A}$				
A				

LABORATORY PROJECT

In this lab you will first design, and implement on a software simulator the following "simplified" traffic light; the simplification of the truth table is done using Karnaugh Mapping.

The project description of a traffic light is as the following:

The vehicular traffic at the intersection of a main street and a cross street is controlled by a traffic light. Vehicle-detection sensors are placed along the lanes D and C of the main road and along B and A of the cross street. When vehicles are detected, the sensors give a HIGH output. When there are no cars detected, the sensor output is LOW. Here are the specifications for the traffic light.

1. The east-west (EW) traffic light will be GREEN whenever both lanes C and D are occupied.
2. The EW light will be green whenever either C or D are occupied but lanes A and B are not both occupied.
3. The north-south (NS) light will be green whenever both lanes A and B are occupied but lanes C and D are not both occupied.
4. The north-south (NS) light will also be green when either A or B are occupied while C and D are both vacant.
5. The east-west (EW) light will be green when no vehicles are present.

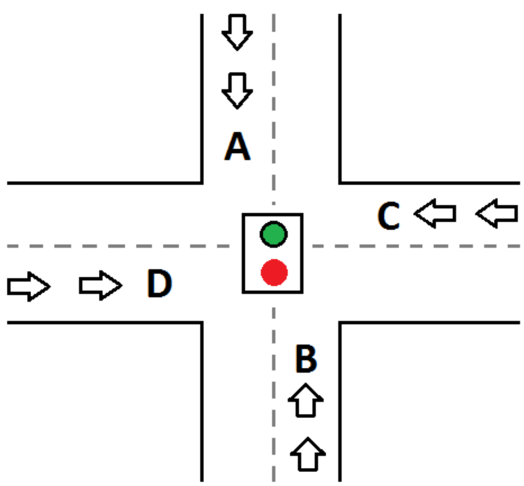


Figure 7.1- Traffic Light schematic

PROCEDURE

Step 1: Complete Table 7.1 according to the description of the simple traffic light. Remember that a logic:

- LOW = No cars detected
- HIGH = Cars detected

Minterm	D	C	B	A	East-West	North-South
0	0	0	0	0		
1	0	0	0	1		
2	0	0	1	0		
3	0	0	1	1		
4	0	1	0	0		
5	0	1	0	1		
6	0	1	1	0		
7	0	1	1	1		
8	1	0	0	0		
9	1	0	0	1		
10	1	0	1	0		
11	1	0	1	1		
12	1	1	0	0		
13	1	1	0	1		
14	1	1	1	0		
15	1	1	1	1		

Table 7.1 Traffic Light Truth Table

Step 2: Use a Karnaugh map (K-Map) to minimize the East-West and North-South equation. Complete the K-map below according to Table 7.1

East-West Karnaugh Map

	$\bar{D}\bar{C}$	$\bar{D}C$	DC	$D\bar{C}$
$\bar{B}\bar{A}$				
$\bar{B}A$				
BA				
$B\bar{A}$				

North-South Karnaugh Map

	$\bar{D}\bar{C}$	$\bar{D}C$	DC	$D\bar{C}$
$\bar{B}\bar{A}$				
$\bar{B}A$				
BA				
$B\bar{A}$				

Write the simplified SOP equation from East-West and North-South

East-West ___________________________ **North-South** _______________________________

Step 3: Once we have the SOP equations, you can pick the equation with fewer ones (East-West or North-South), to build and simulate. Remember:

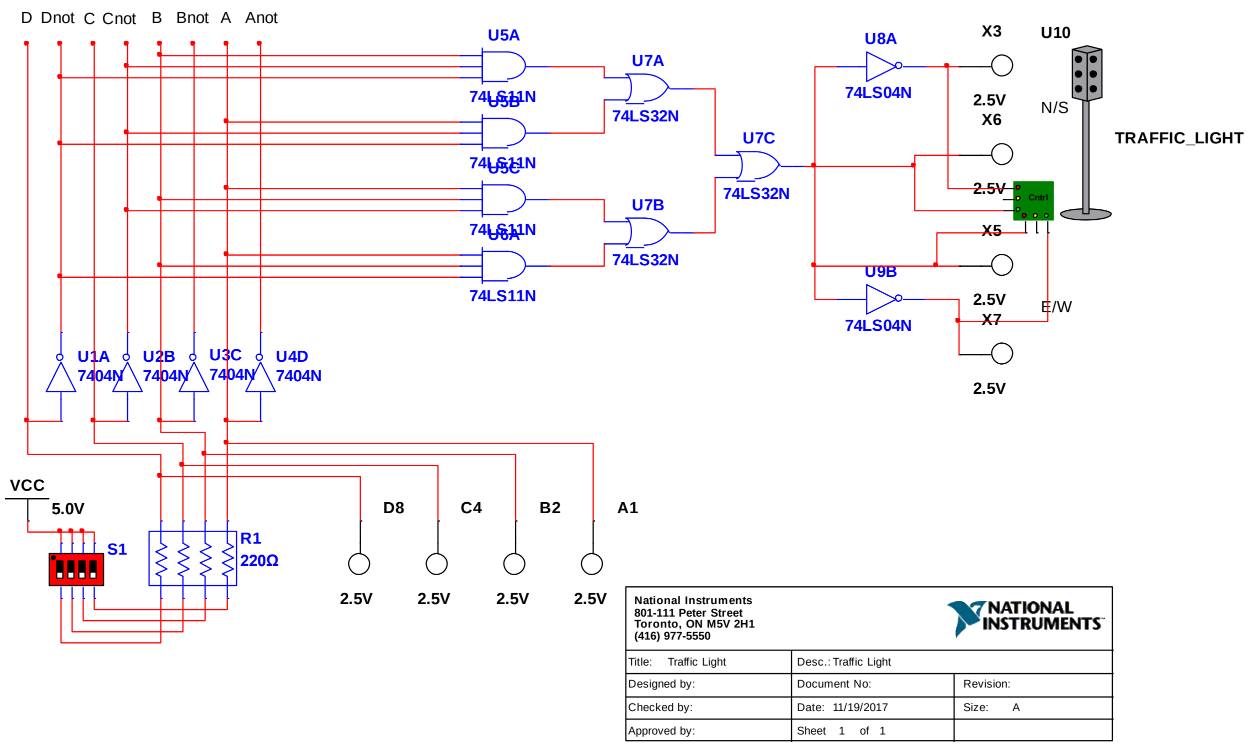
- Simulation of logic inputs = switch
- If you invert the NS output you can create the EW output
- If you invert the EW output you can create the NS output

Write the SOP equation that you are going to use to build the logic circuit: ___________________

Using the selected SOP equation, sketch the circuit schematic below. Call your lab instructor to verify your circuit.

Step 4: Once you have the sketch of the logic circuit, the next step is to build and simulate your circuit using Multisim. Open Multisim, build the logic circuit from **Step 3** in Multisim, and test the output with Table 7.1.

One possible design is shown below:



Demonstrate your simulation to your instructor.

Student's name______________________Lab Instructor's Signature____________________

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