Lab Experiment 11

Data Flip Flops and J-K Flip Flops

The Flip Flop is a bistable (stable in two states) multivibrator. The other two types of multivibrators are the monostable or one shot (stable in one state only) and the astable (not stable) or oscillator. The Flip Flop is the basic memory device because by staying in the state that it was assigned, it "remembers" the last state. In FF talk, when Q=1 the FF is said to be "set" while when Q=0 it is said to be "reset" or "clear." Some Flip Flops may have a reset (or clear) and/or a set line that directly change the output. All Flip Flops change states according to data lines on clock pulses.

All Flip Flops have an output usually labeled Q, the inverse of the output, labeled $\overline{Q}$, a SET, and a RESET.

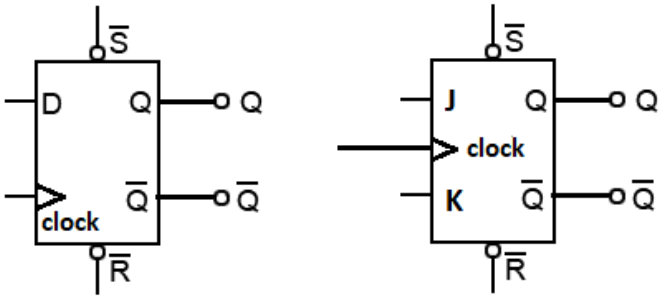
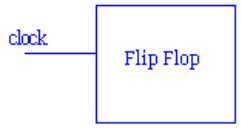
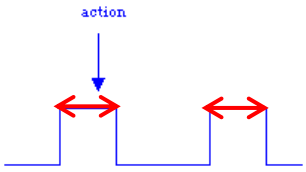
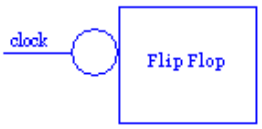
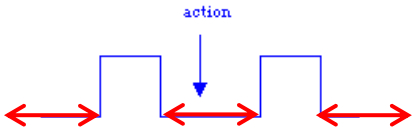
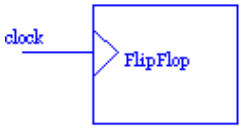
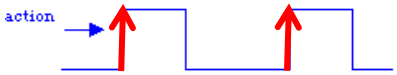
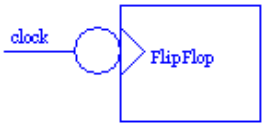
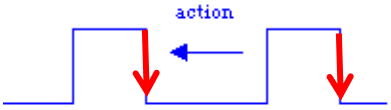


Figure 11.1 – D Flip Flop and JK Flip Flop

The change can take place at one of four times of the clock pulse: when the clock is high, when the clock is low, when the clock is in transition from low to high, or when the clock is in transition from high to low.

Digital clock		
Diagram	**Clock condition for action**	**Explanation**
		State change takes place when clock is **high**
		State changes when clock is **low**
		State changes on the low to high transition (**leading edge**)
		State changes on the high to low transition (**trailing edge**)

The Data Flip Flop (D FF)

The operation of the Data Flip Flop is very simple. The D Flip Flop has one input line usually labeled D. At the active part of the clock pulse whatever data bit (a 0 or a 1) is present on the D line gets passed to the output Q. The term Q_n indicates the *present state*. The term Q_{n+1} indicates the state that the FF will assume at the active portion of the clock pulse. This is usually referred to as the *next state*. An x indicates a "don't care" condition. Here is the truth table for the D FF.

D	Q_n	Q_{n+1}
0	x	0
1	x	1

You will now examine the operation of a 7474 Dual D FF. It is called a Dual FF because there are two FFs in the DIP. Here is the pin assignment diagram for the 7474. Power and ground are at pin 14 and 7. Pins 4 and 10 preset the output. Pins 1 and 13 clear the output. They are both active low. Data presented at 2 and 10 appear at pins 5 and 9 when the clock goes up.

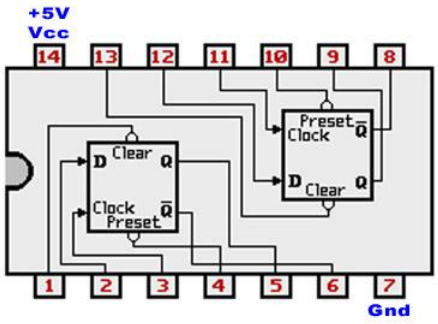


Figure 11.2 – D Flip Flop Pin Number

The J-K Flip Flop

The JK Flip Flop is very versatile. It has two inputs, J and K, it has a clock input, some FFs have pre-clear and pre-set, some have only pre-clear; and of course they have the output Q and its inverse $\overline{Q}$.

The way the JK FF operates is as follows. When the clock strikes, if J and K are both 0, the FF does not change state; if J and K are both 1, the FF toggles; otherwise the FF follows J. Here is the truth table for the 7473 Dual JK FF with pre-clear. This truth table also called the JK FF Operation Table.

$\overline{CLR}$	CLK	J	K	Q_{n+1}	$\overline{Q_{n+1}}$
0	x	x	x	0	1 (clears)
1	↓	0	0	Q_n	$\overline{Q_n}$ (no change)
1	↓	0	1	0	1 (follows J)
1	↓	1	0	1	0 (follows J)
1	↓	1	1	$\overline{Q_n}$	Q_n (toggles)

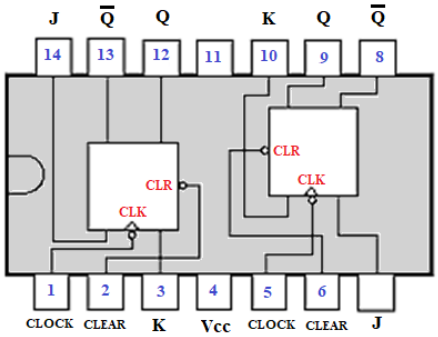
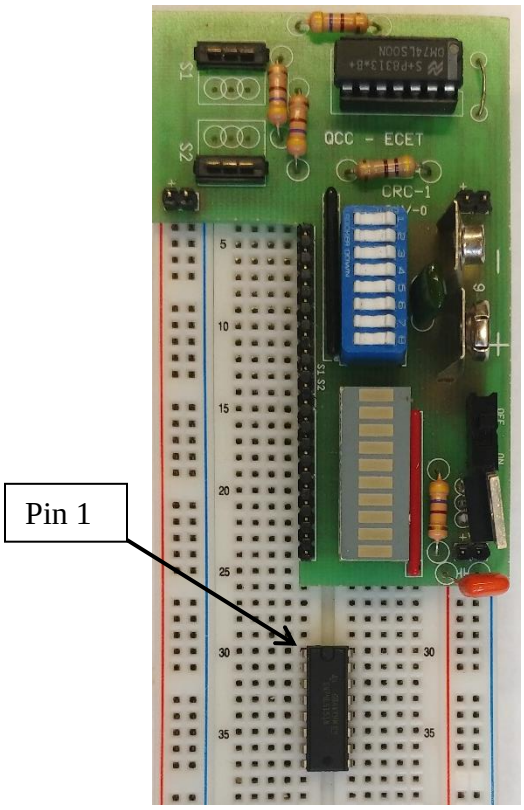


Figure 11.3 – JK Flip Flop Pin Number

Lab Experiment Procedure

Part 1) D Flip Flops

1. Insert the 7474 into the protoboard so that pin 1 of the chip is in hole E30.



2. Connect the battery. Connect pin 7 to ground and pin 14 to + power.
3. Connect pin 5 to LED 1 and pin 9 to LED 2.

   What are the states of LED 1 and LED 2? Explain your answer _____

   _____

   _____

   _____

4. Connect one end of a test jumper wire to ground. With the other end of the test jumper shortly touch pin 1 and then pin 13. Both LEDs should be off.
5. With the other end of the test jumper wire, touch pin 4. What happened to LED 1? _____

   _____

   _____

   _____

6. Now touch pin 10. What happened to LED 2? _____

_____

_____

_____

_____

7. Now clear both FFs by first touching pin 1 and then pin 13. Did both FFs clear? How can you tell that both FFs are clear? _____

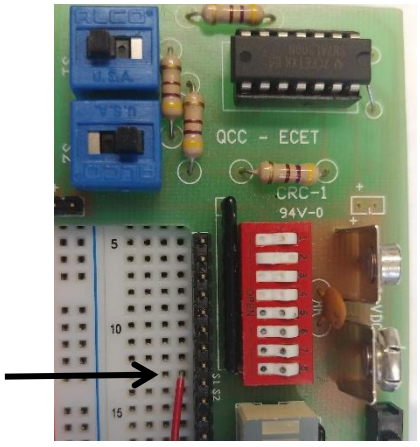
_____

_____

_____

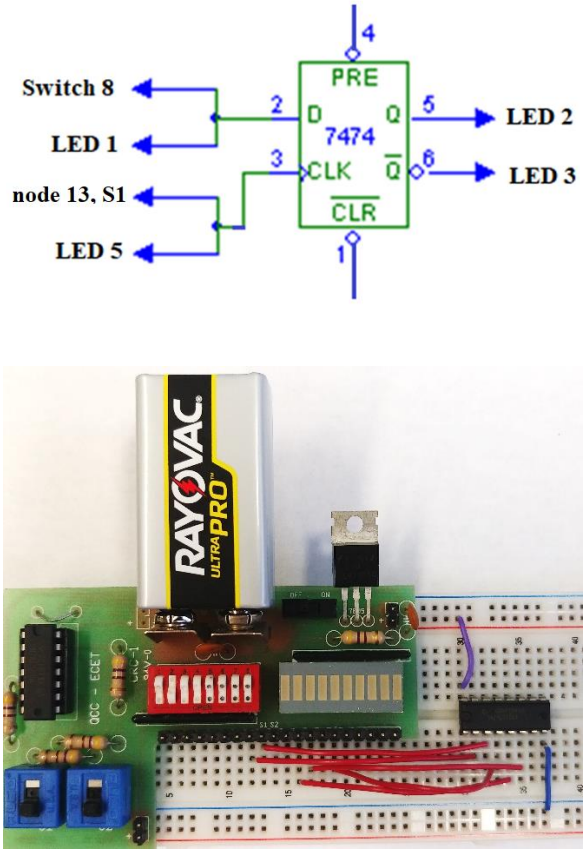
_____

8. Remove the jumper wires between LED 1 and pin 5, and between LED 2 and pin 9.
9. Connect a jumper wire from switch 8 to pin 2. Switch 8 will serve as the Data input.
10. Connect a jumper wire from pin 2 to LED 1. LED 1 is used as the Data input indicator.
11. Connect a jumper from pin 5 to LED 2. LED 2 is used to show the state of the output Q.
12. Connect a jumper from pin 6 to LED 3. LED 3 is used show the state of the inverted output $\overline{Q}$.
13. Connect a jumper wire from S1 (hole D13) to pin 3. This will generate the clock pulse transition when the black slide switch on the left labeled S1 is activated. Slide Switch 1. S1, will be used as the circuit CLOCK.



14. Connect a jumper from pin 3 to LED 5. LED 5 will show the clock action.

You have just set up the following circuit.



Circuit 11.1 – D FFs connection

15. Make sure that the FF is cleared by shortly touching pin 1 with the test jumper to ground.
16. Place a 1 on the D line (on the switch bank, slide switch 8 up.) LED 1 should light.
17. LED 2 should be off (Q=0, FF is clear.)
18. LED 3 should be on because it is the inverse of Q.
19. Slide the CLOCK switch down. Make sure you UNDERSTAND the following BEFORE sliding the CLOCK switch up.
20. In the next step, you are going to slide the CLOCK switch up. Slide the CLICK switch up. Observe that LED 2 goes on as you are sliding it up (leading edge), and LED 3 goes off (it does the inverse.). LED 5 goes on (showing that the clock pulse went high.)
21. Now slide the CLOCK switch down. LED 5 goes off (the clock pulse goes low) but LED 2 stays ON and LED 3 stays OFF.
22. Slide the CLOCK switch up and down, observing what was described in step 19. If you missed it, do a pre-clear (step 15) and slide the CLOCK switch up and down again.
23. Set switch 8 to OFF. Notice that LED 1 went OFF. A zero is now on the Data line.
24. Slide the CLOCK switch up and down. Notice that the 0 from the D line was passed on to the output Q (LED 2 went OFF.)

25. Now that you know how to work the D Flip Flop, first pre-clear the FF (step 15) and then pass the Data bits shown in the following table from D to Q (make sure to set slide switch 8 before you press work the CLOCK). Fill in the Table 11.1

Clock pulse	D	Q
1	**1**	
2	**0**	
3	**1**	

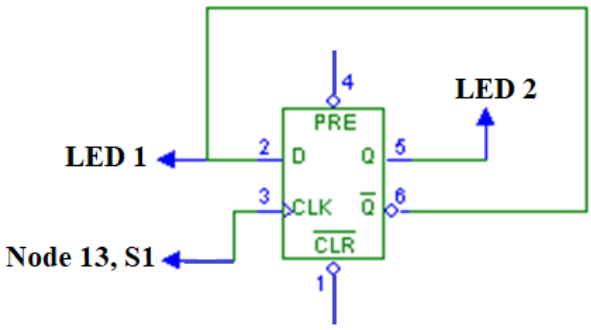
Table 11.1 – D FFs operation

Part 2) The T (toggle) Flip Flop.

A toggle FF responds to a clock pulse by going to its opposite state. Here is the truth table.

Clock pulse	Q_n	Q_{n+1}
↑	0	1
↑	1	0

A toggle FF may be built by simply connecting the $\overline{Q}$ output to the D input. This is so because the next input is always the inverse of the present output. The FF therefore will toggle.



Circuit 11.2 – Toggle Flip Flop pin connection

26. Move the jumper wire from switch 8 to pin 6.
27. Operate the CLOCK switch a few times and notice that the FF toggles. Describe your observations. _____

_____

_____

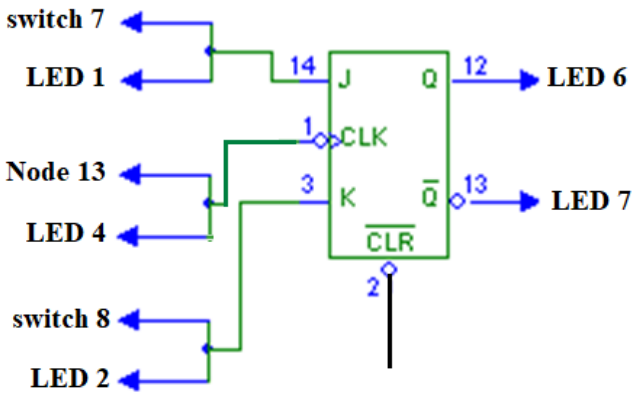
28. Turn the power OFF and remove the 74LS74 and all the wires connected from the protoboard.

Part 3) The JK Flip Flop

Here is the pin assignment diagram for the 74LS73 in *Figure 11.3*. **Note that the power supply connections to +5V is pin 4 and to ground is pin 11.**

29. Insert the 74LS73 into the protoboard with pin 1 in node 30.
30. Connect power and ground: +5V to pin 4 and ground to pin 11.
31. Connect switch 7 to pin 14. Switch 7 is going to control the J input.
32. Connect pin 14 to LED 1. LED 1 is going to monitor the J input.
33. Connect switch 8 to pin 3. Switch 8 is going to control the K input.
34. Connect pin 3 to LED 2. LED 2 is going to monitor the K input.
35. To connect the CLOCK to the circuit, connect pin 1 to node 13, which is S1. Note that the clock will activate the FF during the trailing edge of the clock pulse. In our case, when you slide switch S1 down.
36. Connect pin 1 to LED 4.LED 4 is going to monitor the clock.
37. Connect pin 12 to LED 6. LED 6 is going to monitor the output Q.
38. Connect pin 13 to LED 7. LED 7 is going to monitor the inverse of the output $\overline{Q}$.

    You have just set up the following circuit.



Circuit 11.3 – JK Flip Flop pin connection

39. Set switches 7 and 8 to OFF. To ensure that the FF is clear, connect a jumper to pin 2 and momentarily touch ground. Then connect the jumper from pin 2 to the +5V line.

40. Set switches 7 and 8 according to each setting in the Table 11.2 and for each setting, and then activate the CLOCK. Record the condition of Q (LED 6) and $\overline{Q}$ (LED 7.) Notice that the FF changes states when CLOCK switch slides to zero (trailing edge of the clock pulse.)

JK FF Operation Table					
Inputs				Outputs	
$\overline{CLR}$	CLK	J	K	Q_{n+1}	$\overline{Q_{n+1}}$
1	↓	0	0		
1	↓	0	1		
1	↓	1	0		
1	↓	1	1		

Table 11.2 – JK Flip flop operation table

41. Use the information in Table 11.2 and place the words in Table 11.3:
    - No change
    - Follows J, SET
    - Follows K, RESET
    - Toggle

    To describe what happens when the clock activates the FF with the particular settings for J and K.

Simplified JK FF Operation Table		
J	K	Output Q
0	0	
0	1	
1	0	
1	1	

Table 11.3 – Simplified JK Flip flop operation table

Sometimes we want the JK FF to go into a particular state. The question is, what to do with J and K to force that condition. A table that describes these settings is referred to as the **JK FF Excitation Table**.

42. Using the information from Table 11.2 and 11.3, complete Table 11.4

JK Flip Flop Excitation Table					
Q_n	→	Q_{n+1}	**J**	**K**	**Action**
0	→	**0**			
0	→	**1**			
1	→	**0**			
1	→	**1**			
Table 11.4 – JK Flip flop excitation					

A summary of Table 11.4, could be as:

- To change a 0 to a 0, we can do two things: we can either not change it (J=0, K=0) or we can clear it (J=0, K=1.) So, J has to be a 0 and K doesn't matter.
- To change a 0 to a 1, we can do two things: we can either set it (J=1, K=0) or we can toggle it (J=1, K=1.) So, J has to be a 1 and K doesn't matter.
- To change a 1 to a zero, we can do two things: we can either clear it (J=0, K=1) or we can toggle it (J=1, K=1.) So, J doesn't matter and K has to be a 1.
- To change a 1 to a 1, we can do two things: we can either not change it (J=0, K=0) or set it (J=1, K=0.) So, J doesn't matter and K has to be a 0.

The final JK flip flop excitation table looks as:

JK Flip Flop Excitation Table				
Q_n	→	Q_{n+1}	**J**	**K**
0	→	0	0	X
0	→	1	1	X
1	→	0	X	1
1	→	1	X	0
Table 11.4 – simplified JK Flip flop excitation				

43. Set the JK FF to toggle and operate the clock until the FF is set.

    Now, let's say we want to change the state of the FF to a OFF. According to the Table 11.5, we have to set K to 0, but J can be either a 0 or a 1. So, set switch 8 (K) to 0 and switch 7 (J) to 0.

44. Pulse the clock. Did the state change to 0? _____

_____

_____

_____

45. Set the JK FF to toggle and operate the clock until the FF is SET.

    Repeat step 45 with K=0 and J=1. Did you get the same result? _____

    _____

    _____

    _____

    The JK Excitation Table 11.5 is crucial in designing synchronous counters. We will use it in a future experiment.

46. Disconnect the battery, remove all wires and the IC chip from the protoboard.

Questions

1. On the 74LS74 explain the reasons to leave the PRE-CLEAR and PRE-SET line not connected for normal operation?
2. Explain two steps to clear a current state of a D and JK Flip Flop?
3. According to Circuit 11.1, what type of digital clock operates the D Flip Flip, 74LS74?
4. According to Circuit 11.3, what type of digital clock operates the JK Flip Flip, 74LS73?
5. Explain the reason that the JK Flip Flop is more versatile than a D FF.
6. Why would using a D FF sometimes be better than using a JK FF, or vice versa?
7. If a FF has a PRE-CLEAR and a PRE-SET, both active LOW, why is it a good idea to connect these pins to +5V for normal FF operation?

Student's Name: _____ Lab Instructor's Signature_____

---------- LAB EXPERIMENT ENDS HERE ----------