Lab Experiment 12

Design of Synchronous Counter

INTRODUCTION

Most counters follows a normal binary sequence, although their counting sequences can be somewhat altered, for example, 000, 010,100, 110, …

Several methods exist for designing counters that follow arbitrary sequences, in this exercise, you will be introduced to the design a synchronous counter using J-K flip flops.

In synchronous counters, all of the FFs are clocked at the same time. Before each clock pulse, the J and K input of each FF in the counter must be at the correct level to ensure that the FF goes to the correct state. For example, consider the situation in Table 12.1, when the clock pulse occurs, the J and K inputs of the FFs must be at the correct levels that will cause FF C to change from 1 to 0, FF B from 0 to 1, and FF A from 1 to 1

PRESENT state			**NEXT state**		
C	**B**	**A**	**C**	**B**	**A**
1	0	1	0	1	1

Table 12.1 – Transition state of J-K FF

In order to understand the transition state in a J-K FF, we need to recall the truth table of a J-K FF, Table 12.2

Truth Table of a J-K flip flop			
Input		**Output**	
J	**K**	**Q_{NEXT}**	**Comments**
0	0	Q	No change
0	1	0	Reset
1	0	1	Set
1	1	Q~	Toggle, change state

Table 12.2 – Truth Table of a J-K flip flop

Before we begin the process of designing the decoder circuits for each J and K input, we will first review the operation of the J-K flip-flop using a different approach called an excitation table

as shown in Table 12.3. The column of *Transition at output* shows the possible combination of the transition going from 0 or 1 to the next possible state. The transition of going FROM is known as the *PRESENT state – Q(N),* and the transition of going TO in known as the NEXT state – Q(N+1)

Transition at output	PRESENT State Q(N)	NEXT State Q(N+1)	Comments
0 ➔ 0	0	0	The present state is at 0 and is to remain at 0 for the NEXT state According to Table 10.2: J = 0, K= 0 ➔ Q_{NEXT} = 0 (No change) J = 0, K =1 ➔ Q_{NEXT} = 0 (Reset) **J = 0, K=Don't care**
0 ➔ 1	0	1	The present state is at 0 and the NEXT state is 1 According to Table 10.2: J = 1, K= 0 ➔ Q_{NEXT} = 1 (Set) J = 1, K =1 ➔ Q_{NEXT} = 1 (toggle) **J = 1, K=Don't care**
1 ➔ 0	1	0	The present state is at 1 and the NEXT state is 0 According to Table 10.2: J = 0, K= 1 ➔ Q_{NEXT} = 0 (Reset) J = 1, K =1 ➔ Q_{NEXT} = 1 (toggle) **J = Don't care, K=1**
1 ➔ 1	1	1	The present state is at 1 and the NEXT state is 1 According to Table 10.2: J = 0, K= 0 ➔ Q_{NEXT} = 1 (No change) J = 1, K =0 ➔ Q_{NEXT} = 1 (Set) **J = Don't care, K = 0**

Table 12.3 – J-K FF excitation table

From the Comments on Table 12.2 we can find the inputs for J and K as shown in Table 12.4. For this case, the ***don't care*** state is represented with a ***X***

Transition at output	PRESENT State Q(N)	NEXT State Q(N+1)	J	K
0 ➔ 0	0	0	0	X
0 ➔ 1	0	1	1	X
1 ➔ 0	1	0	X	1
1 ➔ 1	1	1	X	0

Table 12.4 – J-K FF excitation table

Having and understanding Table 12.4, we can start the design of a synchronous counter.

PART 1 – CREATING A SYNCHRONOUS COUNTER TO DISPLAY 0,1,2,3, AND 4

Step 1: Write the sequence of the synchronous counter, for this experiment, we are going to design a synchronous counter that will display 0, 1, 2, 3, and 4. For this, we can draw a transition state as Figure 12.1

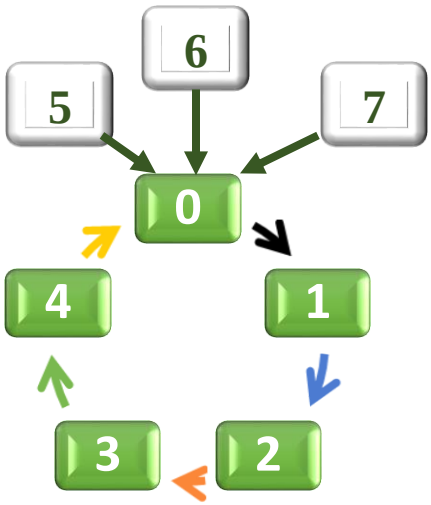


Figure 12.1 – Synchronous Counter Sequence

Step 2: Determine the number of flip flops that you need. Since 4 is the highest number (100_2 = 4), then we need three flip flops, one flip flop per bit. Name the Least Significant flip flop A and the Most Significant flip flop C

Step 3: Construct a truth table of the transition state with the PRESENT state and the NEXT state.

PRESENT state			NEXT state		
C	**B**	**A**	**C**	**B**	**A**
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	0	0	0
1	0	1	0	0	0
1	1	0	0	0	0
1	1	1	0	0	0

Table 12-5 – State table

Step 4: Use the excitation Table 12.4 to complete the J-K input for each flip flop

PRESENT state			NEXT state			J-K State					
C	**B**	**A**	**C**	**B**	**A**	**J_C**	**K_C**	**J_B**	**K_B**	**J_A**	**K_A**
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	0	0	0	X	1	0	X	0	X
1	0	1	0	0	0	X	1	0	X	X	1
1	1	0	0	0	0	X	1	X	1	0	X
1	1	1	0	0	0	X	1	X	1	X	1

Table 12.6 – Circuit excitation table

Step 5: Using Table 12.6, design the logic circuits needed to generate the levels required at each J and K input. For this, you create a k-map table for each J and K input and find the SOP equation of each.

J_C

	$\overline{C}$	C
$\overline{A}\overline{B}$	0	X
$\overline{A}B$	0	X
AB	1	X
$A\overline{B}$	0	X

SOP : **AB**

J_B

	$\overline{C}$	C
$\overline{A}\overline{B}$	0	0
$\overline{A}B$	X	X
AB	X	X
$A\overline{B}$	1	0

SOP: $A\overline{C}$

J_A

	$\overline{C}$	C
$\overline{A}\overline{B}$	1	0
$\overline{A}B$	1	0
AB	X	X
$A\overline{B}$	X	X

SOP: $\overline{C}$

K_C

	$\overline{C}$	C
$\overline{A}\overline{B}$	X	1
$\overline{A}B$	X	1
AB	X	1
$A\overline{B}$	x	1

SOP : **1**

K_B

	$\overline{C}$	C
$\overline{A}\overline{B}$	X	X
$\overline{A}B$	0	1
AB	1	1
$A\overline{B}$	X	X

SOP: **A**+**C**

K_A

	$\overline{C}$	C
$\overline{A}\overline{B}$	X	1
$\overline{A}B$	X	1
AB	X	1
$A\overline{B}$	X	1

SOP: **1**

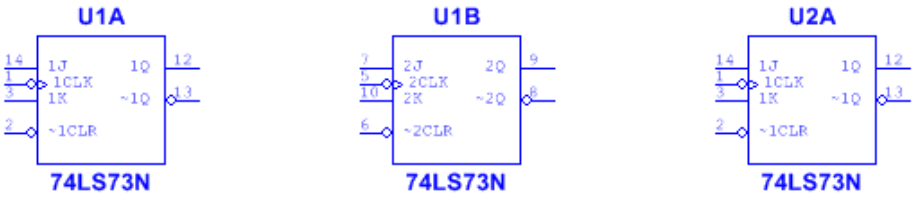
Step 6: Complete and sketch the counter circuit using the SOP equation found in **step 5.** Draw the schematic below.

To build the circuit, the J-K FF can be found in Group: TTL, Family: 74LS, Component: 74LS73N, which is a DUAL JK FLIP FLOP-NO PRESET. Since it is a 3-bit counter, we will need three JK FF.

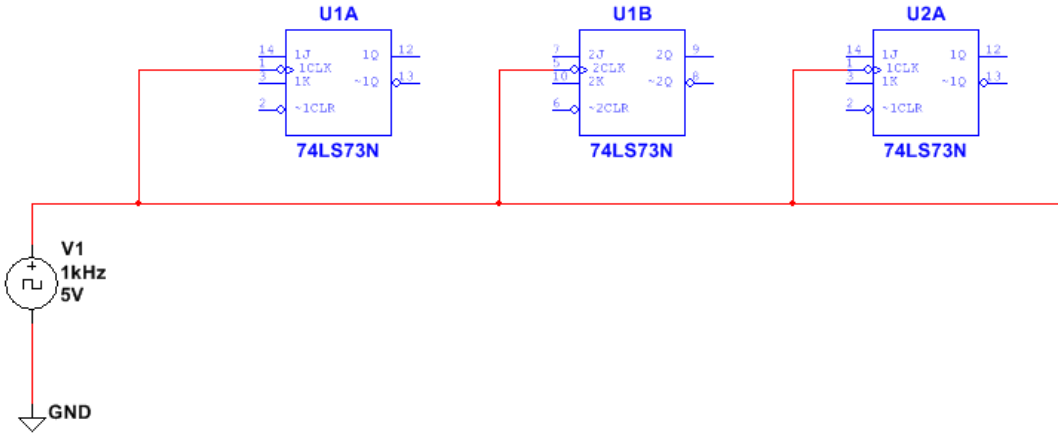
According to the design of this counter, the components and basic components that you need are:

- Voltage pulse (Group: Source, Family: Signal Voltage Sources, Component: Clock_Voltage)
- Digital Ground (Group: source, Family: Power_Source, Component: DGND)
- 5 volts VCC (Group: source, Family: Power_Source, Component: VCC)
- Two AND gate (Reference from previous lab)
- One OR gate (Reference from previous lab)
- Three JK flip flops (Group TTL, Family: 74LS, Component: 74LS73)
- Three Red Probe for each bit of the circuit (Group: Indicators, Family: Probe, Component: RED Probe)

✓ Open multisim and save the mulsim file as "Lab10_sample"
✓ Place three 74LS73N in your workspace in multisim

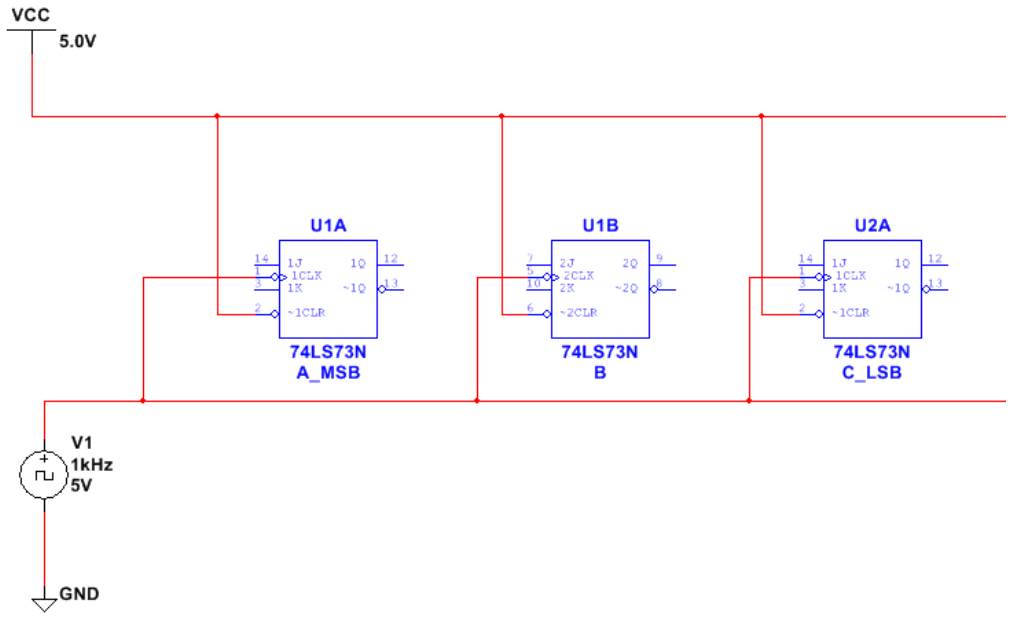


✓ Insert a Voltage Clock in your workspace and change the frequency to 1 Hz.
✓ Insert a Digital Ground
✓ Make the proper connection to generate a synchronous counter

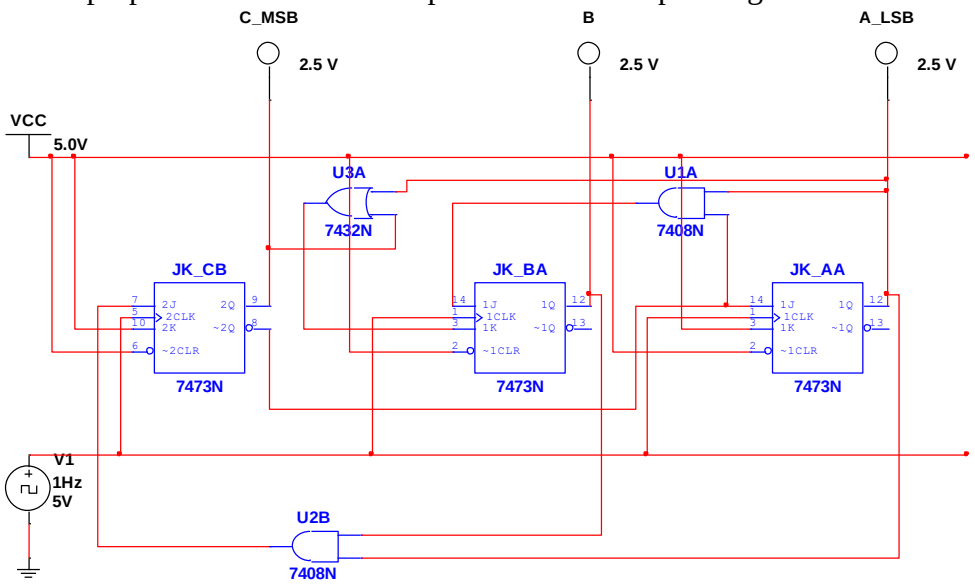


✓ Double click on the first FF, which is the one next to the clock, and label it as "A_MSB", the second FF label it as "B", and label the last FF as "C_LSB"

- ✓ Insert a VCC of 5 V
- ✓ Make the proper connection to the *Clear* "CLR" input of the FF



- ✓ Make the circuit connection according to the SOP equation of input J-K of each FF
- ✓ Insert three Red Probe for each bit of the circuit
- ✓ Double click on one probe and change the label name to "A_LSB", the other one to "B", and the last one to "C_MSB"
- ✓ Make the proper connection of each probe to its corresponding FF.



- ✓ RUN your simulation to make sure that your counter is working property
- ✓ Save your work

LAB EXPERIMENT PROCEDURE

PART 2 – CREATE A SYNCHRONOUS COUNTER TO DISPLAY 2, 3, 1, 7, 6, 5, 4, 0

Using each of the steps from Part 1, you will create a synchronous counter that will display the following sequence: 2, 3, 1, 7, 6, 5, 4, 0.

Step 1: Write and sketch the sequence of the synchronous counter

Step 2: Determine the number of flip flops that you need

Step 3 and 4: Construct a truth table of the transition state with the PRESENT state and the NEXT state, and complete the J-K input for each flip flop

PRESENT state			NEXT state			J-K State					
C	**B**	**A**	**C**	**B**	**A**	J_C	K_C	J_B	K_B	J_A	K_A
0	**0**	**0**									
0	**0**	**1**									
0	**1**	**0**									
0	**1**	**1**									
1	**0**	**0**									
1	**0**	**1**									
1	**1**	**0**									
1	**1**	**1**									

Table 12.7 – Circuit excitation table for sequence 2, 3, 1, 7, 6, 5, 4, 0

S**tep 5:** Create a k-map table for each J and K input and find the SOP equation of each.

J_C

	$\overline{C}$	C
$\overline{A}\overline{B}$		
$\overline{A}B$		
AB		
$A\overline{B}$		

SOP :

J_B

	$\overline{C}$	C
$\overline{A}\overline{B}$		
$\overline{A}B$		
AB		
$A\overline{B}$		

SOP:

J_A

	$\overline{C}$	C
$\overline{A}\overline{B}$		
$\overline{A}B$		
AB		
$A\overline{B}$		

SOP:

K_C

	$\overline{C}$	C
$\overline{A}\overline{B}$		
$\overline{A}B$		
AB		
$A\overline{B}$		

SOP :

K_B

	$\overline{C}$	C
$\overline{A}\overline{B}$		
$\overline{A}B$		
AB		
$A\overline{B}$		

SOP:

K_A

	$\overline{C}$	C
$\overline{A}\overline{B}$		
$\overline{A}B$		
AB		
$A\overline{B}$		

SOP:

Step 6: Open a Multisim file and save it as "LastName_Lab12". Complete your counter circuit according to each SOP equation from **Step 5**

Note: remember that this counter you are going to use for your final project, make sure that you save it as "LastName_Counter"

Student's Name_____Lab Instructor's Signature _____

---------- **LAB EXPERIMENT ENDS HERE** ----------