Guowei Sun

Master of Computer Technology

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Education

Master of Computer Technology *University of Science and Technology of China* **Anhui, CHINA** *2021-2024*
Related Courses: Theories and Design of Distributed Algorithms, Machine Learning, Deep Learning, Advanced Computer Networks, etc.
GPA:3.33/4.3

Bachelor of Computer Science and Technology *China University of Petroleum (Beijing)* **BeiJing, CHINA** *2017-2021*
Related Courses: Data Structures, Software Engineering, Design Patterns, and other core computer science courses
GPA:83/100

Research Experience

Research on the design of the EDA algorithm based on computational geometry and artificial intelligence. Focus on back-end design in graph theory algorithms, studying Placement, Global Routing and Clock.

- **Timing-Rectilinear Steiner Tree,** *IEEE PDF* **Anhui, China** *1/2023 - 06/2023*
The objective of this problem is to achieve the optimal trade-off between the shortest distance(timing) and the total length(routing resources) in a Steiner rectilinear tree. Attaining the best trade-off is a critical goal in chip design. We obtained the best Pareto curve by utilizing reinforcement learning and graph geometric training.

- **Skew-Rectilinear Steiner Tree,** *Contest github,* **Anhui, China** *12/2023 - 06/2024*
First place in OpenROAD competition with research on routing based on skew-cost minimization, awarded **$2500**. The competition is supported by UCSD, OpenRoad and DARPA. The related paper was accepted at DAC 2025(to appear, **first author**).

Publications

- **Towards Timing-Driven Routing: An Efficient Learning-Based Geometric Approach** **SF, USA** *ICCAD 2023*
Liying Yang*, **Guowei Sun***, Hu Ding (* first co-author)

- **To Tackle Cost-Skew Tradeoff: An Adaptive Learning Approach** **SF, USA** *DAC 2025*
Guowei Sun, Lin Chen, Qiming Huang, Hu Ding

Working Experience

- **Univista,EDA R&D Software Engineer** **Shanghai, China** *7 /2024 - present*
Focused on the **Prototyping** and **Emulation** processes of chip design, particularly the mapping of circuits from ASIC to FPGA. Specialized in optimizing clock-related issues, including reducing skew in clock paths to enhance circuit operating frequency. Additionally, he contributed to improving the compilation speed of EDA software through graph algorithmic and workflow optimizations.

- **Huawei(Intern),Software Development Engineer** **Shanghai, China** *7 /2023 - 9 /2023*
Worked on the development of Linux kernel and Android audio drivers for new chips like HiSilicon; refactored device management and audio algorithm mode switching in the proprietary normalized HAL layer using the Abstract Factory pattern.

- **iFlytek(Intern), Assistant Research Algorithm Engineer** **Hefei, China** *2/ 2023 - 4/ 2023*
Conducted research on natural language understanding and reinforcement learning for medical dialogue models, handling real doctor-patient dialogue data from the First Affiliated Hospital of USTC.

Award & Certifications

- **Outstanding Graduate of USTC, 2024**
- **English**: CET6-500.
- **Mathematics**: First Prize in Beijing Mathematics Competition; Second Prize in National College Students' Mathematics Competition.
- **First Prize** in USTC Academic Scholarship twice, Second Prize once; continuous scholarship recipient throughout undergraduate studies.
- **Competitions**: Top 10% in CCF Personal Credit Default Prediction (out of 4000 teams); Top 6% in Ali Tianchi NLP Competition (out of 3600 individuals); Third Prize in Logistics Robot Competition at the university level.