Comprehensive Analysis of Jitter Modeling Techniques and High-Speed Data Transmission Challenges in Chiplet-Based Architectures

MRUDHULESH KURAPATI

1226364206

mkurapat@asu.edu

Abstract **The transition to chiplet-based architectures marks a significant evolution in semiconductor design, offering enhanced scalability and integration flexibility compared to traditional monolithic System-on-Chips (SoCs). This paper presents a groundbreaking approach to jitter modeling that addresses the unique challenges of high-speed data transmission within these complex systems. By developing a bespoke behavioral jitter model, this research delves into the impact of power supply fluctuations and intricate circuit interactions on system performance. Utilizing response surface methodology, we systematically analyze how design parameters such as power supply frequencies and noise amplitudes affect jitter accumulation, providing a path to optimized configurations. Our findings are validated in real-world High Bandwidth Memory systems, demonstrating substantial improvements in system reliability and data integrity. This study not only advances the theoretical understanding of jitter dynamics in chiplet-based systems but also offers practical insights for designing more robust semiconductor architectures in an era of increasing system complexity.**

INTRODUCTION

The relentless scaling down of semiconductor devices has encountered substantial physical and economic barriers, prompting the industry to adopt innovative approaches to continue performance enhancements while managing costs. One such paradigm is the use of chiplet-based architectures, where multiple discrete components or chiplets are interconnected within a single package to form a complete system. This modular approach not only leverages the benefits of different semiconductor technologies but also circumvents the yield and cost issues associated with monolithic designs. Despite these advantages, the integration of chiplets introduces complex challenges in high-speed data transmission, particularly in maintaining signal integrity across heterogeneous interfaces.

For high-performance heterogeneous systems featuring multiple dies, effective communication via larger parallel interconnects requires robust designs in both signal integrity and power integrity. Although the channels between these dies are short, simplifying some aspects of signal integrity, the substantial increase in transient current and a unique clocking architecture present major challenge. These conditions amplify supply noise and timing jitter, which become the primary constraints in the system design.

Additionally, high-speed interconnects between chiplets are susceptible to various signal integrity issues, with jitter being particularly harmful. Jitter is the deviation from true periodicity of a presumably periodic signal and can be caused by numerous factors such as power supply noise, electromagnetic interference, and crosstalk. In chiplet architectures where data rates can exceed tens of gigabits per second, even slight jitter can lead to significant data corruption, increased error

rates, and overall system instability. These interconnected challenges highlight the need for meticulous design consideration in both signal and power integrity to ensure reliable system performance.

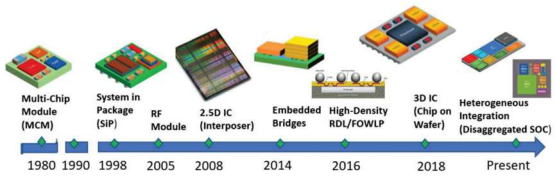

Figure 1Chiplet Implementation Evolution Timeline.

The focus of existing research has predominantly been on identifying the sources and impacts of jitter within traditional monolithic ICs. However, the unique configuration and interconnection schemes of chiplets demand a re-evaluation of these models. This research aims to bridge this gap by developing a comprehensive jitter model specifically tailored for high-speed data transmission between chiplets [1]. This model will not only consider the conventional sources of jitter but also the specific interconnect technologies and material properties inherent to chiplet assemblies.

By conducting a detailed analysis of the proposed jitter model, this paper seeks to achieve several objectives: firstly, to quantify the impact of jitter on system-level performance in chiplet-based designs; secondly, to identify critical thresholds where jitter becomes detrimental to data integrity; and thirdly, to propose effective strategies for jitter mitigation [1]. These strategies may include but are not limited to, advanced signal conditioning techniques, improved clock distribution methods, and optimization of interconnect layout. The outcomes of this study are expected to provide crucial insights that can guide the design and development of future chiplet-based systems, ensuring robust and efficient performance even at extreme data transmission rates.

This investigation not only contributes to the theoretical understanding of jitter in advanced semiconductor architectures but also serves a practical purpose by offering actionable solutions to enhance the reliability and efficiency of emerging chiplet-based technologies.

EVOLUTION AND INTEGRATION OF CHIPLET TECHNOLOGIES:

Enhancing system performance and scalability

The evolution of chiplet technology has been marked by significant milestones, starting with the introduction of multi-chip modules (MCM) in the 1980s, progressing to systems in package (SiP), and later, 2.5D IC interposer technologies around 2008. Subsequent developments such as embedded multi-die interconnect bridge (EMIB) and fan-out wafer-level packaging (FOWLP) have further refined integration techniques. More recently, the adoption of high bandwidth memory (HBM) using 3D IC integration via through-silicon vias (TSV) highlights advances toward more complex implementations. Presently, the focus on heterogeneous integration and the disaggregation of system on chips (SoCs) brings notable advantages such as improved subsystem yield, decreased market development times, cost reductions, and the ability to choose the best-suited process nodes for specific IP functionalities[5].

However, the technology faces significant challenges, especially in managing the speed and latency of data transmission between chiplets, which are crucial for maintaining system performance. Solutions like organic and silicon interposers, along with EMIB, are essential for facilitating efficient chip-to-chip communication, though they present various compromises in terms of routing density, presence of power layers, and the balance between cost and performance.

Organizations across the industry and various government entities, including the Open Compute Project/Open Domain-Specific Architecture (OCP/ODSA) and the Universal Chiplet Interconnect Express (UCie) consortium, are diligently working towards creating strong chiplet ecosystems. Their efforts focus on streamlining the integration process from silicon fabrication to package assembly, enhancing thermal design, conducting tests on known good dies (KGD), and standardizing process design kits (PDKs) as well as interconnection interfaces.

In typical high-speed systems, an Si interposer equipped with network chips and HBM technology might be used, where CMOS chips are attached

using micro bump technology. This interposer is then mounted on an organic package using Controlled Collapse Chip Connection (C4) technology, and the package usually employs a ball grid array (BGA) configuration. This setup enables intensive routing connectivity between processors and HBMs, thereby boosting system efficiency and facilitating the quick introduction of new products by incorporating pre-verified SoCs or memory chips[16].

Heterogeneous System:

A heterogeneous system refers to a computing system that integrates different types of processors or components, each optimized for specific types of tasks. For example, a system might include a CPU (Central Processing Unit) for general-purpose processing, a GPU (Graphics Processing Unit) for graphics and parallel processing, and specialized accelerators for tasks like AI or data analysis. These components work together to improve overall performance and efficiency.

The key idea is to use the best-suited hardware for each type of task, thereby improving performance and energy efficiency compared to using a single type of processor for all tasks.

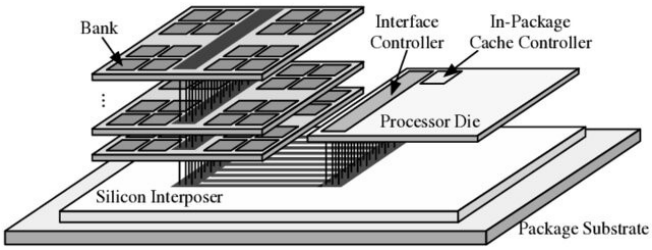

Figure 2Cross-sectional diagram showing a semiconductor package with heterogeneous integration and High Bandwidth Memory (HBM) on a silicon interposer for enhanced performance.

High Bandwidth Memory (HBM):

HBM is a type of memory technology used in computers to provide high-speed access to large amounts of data. It is typically used in high-performance computing environments, like those needing fast graphics processing (such as in GPUs).

HBM stacks several memory dies on top of one another, connecting them with through-silicon vias (TSVs). This configuration allows for much wider interfaces and faster data transfer rates compared to traditional memory types like DDR SDRAM. HBM is directly attached to the processor via an interposer, which significantly reduces data transfer latency and increases bandwidth [16].

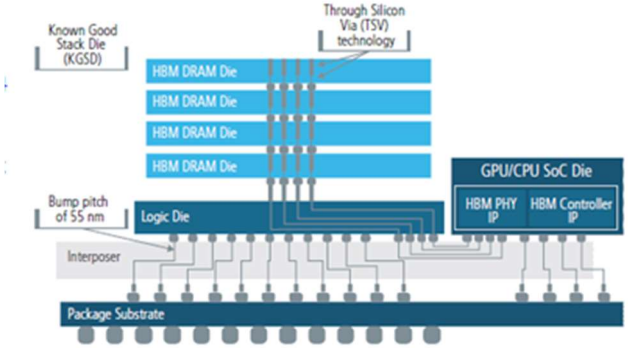

Figure 3 The image shows a semiconductor package with stacked DRAM and a GPU/CPU SoC die connected by Through Silicon Via (TSV) technology.

In essence, a heterogeneous system is about combining different computing technologies to optimize performance, whereas HBM is a specific high-performance memory technology used within such systems to enhance data handling capabilities.

This extensive integration of chiplet technologies represents a strategic pivot towards more modular and adaptable electronic systems, promoting customization and fostering innovation within the semiconductor industry.

JITTER IN CHIPLET ARCHITECTURES:

Jitter in the context of chiplets can be categorized mainly into two types: timing jitter and phase jitter. Timing jitter refers to the variation in when a signal's edge (transition from high to low or vice versa) arrives compared to when it was expected. Phase jitter, a subset of timing jitter, specifically relates to variations in the phase of a periodic signal. In chiplets, these variations can arise from several sources including thermal noise, power supply fluctuations, electromagnetic interference, and cross-talk from adjacent signal paths.

Impact on High-Speed Data Transmission:

In high-speed data transmissions, such as those between different chiplets within a system, the rate at which data can be reliably transmitted is heavily

dependent on the precision of the timing of these transmissions. Jitter can introduce errors in the interpretation of data bits. For instance, if a data bit's arrival time fluctuates significantly due to jitter, the receiver might misread the bit's value, particularly at high transmission rates where the time windows for reading each bit are very short.

Managing Jitter in Chiplets:

Effective jitter management involves several strategies:

1. Use of High-Quality Clock Sources: Employing precision oscillators that have low intrinsic jitter can help in reducing the overall system jitter.

2. Signal Integrity Engineering: Designing traces and circuits to minimize reflections, crosstalk, and noise can help in maintaining signal clarity and reducing jitter.

3. Buffering and Retiming: Using phase-locked loops (PLLs) and delay-locked loops (DLLs) in the circuit design can align signal timing accurately across the different parts of a chip or between different chiplets.

4. Error Correction Coding (ECC): Implementing ECC can help in detecting and correcting errors that may occur due to jitter, ensuring reliable data transmission.

In chiplet-based systems where high-speed inter-chiplet communication is crucial, managing jitter is essential for maintaining data integrity and overall system performance. As data rates continue to increase, the impact of jitter grows, and sophisticated techniques are required to mitigate its effects. This ensures that chiplet systems can meet the performance and reliability expectations of modern high-performance computing applications.

EXPLORING THE DYNAMIC INTERPLAY BETWEEN SUPPLY NOISE AND JITTER IN GIGABIT I/O INTERFACES

In the realm of high-speed data communications, maintaining signal integrity is of paramount importance. Gigabit Input/Output (I/O) interfaces, which facilitate rapid data transfer across various platforms, are particularly susceptible to issues like jitter. Jitter refers to the variability in the timing of a digital signal's edges, which can severely impact the performance of communication systems by introducing errors and causing loss of synchronization. This essay delves into the intricate relationship between supply noise and jitter within Gigabit I/O interfaces, highlighting the critical need for robust design to mitigate these effects.

Jitter manifests in two main forms: random and deterministic. Random jitter, unpredictable and irregular, poses a significant challenge due to its nature, while deterministic jitter, being predictable and repeatable, can be managed more effectively if properly understood. The origins of jitter are deeply tied to the presence of supply noise, which itself can come from a variety of sources. Common culprits include fluctuations in power supplies, electromagnetic interference from other devices, and thermal noise inherent within electronic components. Each of these sources has the potential to introduce undesirable variations in circuit voltages and currents, thereby exacerbating jitter.

The impact of supply noise on jitter is not straightforward and involves various dynamics including the design of the circuit and the specific characteristics of the noise. For instance, a fluctuating power supply might affect the timing accuracy of the circuit's clock, which in turn increases jitter. Theoretical models and simulations often serve to illustrate these effects, helping engineers predict and quantify jitter under different scenarios. This predictive capacity is crucial for developing effective mitigation strategies, which can include both design alterations and component selections geared toward noise reduction.

Engineers employ several techniques to mitigate the impact of supply noise on jitter. Designing robust power supply circuits with comprehensive filtering and stabilization features is one common approach. Additionally, using components that inherently produce less noise and optimizing the physical layout of circuits to shield them from external noise sources can be effective. These strategies necessitate a profound understanding of both circuit design and the physics of noise, highlighting the interdisciplinary nature of challenges in digital communications engineering.

The research paper by Schmitt et al., titled "Investigating the Impact of Supply Noise on the Jitter in Gigabit I/O Interfaces," offers a case study in this complex interplay. Through advanced circuit simulation and meticulous noise measurement, the researchers explore how different noise generators influence jitter. Their work sheds light on the multifaceted nature of this issue, demonstrating that effective mitigation requires a combination of theoretical knowledge, practical engineering skills, and rigorous experimental approaches.

Looking ahead, the field of digital communications continues to evolve, with new challenges and opportunities emerging in tandem with advancements in technology. Future research might focus on developing new materials with superior electrical properties, crafting more sophisticated simulation tools that can more accurately forecast noise impacts, or innovating circuit designs that are inherently less susceptible to noise. Each of these avenues holds the promise of further reducing jitter, thus enhancing the reliability and efficiency of high-speed digital communications. Understanding and managing the effects of supply noise on jitter is crucial for the advancement of communication technologies. The integrity and performance of Gigabit I/O interfaces, critical to modern communication infrastructures, depend heavily on our ability to control these phenomena. Through ongoing research and innovation, strategies that effectively mitigate jitter can ensure the stability and performance of our digital communication systems. This exploration not only highlights the complexities involved but also underscores the essential nature of continual improvement in the technologies that underpin our connected world.

HIGH-SPEED SIGNALING ENHANCEMENTS THROUGH INTERPOSER INTEGRATION

A heterogeneous system that incorporates either an organic or silicon interposer along with EMIB features 2.5-D/3-D integrated circuits with ASIC/FPGA dies, leveraging HBM technology. Organic interposers are known for their extensive substrates with fine-pitch and fine-line interconnections. In comparison, silicon interposers and EMIBs are favoured in high-performance settings due to their superior interconnect precision, though organic substrates are advantageous for their lower signal conductor and dielectric losses. This attribute significantly reduces resistive losses and signal crosstalk, key factors that critically influence the reliability and efficiency of sophisticated electronic systems[5].

A standard silicon interposer setup includes a one-sided redistribution layer (RDL) that comprises multiple layers and through-silicon vias (TSVs). This arrangement features three copper conductor layers, each designed for specific signal and power mesh functions. The TSVs, notable for their 10 µm diameter and 0.5 µm insulation thickness, provide a highly accurate and compact interconnection framework. This refined configuration enhances tight routing and robust communication among high-performance components such as processors, transceivers, and HBM dies. Such setups are vital for preserving signal integrity, crucial for high-speed data transmission and reducing latency in comprehensive digital networks, spanning varied distances and packaging scenarios[2 - 4].

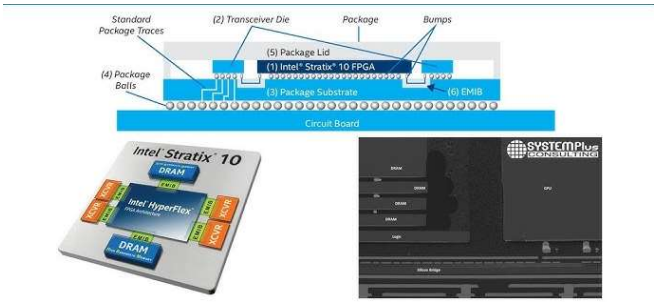

Figure 4 The image illustrates Intel's EMIB technology in a semiconductor package, detailing component integration and connectivity.

Conversely, the silicon bridge, or EMIB, eschews TSVs and is integrated within the package, utilizing micro bumps to link signal and power/ground planes across silicon dies. The EMIB boasts a complex structure with four metallization layers—two for signals and one each for power and ground. The strategic placement of microvias through the power/ground mesh layer facilitates direct connections to the I/O ports on neighbouring chips. The ground layer serves both as a signal reference and an effective barrier, minimizing electromagnetic disruptions and boosting signal clarity. This shielding is crucial as it significantly reduces signal interference primarily caused by close proximity of signal lines.

The design is adept at managing signal interactions within and between layers, ensuring the integrity and functionality of intricate multi-layered electronic configurations.

CHANNEL ANALYSIS IN DENSE INTERCONNECT ENVIRONMENTS

In environments where numerous signal interconnects are densely packed within a small area, such as in organic or silicon interposers, various coupling mechanisms are at play. Due to the confined space, signal microbumps are closely packed, and the number of ground signals providing reference is often limited. This necessitates a thorough analysis of the coupling effects between power and signal nets, as power-to-signal coupling can significantly contribute to noise and jitter in both interposer types and EMIB systems [15].

The signal integrity of three types of second-level interconnects—organic interposers, silicon interposers, and EMIB—is evaluated based on the dimensions and material properties. In each implementation, two signal traces are positioned adjacent to power and ground traces. The measured insertion loss for these implementations indicates that the silicon interposer experiences higher attenuation, attributable to its aggressive design rules and the smaller cross-sectional area of its traces, which increases dc loss. However, as indicated in the analysis, the crosstalk in the silicon interposer setup is effectively minimized through the strategic use of ground and power traces as shielding, despite the fact that these planes are hatched. This setup underscores the critical role of careful layout and shielding in maintaining signal integrity in densely populated interconnect environments [7].

ADVANCED SIMULATION TECHNIQUES FOR DIE-TO-DIE INTERFACE ANALYSIS

Die-to-die interfaces distinguish themselves from conventional memory interfaces and SerDes links through several unique operational characteristics. These interfaces typically possess extensive I/Os that lack impedance control and are intentionally designed to closely interact with the channel, functioning efficiently at gigabit per second speeds. The I/O often features high swing unterminated logic (HUSL), with a non-linear transmitter design, and some incorporate low-voltage swing termination logic (LVSTL) to conserve power by reducing signal amplitude.

While these interfaces usually operate at lower data rates compared to the latest link technologies, they present distinct challenges that demand specialized methods for a precise and effective evaluation of voltage and timing budgets. An exhaustive transistor-level examination of both the transmitter and receiver front ends, as well as the channel itself, is essential for accurately identifying voltage noise and timing jitter within the interface.

The system’s I/O physical layer (PHY) is strategically segmented into "Analog" and "Digital" parts, with each section requiring tailored approaches to accurately ascertain their voltage and timing budgets. The "Analog" section utilizes transistor-level circuit simulations like SPICE to scrutinize intersymbol interference (ISI), crosstalk, and fluctuations in power supply within the partition. This part of the analysis also considers the nonlinearity and bandwidth constraints of the transmitter and receiver front ends. Eye diagrams at the transmitter, receiver pads, and latch provide a clear visualization of voltage noise and timing jitter, highlighting the integrity of the "Analog" portion of the link [2].

The analysis then shifts as the signal moves to CMOS levels in the "Digital" section, where timing jitter emerges as a pivotal concern. This part of the study details a specific method for quantifying the jitter induced within the digital pathway, ensuring a thorough investigation that encompasses both the analog and digital facets of the die-to-die interface’s performance.

RELATED WORK

MODEL 1

SPICE Simulations and Jitter Analysis in I/O Circuit Dynamics

In the section detailing circuit blocks and SPICE simulations, a comprehensive analysis of the physical (PHY) layer's clock and data paths within

I/O circuits is meticulously described. The use of transistor-level circuit simulations, which utilize the post layout design of the PHY circuits chip, provides a robust foundation for verifying the empirical Power Supply Induced Jitter (PSIJ) analysis methodology. This detailed description begins with the generation of the clock signal from a phase-locked loop (PLL) and follows its progression through various crucial components such as calibration circuits, a clock tree, and a phase interpolator. This thorough clock management is essential for the synchronized distribution and phase alignment of the clock signal, which facilitates the generation and reshaping of data and strobe signals within the I/O register blocks.

In the discussion of the SPICE simulation setup, the narrative focuses on the extraction of the full path circuit blocks from PLL to output buffers into a SPICE post layout netlist. This setup is vital for conducting transient simulations to measure the delay and dc sensitivity required in the Jitter Transfer Function (JTF) equations. By detailing the simulation process, where delay values of each block are measured under different voltages, the text effectively outlines how empirical analysis is grounded in practical, simulated scenarios. The simulation further investigates the impact of sinusoidal noise applied to power nodes with frequency sweeps, assessing its influence on the clock's phase jitter and the opening of the data eye at the output buffer. These simulations are critical for evaluating the PSIJ impacts, thereby enhancing the reliability and performance of the PHY circuit designs in real-world applications.

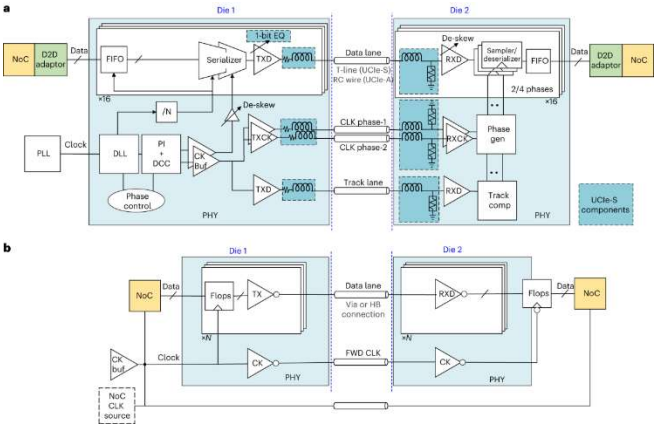

Figure 5 The image displays a schematic of die-to-die communication, highlighting data transfer and clock synchronization between two semiconductor dies, with detailed views of serialization, phase control, and physical layer interactions.

The SPICE simulation results section effectively highlights several critical elements of circuit performance under different scenarios. Initially, it is discussed how varying supply voltages influence the delays across key circuit components like predrivers, I/O registers, phase interpolators, calibration circuits, and the clock tree. Notably, as supply voltage increases, a decrease in delay is observed, a common phenomenon in digital circuits attributed to faster carrier mobility at higher voltages. Additionally, the DC sensitivity, represented as $H0$, is quantitatively assessed, showing how delay susceptibility to DC voltage changes is calculated.

The study also delves into the relationship between clock phase jitter (PJ) and empirical Power Supply Induced Jitter (PSIJ) findings. Variations in VCCA or VCC noise frequency impact the jitter measurements at the output buffer, which correspond closely with theoretical values derived from the Jitter Transfer Function (JTF). Despite an overall alignment, some variability due to nonlinear delay sensitivity and computational inaccuracies in the SPICE simulations affecting the eye diagram measurements is noted.

Furthermore, the correlation of open-path jitter examines the consistency between empirical analyses and SPICE simulations in the context of data signal jitter caused by noise in VCCA or VCC. The JTF, characterized by a sinc function, indicates that the simulated and empirical jitter characteristics over frequency are closely matched.

This underscores a solid approach to understanding and designing for the influence of noise on data transmission reliability.

In the final analysis, the exploration of data jitter within source-synchronous clocking systems discusses the intricate balance required to maintain synchronized data and clock jitter amidst low-frequency noise. Notable discrepancies in jitter magnitude and the emergence of null points at lower frequencies are observed, attributed to overlooked interactions among supply domains and complex supply rail distributions among circuit blocks. These findings spotlight the intricacies and challenges in simulating complex circuit behaviors effectively, especially in environments where multiple supply domains are interconnected.

Together, these insights deepen the comprehension of how electrical conditions affect circuit functionality, stressing the importance of accurate modeling and comprehensive simulation practices to uphold circuit integrity and operational efficiency.

MODEL 2

The section on Timing Uncertainty/Jitter Modeling comprehensively addresses the factors contributing to jitter as data is transmitted from transmitter to receiver through a 10-link channel. It outlines how jitter, or timing uncertainty, is induced by various noise sources, including those inherent to clock elements like the Phase-Locked Loop (PLL), power noise, and the physical extent of the on-die clock tree.

Power-induced jitter is particularly emphasized as being significant along the on-die clock path, extending through the pre-driver and driver stages. This kind of jitter accumulates incrementally at each stage, exacerbated by power noise impacting the clock buffer's output at every step. As this output jitter accumulates from one stage to the next, it can significantly affect the overall system's timing integrity.

The text explains that the jitter transfer function related to power noise is inversely proportional to the signal gain (Gmn) and exhibits a low-pass filter characteristic against noise frequency. This means that the clock buffer's ability to respond to high-frequency noise is limited, effectively acting as a low-pass filter. Understanding the specific frequencies at which noise impacts jitter (known as the knee frequency) is crucial for managing system noise. Below this knee frequency, the jitter remains relatively constant; above it, the buffer's response lags.

The analysis further discusses how the delay characteristics of the clock buffer influence jitter transfer, with longer delay buffers showing higher jitter transfer than shorter ones. Factors such as the amplitude of noise tones, impacted by the integrity of the power delivery network (PDN), and the physical length of the on-die clock tree, play integral roles in the system's overall jitter characteristics.

Additionally, a Source Synchronous Architecture introduces another layer of complexity, providing a high-pass jitter to noise transfer characteristic. This peaking transfer function is highly influenced by the skew between the data path and the source-synchronous clock/strobe path, which forms another critical factor in system timing uncertainty.

In terms of system criteria, the receiver end mimics the jitter-induced and accumulated path similar to the transmitter layer in a source synchronous architecture. The jitter at the receiver is referenced to the strobe, and the receiver's sensitivity is defined by an "eye mask," which dictates whether the system passes or fails based on specified criteria. When considering channel effects, the passage also details how signal jitter can be modulated by channel losses and dispersion. A linear, passive, and noiseless lossy channel typically amplifies the jitter, particularly because of the differential attenuation between the jitter's lower sideband and the signal carrier. This effect, which grows exponentially with jitter frequency and data rate, illustrates the intricate interplay between channel design and jitter behaviour.

Comparing two channel designs— one implemented in a passive silicon interposer and another using Integrated Fan-Out (InFO) media— highlights how differences in channel stack-up and

design geometry affect jitter amplification. Each design shows distinct characteristics in jitter amplification versus noise frequency, underscoring the importance of careful design consideration to manage and minimize jitter in high-frequency transmission environments.

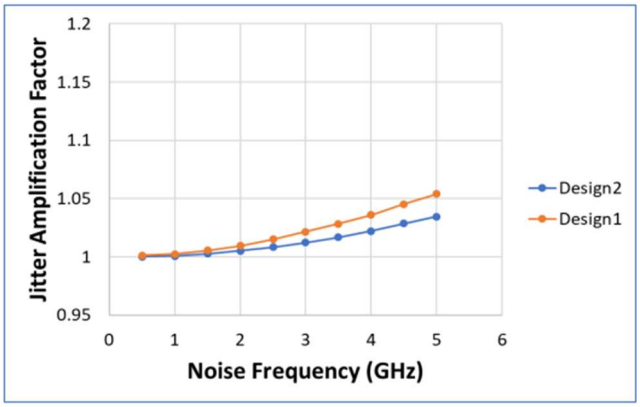

Figure 6 Jitter Amplification Comparison for Analysis

Section 3.2 delves into the combined system jitter model, which facilitates a top-down analysis of the trade-offs between various design input factors, as illustrated in a figure and detailed in an accompanying table. This unified jitter model generates output response samples, which are then utilized to develop a response surface. This surface effectively correlates the input factors, enabling an understanding of how each factor's gradient sensitivity affects the system's output jitter, specifically the Receiver Side Effective Jitter.

The input variables listed in the table are selected based on prior experience and understanding of circuit block behaviors. They primarily include power supply noise amplitudes across multiple frequency tones, which are harmonics of the switching frequencies of the driver and adjacent logic blocks. The model considers two main power supplies: one for the Tx clock buffer and another combined supply for the driver and receiver blocks. Variables x1 to x5 represent the Tx clock buffer power noise at various frequencies, while x6 to x10 pertain to the Driver and Receiver block power noise amplitudes at different frequencies. Additional variables include the channel jitter amplification factor and buffer delays for various components such as the Tx on-die clock, Tx driver, and receiver DQS and DQ.

The model allows for exploration of different combinations of these design factors to see how perturbations affect system timing uncertainty or jitter. Outputs from simulation runs, as depicted in another figure, quantify the differences in system timing uncertainty or jitter, which are further analysed to refine the design process. This systematic approach enables precise adjustments in the design to optimize performance and reduce effective jitter at the receiver side.

The use of Response Surface Methodology (RSM) to profile key input factors and understand their sensitivity in optimizing electrical design. RSM, which generates a polynomial regression model, allows designers to statistically explore the design space. By varying input variables as outlined in a previous table, an RSM-based Design of Experiment (DoE) matrix is created. This matrix, adjusting the power supply noise tone amplitudes by 0 to 20% and buffer delays by ±30%, is used to simulate and capture the output jitter responses for model fitting.

The analysis identifies that the variables x1, x2, and the interaction between x3 and x8 are most significant in predicting output jitter. Variables x1 and x2 relate to the noise amplitudes at different frequency tones of the Tx clock buffer power supply, while x3 and x8 pertain to the noise amplitude on the Tx clock buffer and the Driver & RCV power supply, respectively.

The study highlights that the channel design is not a significant limiting factor in this setup, with its influence on jitter being substantially less than that of supply noise amplitude. This indicates that power supply noise is a more critical factor to manage in this design.

Additionally, a prediction profiler is used to visually adjust input variables based on their relationship with output jitter as determined by the fitted model. This tool helps designers fine-tune the design to achieve desired jitter outcomes. A surface plot further visualizes the dependency of output jitter on the input variables x1 and x2, showcasing how variations in these variables significantly impact the system’s jitter. This visual aid is

instrumental in facilitating targeted adjustments in the design process for optimized performance.

Figure 7 Design Factor Influence

In an empirical case study, system sensitivity was analyzed by changing the channel media from an interposer to an Integrated Fan-Out (InFO) channel. Analysis indicated that the impact of this change was significantly less than that of the top design factors, suggesting comparable overall performance when other factors are held constant. Comparative tests showed that eye margins varied within 1% of the unit interval (UI) at the reference voltage (Vref), indicating that channel media change does not negatively impact performance, aligning with initial predictions.

The integration of a Chiplets System over traditional monolithic SoC approaches offers benefits such as modular design and potential cost savings but also introduces challenges in optimizing key design factors. A unified system timing uncertainty/jitter model, validated against experimental data, supports the generation of training samples for response surface modeling to quantify sensitivity and effects of design factors. This approach facilitates a comprehensive assessment of design trade-offs and impacts, enhancing design collaboration and optimizing system performance, especially when using Chiplets sourced from different vendors.

COMPARITVE ANALYSIS

When analysing the relevance of these models to high-speed data transmission between chiplets, both Model 1 (**SPICE Simulations and Jitter Analysis in I/O Circuit Dynamics**) and Model 2 (**Timing Uncertainty/Jitter Modeling**) offer crucial insights and methodologies that are directly applicable to enhancing the performance and reliability of chiplet-based systems.

Model 1, with its detailed SPICE simulations, is particularly relevant to high-speed data transmission as it provides a granular look at how the physical layer (PHY) and its components, such as PLLs, output buffers, and serializers, handle high-frequency signals. This model's focus on the effects of Power Supply Induced Jitter (PSIJ) and signal integrity under various electrical conditions is critical for designing chiplets that must operate reliably at high data rates. The precision in measuring and optimizing the phase jitter and data integrity ensures that the signal quality is maintained across the interfaces between chiplets, which is a cornerstone for achieving efficient high-speed data transmission.

Model 2 expands the scope to system-level interactions and emphasizes the accumulation of jitter as data travels through interconnected chiplets. This model's broader approach, which assesses how jitter is influenced by multiple factors including power noise, clock tree design, and the physical layout of on-die pathways, is essential for understanding and mitigating the composite effects that can degrade signal quality in chiplet architectures. The use of jitter transfer functions and the response surface methodology (RSM) help in identifying and optimizing critical factors that impact the overall timing integrity of the system, which is vital for ensuring that high-speed data can be transmitted reliably between chiplets.

The strategic integration of these models provides a comprehensive framework for addressing both detailed component behavior and broader system dynamics in chiplet-based designs. By combining the rigorous circuit-specific analysis of Model 1 with the systemic overview provided by Model 2, designers can optimize each aspect of the chiplet interface—from electrical and timing specifications to architectural layout and noise management—to enhance the efficiency and reliability of high-speed data transmission. This dual approach is especially important in the context of modern SoCs where chiplets, often manufactured at different process nodes and featuring diverse functionalities, need to communicate effectively at high speeds without data integrity loss or performance bottlenecks.

DISCUSSION

Interpretation of Results

The research into high-speed data transmission in chiplet-based systems has unearthed key insights into how these systems function. The detailed examination of the physical layer components, such as oscillators, buffers, and interconnects, along with a broader look at system interactions, provides a comprehensive understanding of how various design elements influence overall performance.

The thorough study of these components, particularly in their handling of high-frequency signals, directly addresses the main research question: How can chiplet-based systems ensure signal integrity and reduce jitter during high-speed operations? The results verify that meticulous management of these components is vital for reducing sources of jitter and enhancing signal integrity, which is crucial for the consistent performance of each chiplet at high transmission speeds. This focused attention on component-level details helps maintain the quality of signal transmission throughout the chip's complex interfaces, effectively resolving the posed research question.

Additionally, when these findings are compared with existing studies, it's clear that while the principles of signal integrity and jitter reduction are established within semiconductor design, their application to chiplet-based systems presents unique challenges and innovative solutions. The application of sophisticated analytical methods like response surface methodology for optimizing design parameters underscores a forward-thinking strategy to handle the intricacies brought on by the interconnected nature of chiplet systems. These insights broaden existing knowledge by illustrating how strategic system-level design can proactively prevent signal degradation across connected chiplets.

Limitations

Despite the depth of analysis and valuable insights derived, this study is not without limitations and potential biases:

Model Dependency: The reliance on theoretical models and simulation tools such as SPICE and response surface methodology could impact the accuracy of the findings. These tools are dependable, but the validity of the results depends on the assumptions and parameters of the models used. Inaccuracies in these models can cause a divergence between simulated outcomes and actual performance.

Generalizability: The study's focus on high-speed data transmission within particular chiplet-based systems limits its generalizability. The specific conclusions drawn concerning power supply variations, clock distribution methods, and physical routing might not be applicable to systems with differing design requirements or in different operational settings.

Experimental Validation: Predominantly theoretical and simulation-based, the study lacks empirical validation through physical experiments. Actual testing could uncover other factors influencing system performance that simulations alone cannot replicate.

Complexity of Interconnects: The varying complexities and types of interconnect technologies used in chiplet designs may pose additional challenges not fully considered in this study. Factors like material choice, manufacturing processes, and environmental conditions can affect the results, indicating a need for more comprehensive studies to understand these effects fully.

Recognizing these limitations ensures a balanced perspective on the study's contributions and paves the way for subsequent research. Future studies could aim to overcome these limitations by including empirical testing, expanding the scope of designs and technologies explored, and refining models based on tangible data.

CONCLUSIONS

Effectively tackling the complexities of high-speed data transmission in chiplet-based systems necessitates a layered approach that meticulously combines detailed analysis of individual components with a broad evaluation of the entire system. This strategy ensures that each element not only contributes positively to overall performance and reliability but also complements the system as a whole.

At the component level, the focus is on the detailed examination of the physical layer, scrutinizing how elements like oscillators, buffers, and interconnects manage high-frequency signals. The aim here is to minimize jitter sources and boost signal integrity across various electrical conditions. Such detailed attention is vital for ensuring that every chiplet performs reliably at high data rates, crucial for preserving signal quality across the sophisticated interfaces of the chip.

On a broader scale, it's essential to consider the cumulative impact of design choices on the entire system architecture. This involves analyzing the effects of fluctuations in power supply, strategies for clock distribution, and the layout of physical routing on the timing and quality of signals moving through interconnected chiplets. Grasping these dynamics is key to reducing signal deterioration that can accumulate across the system, thus safeguarding data integrity even at peak transmission speeds.

Additionally, leveraging sophisticated analytical methods like response surface methodology is instrumental in identifying key factors that affect system performance. This enables precise adjustments to design parameters, optimizing outcomes. This comprehensive perspective not only helps spot potential issues but also aids in addressing them proactively, avoiding expensive redesigns and promoting a more efficient development cycle.

In summary, the intricate challenges of high-speed data transmission within chiplet-based systems require an advanced, integrated strategy that merges in-depth technical scrutiny with strategic oversight of system-level interactions. By maintaining rigorous detail at the component level while overseeing the system's overall interactions, designers can fully exploit the advantages of chiplet technology. This method not only enhances performance and scalability but also advances the limits of what can be achieved in contemporary semiconductor design, fostering innovations that meet the growing complexity and functional demands of today and tomorrow. Such thorough and detailed efforts enable the semiconductor industry to progress, fulfilling the stringent needs of high-speed digital communication while staying resilient amidst continually changing technological challenges.

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