

Assignment-2 Report

EE 705: VLSI Design Lab

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1 Question 1: Dadda Multiplier

1.1 Simulation results

16x16 multiplier was implemented with 6 stages of depth - 2,3,4,6,9,13 . ($d_{k+1} = 1.5d_k$) . In the last stage 32 bit brent kung adder was used from the previous results . Successful simulation results are obtained as shown in 1 .

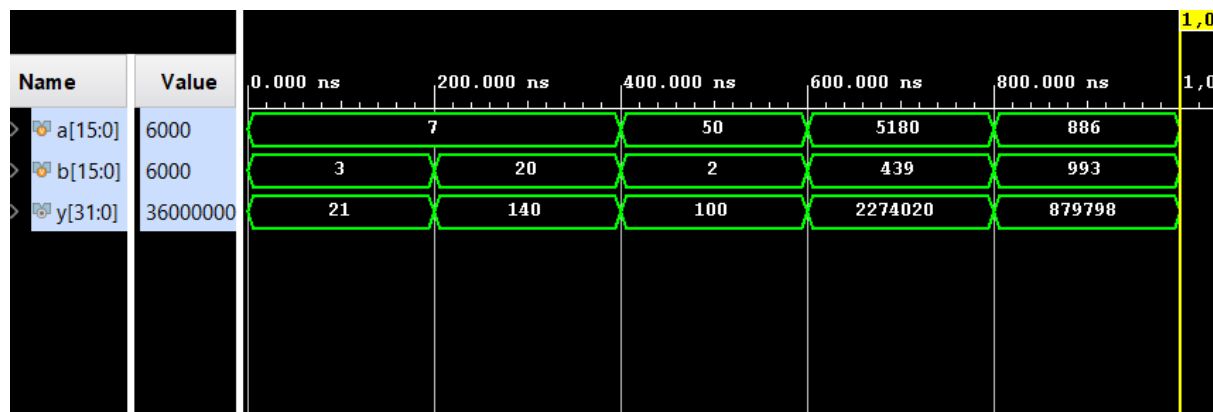


Figure 1: Simulation waveforms (Dadda multiplier)

1.2 Resource utilization (dadda multiplier)

1. Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	314	0	53200	0.59
LUT as Logic	314	0	53200	0.59
LUT as Memory	0	0	17400	0.00
Slice Registers	0	0	106400	0.00
Register as Flip Flop	0	0	106400	0.00
Register as Latch	0	0	106400	0.00
F7 Muxes	0	0	26600	0.00
F8 Muxes	0	0	13300	0.00

* Warning! The Final LUT count, after physical optimizations and full implementation,

1.1 Summary of Registers by Type

Total	Clock Enable	Synchronous	Asynchronous
0	-	-	-

0		-		-		Set	
0		-		-		Reset	
0		-		Set		-	
0		-		Reset		-	
0		Yes		-		-	
0		Yes		-		Set	
0		Yes		-		Reset	
0		Yes		Set		-	
0		Yes		Reset		-	
+-----+							

2. Memory

+-----+					
Site Type	Used	Fixed	Available	Util%	
+-----+					
Block RAM Tile	0	0	140	0.00	
RAMB36/FIFO*	0	0	140	0.00	
RAMB18	0	0	280	0.00	
+-----+					

* Note: Each Block RAM Tile only has one FIFO logic available and therefore can accom

3. DSP

Site Type		Used		Fixed		Available		Util%	
DSPs		0		0		220		0.00	

4. IO and GT Specific

+-----+-----+-----+-----+				
Site Type	Used	Fixed	Available	Util%
+-----+-----+-----+-----+				
Bonded IOB	64	0	125	51.20
Bonded IPADs	0	0	2	0.00
Bonded IOPADs	0	0	130	0.00
PHY_CONTROL	0	0	4	0.00
PHASER_REF	0	0	4	0.00
OUT_FIFO	0	0	16	0.00
IN_FIFO	0	0	16	0.00

IDELAYCTRL		0		0		4		0.00	
IBUFDS		0		0		121		0.00	
PHASER_OUT/PHASER_OUT_PHY		0		0		16		0.00	
PHASER_IN/PHASER_IN_PHY		0		0		16		0.00	
IDELAYE2/IDELAYE2_FINEDELAY		0		0		200		0.00	
ILOGIC		0		0		125		0.00	
OLOGIC		0		0		125		0.00	
+-----+-----+-----+-----+-----+									

5. Clocking

+-----+-----+-----+-----+-----+					
Site Type	Used	Fixed	Available	Util%	
+-----+-----+-----+-----+-----+					
BUFGCTRL	0	0	32	0.00	
BUFIO	0	0	16	0.00	
MMCME2_ADV	0	0	4	0.00	
PLLE2_ADV	0	0	4	0.00	
BUFMRCE	0	0	8	0.00	
BUFHCE	0	0	72	0.00	
BUFR	0	0	16	0.00	
+-----+-----+-----+-----+-----+					

6. Specific Feature

+-----+-----+-----+-----+-----+					
Site Type	Used	Fixed	Available	Util%	
+-----+-----+-----+-----+-----+					
BSCANE2	0	0	4	0.00	
CAPTUREE2	0	0	1	0.00	
DNA_PORT	0	0	1	0.00	
EFUSE_USR	0	0	1	0.00	
FRAME_ECCE2	0	0	1	0.00	
ICAPE2	0	0	2	0.00	
STARTUPE2	0	0	1	0.00	
XADC	0	0	1	0.00	
+-----+-----+-----+-----+-----+					

7. Primitives

+-----+-----+-----+-----+					
Ref Name		Used		Functional Category	

LUT6	199	LUT
LUT5	68	LUT
LUT3	63	LUT
LUT4	39	LUT
OBUF	32	IO
IBUF	32	IO
CARRY4	8	CarryLogic
LUT2	7	LUT

1.3 Using * Operator

1.4 Simulation results (* operator)

Same results were obtained as dadda multiplier .

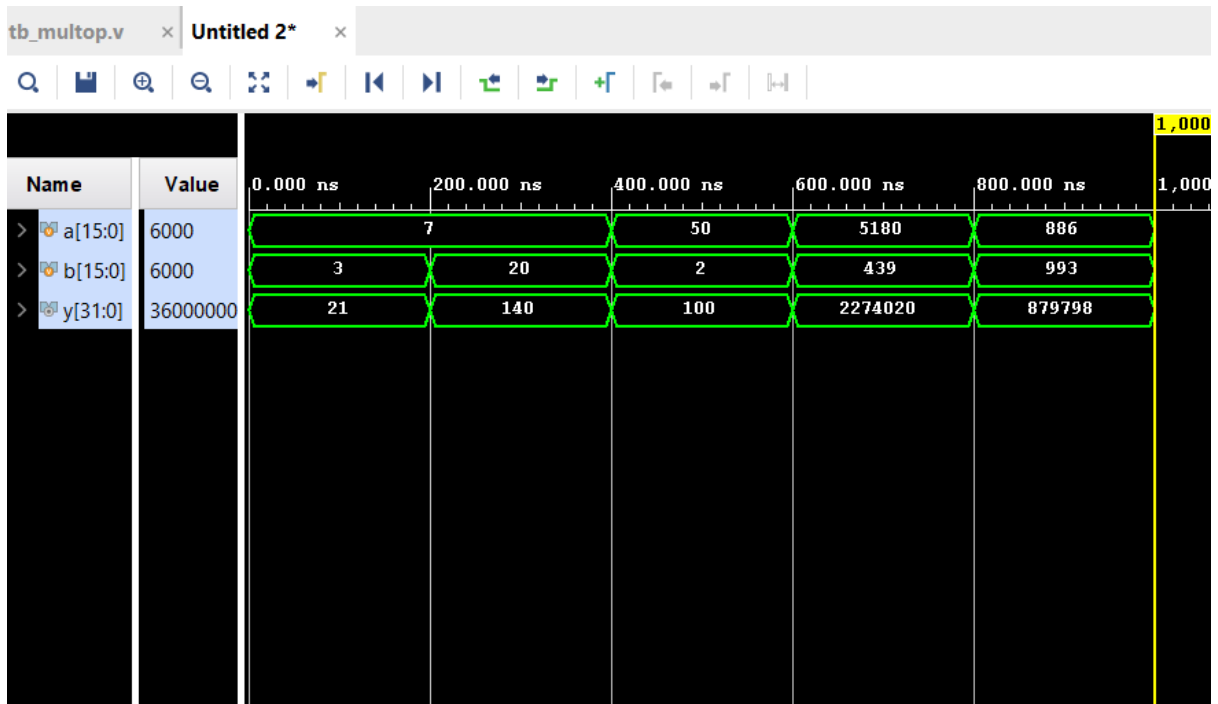


Figure 2: Simulation waveforms (multiplier operator)

1.5 Resource utitlization(* operator)

1. Slice Logic

Site Type	Used	Fixed	Available	Util%
Slice LUTs*	0	0	53200	0.00
LUT as Logic	0	0	53200	0.00
LUT as Memory	0	0	17400	0.00

Slice Registers	0	0	106400	0.00	
Register as Flip Flop	0	0	106400	0.00	
Register as Latch	0	0	106400	0.00	
F7 Muxes	0	0	26600	0.00	
F8 Muxes	0	0	13300	0.00	

+-----+-----+-----+-----+-----+

* Warning! The Final LUT count, after physical optimizations and full implementation,

1.1 Summary of Registers by Type

+-----+	+-----+	+-----+	+-----+	+-----+
Total	Clock Enable	Synchronous	Asynchronous	
+-----+	+-----+	+-----+	+-----+	+-----+
0	-	-	-	
0	-	-	Set	
0	-	-	Reset	
0	-	Set	-	
0	-	Reset	-	
0	Yes	-	-	
0	Yes	-	Set	
0	Yes	-	Reset	
0	Yes	Set	-	
0	Yes	Reset	-	
+-----+	+-----+	+-----+	+-----+	+-----+

2. Memory

+-----+	+-----+	+-----+	+-----+	+-----+
Site Type	Used	Fixed	Available	Util%
+-----+	+-----+	+-----+	+-----+	+-----+
Block RAM Tile	0	0	140	0.00
RAMB36/FIFO*	0	0	140	0.00
RAMB18	0	0	280	0.00
+-----+	+-----+	+-----+	+-----+	+-----+

* Note: Each Block RAM Tile only has one FIFO logic available and therefore can accom

3. DSP

+-----+	+-----+	+-----+	+-----+	+-----+
Site Type	Used	Fixed	Available	Util%
+-----+	+-----+	+-----+	+-----+	+-----+
DSPs	1	0	220	0.45

DSP48E1 only	1			
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4. IO and GT Specific

Site Type	Used	Fixed	Available	Util%
Bonded IOB	64	0	125	51.20
Bonded IPADs	0	0	2	0.00
Bonded IOPADs	0	0	130	0.00
PHY_CONTROL	0	0	4	0.00
PHASER_REF	0	0	4	0.00
OUT_FIFO	0	0	16	0.00
IN_FIFO	0	0	16	0.00
IDELAYCTRL	0	0	4	0.00
IBUFDS	0	0	121	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	16	0.00
PHASER_IN/PHASER_IN_PHY	0	0	16	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	200	0.00
ILOGIC	0	0	125	0.00
OLOGIC	0	0	125	0.00

5. Clocking

Site Type	Used	Fixed	Available	Util%
BUFGCTRL	0	0	32	0.00
BUFIO	0	0	16	0.00
MMCME2_ADV	0	0	4	0.00
PLLE2_ADV	0	0	4	0.00
BUFMRCE	0	0	8	0.00
BUFHCE	0	0	72	0.00
BUFR	0	0	16	0.00

6. Specific Feature

Site Type	Used	Fixed	Available	Util%
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BSCANE2	0	0	4	0.00	
CAPTUREE2	0	0	1	0.00	
DNA_PORT	0	0	1	0.00	
EFUSE_USR	0	0	1	0.00	
FRAME_ECCE2	0	0	1	0.00	
ICAPE2	0	0	2	0.00	
STARTUPE2	0	0	1	0.00	
XADC	0	0	1	0.00	

7. Primitives

Ref Name	Used	Functional Category	
OBUF	32	IO	
IBUF	32	IO	
DSP48E1	1	Block Arithmetic	

1.6 Controller and bitstream generation

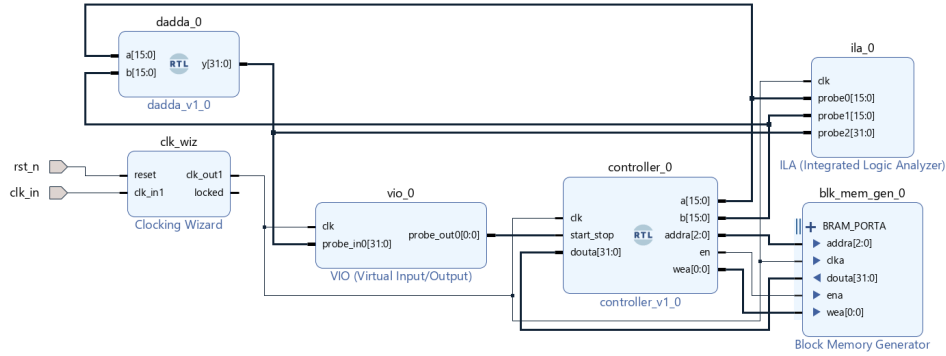


Figure 3: Block design

A .coe file was used to initialize the BRAM with the test vectors provided . The controller begins its execution when start_stop signal is set to 1 . It traverses over all memory locations by incrementing an internal counter of 3 bit(for 5 memory locations) to increment addra . The counter resets to 0 after it crosses all the locations . The data in BRAM consists of 32 bits where first 16 bits comprise of a and next 16 bits of b . It extracts the first 16 bits for a and next 16 bits for b . It has two additional output signals : en (always set to 1 for read enabled for BRAM) and wea (always set to 0 to disable write in BRAM) . The design wrapper was created from the figure shown in 3 . ILA (Integrated Logic Analyzer) and VIO (Virtual Input/Output) are debugging tools in Xilinx Vivado used for FPGA designs. ILA is an in-chip logic debugging tool that allows users to capture

and analyze internal FPGA signals in real-time. It is commonly used to verify signal behavior and debug designs without external probes. VIO provides interactive control and monitoring of FPGA signals, enabling users to dynamically drive inputs and observe outputs during runtime. It is particularly useful for prototyping and testing designs. Block design was generated using ILA and VIO and bitstream file was generated .

The simulation results on the development board obtained correctly matched the computations.

2 Question 2: Log shifter

2.1 Simulation results(barrel shifter)

Left-right shifter was implemented using combinational logic . To control the direction of shift - lr bit was used when set to 1 shifts to right by given amount else shift by 0 . If lr set to 0 bit reversal done at input and output .

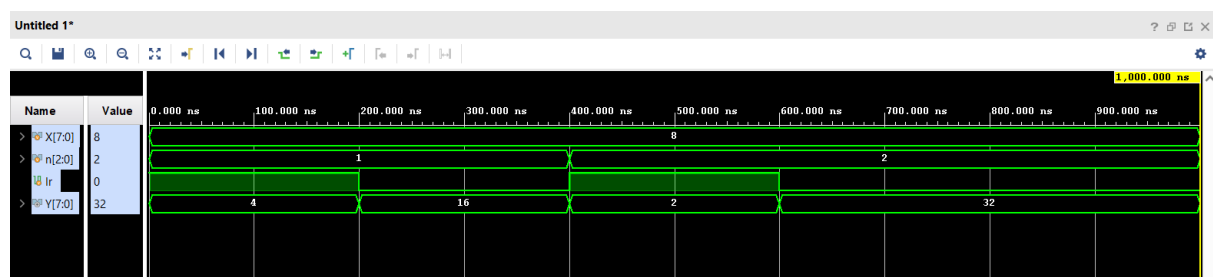


Figure 4: Barrel shifter results

2.2 Resource utilization(barrel shifter)

1.1 Summary of Registers by Type

Total	Clock Enable	Synchronous	Asynchronous
0	-	-	-
0	-	-	Set
0	-	-	Reset
0	-	Set	-
0	-	Reset	-
0	Yes	-	-
0	Yes	-	Set
0	Yes	-	Reset
0	Yes	Set	-
0	Yes	Reset	-

2. Memory

Site Type	Used	Fixed	Available	Util%
Block RAM Tile	0	0	140	0.00
RAMB36/FIFO*	0	0	140	0.00
RAMB18	0	0	280	0.00

* Note: Each Block RAM Tile only has one FIFO logic available and therefore can accom

3. DSP

Site Type	Used	Fixed	Available	Util%
DSPs	0	0	220	0.00

4. IO and GT Specific

Site Type	Used	Fixed	Available	Util%
Bonded IOB	20	0	125	16.00
Bonded IPADs	0	0	2	0.00
Bonded IOPADs	0	0	130	0.00
PHY_CONTROL	0	0	4	0.00
PHASER_REF	0	0	4	0.00
OUT_FIFO	0	0	16	0.00
IN_FIFO	0	0	16	0.00
IDELAYCTRL	0	0	4	0.00
IBUFDS	0	0	121	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	16	0.00
PHASER_IN/PHASER_IN_PHY	0	0	16	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	200	0.00
ILOGIC	0	0	125	0.00
OLOGIC	0	0	125	0.00

5. Clocking

Site Type	Used	Fixed	Available	Util%
BUFGCTRL	0	0	32	0.00
BUFIO	0	0	16	0.00
MMCME2_ADV	0	0	4	0.00
PLLE2_ADV	0	0	4	0.00
BUFMRCE	0	0	8	0.00
BUFHCE	0	0	72	0.00
BUFR	0	0	16	0.00

6. Specific Feature

Site Type	Used	Fixed	Available	Util%
BSCANE2	0	0	4	0.00
CAPTUREE2	0	0	1	0.00
DNA_PORT	0	0	1	0.00
EFUSE_USR	0	0	1	0.00
FRAME_ECCE2	0	0	1	0.00
ICAPE2	0	0	2	0.00
STARTUPE2	0	0	1	0.00
XADC	0	0	1	0.00

7. Primitives

Ref Name	Used	Functional Category
LUT5	12	LUT
IBUF	12	IO
OBUF	8	IO
LUT6	8	LUT
LUT4	4	LUT
LUT3	2	LUT

2.3 Using shift operator

Similar analysis was done using operator .

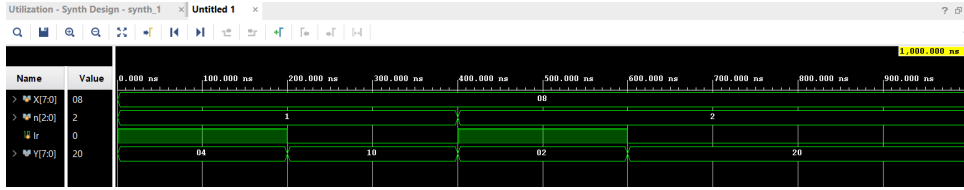


Figure 5: Simulation results (shift operation)

2.4 Resource utilization (shift operator)

1.1 Summary of Registers by Type

Total	Clock Enable	Synchronous	Asynchronous
0	-	-	-
0	-	-	Set
0	-	-	Reset
0	-	Set	-
0	-	Reset	-
0	Yes	-	-
0	Yes	-	Set
0	Yes	-	Reset
0	Yes	Set	-
0	Yes	Reset	-

2. Memory

Site Type	Used	Fixed	Available	Util%
Block RAM Tile	0	0	140	0.00
RAMB36/FIFO*	0	0	140	0.00
RAMB18	0	0	280	0.00

* Note: Each Block RAM Tile only has one FIFO logic available and therefore can accom

3. DSP

Site Type	Used	Fixed	Available	Util%
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DSPs	0	0	220	0.00	
+-----+-----+-----+-----+-----+					

4. IO and GT Specific

Site Type	Used	Fixed	Available	Util%
Bonded IOB	20	0	125	16.00
Bonded IPADs	0	0	2	0.00
Bonded IOPADs	0	0	130	0.00
PHY_CONTROL	0	0	4	0.00
PHASER_REF	0	0	4	0.00
OUT_FIFO	0	0	16	0.00
IN_FIFO	0	0	16	0.00
IDELAYCTRL	0	0	4	0.00
IBUFDS	0	0	121	0.00
PHASER_OUT/PHASER_OUT_PHY	0	0	16	0.00
PHASER_IN/PHASER_IN_PHY	0	0	16	0.00
IDELAYE2/IDELAYE2_FINEDELAY	0	0	200	0.00
ILOGIC	0	0	125	0.00
OLOGIC	0	0	125	0.00

5. Clocking

Site Type	Used	Fixed	Available	Util%
BUFGCTRL	0	0	32	0.00
BUFIO	0	0	16	0.00
MMCME2_ADV	0	0	4	0.00
PLLE2_ADV	0	0	4	0.00
BUFMRCE	0	0	8	0.00
BUFHCE	0	0	72	0.00
BUFR	0	0	16	0.00

6. Specific Feature

Site Type	Used	Fixed	Available	Util%
-----------	------	-------	-----------	-------

BSCANE2	0	0	4	0.00	
CAPTUREE2	0	0	1	0.00	
DNA_PORT	0	0	1	0.00	
EFUSE_USR	0	0	1	0.00	
FRAME_ECCE2	0	0	1	0.00	
ICAPE2	0	0	2	0.00	
STARTUPE2	0	0	1	0.00	
XADC	0	0	1	0.00	

7. Primitives

Ref Name	Used	Functional Category	
IBUF	12	IO	
LUT6	10	LUT	
OBUF	8	IO	
LUT5	6	LUT	
LUT4	4	LUT	
LUT3	4	LUT	

2.5 Controller and bitstream generation

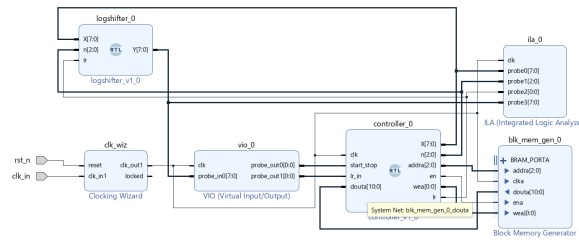


Figure 6: Block design

A .coe file was used to initialize the BRAM with the test vectors provided . The controller begins its execution when start_stop signal is set to 1 . It traverses over all memory locations by incrementing an internal counter of 3 bit(for 8 memory locations) to increment addra . The counter resets to 0 after it crosses all the locations . The data in BRAM consists of 11 bits where first 8 bits comprise of input X and last 3 bits of n (shift amount) . It extracts the first 8 bits for a and next 3 bits for n . It has two additional output signals : en (always set to 1 for read enabled for BRAM) and wea (always set to 0 to disable write in BRAM) . The design wrapper was created from the figure shown in 6 . ILA (Integrated Logic Analyzer) and VIO (Virtual Input/Output) are debugging tools

in Xilinx Vivado used for FPGA designs. ILA is an in-chip logic debugging tool that allows users to capture and analyze internal FPGA signals in real-time. It is commonly used to verify signal behavior and debug designs without external probes. VIO provides interactive control and monitoring of FPGA signals, enabling users to dynamically drive inputs and observe outputs during runtime. It is particularly useful for prototyping and testing designs. Block design was generated using ILA and VIO and bitstream file was generated .