Assignment-3 Report
EE 705: VLSI Design Lab

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Contents

1 Question 1

1.1 Block design

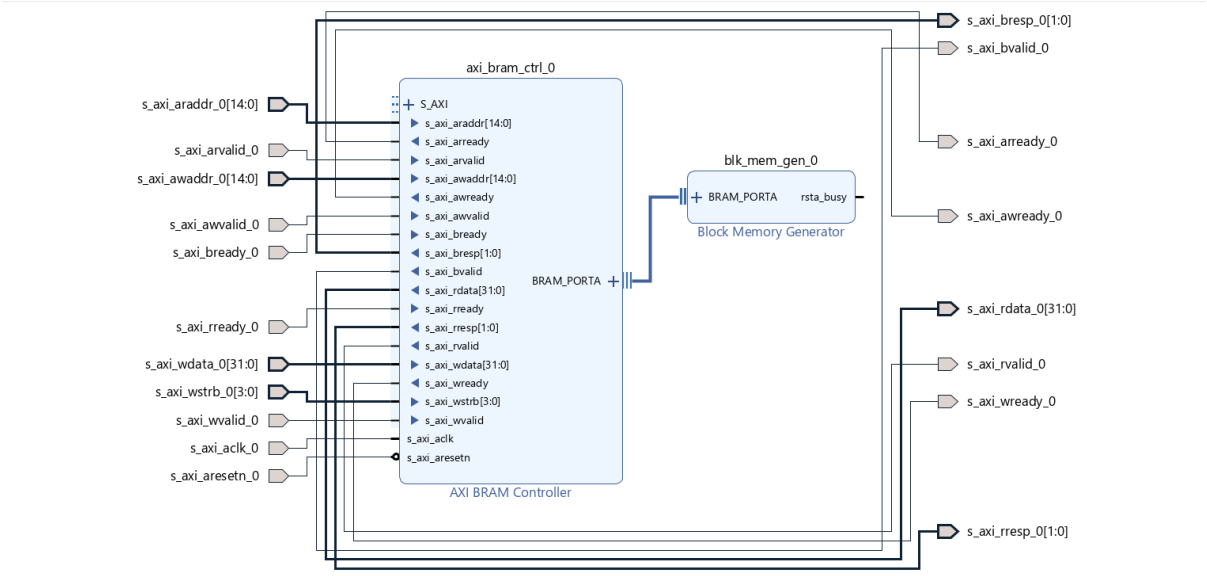

Figure 1: Block design Q1

1.2 Simulation results

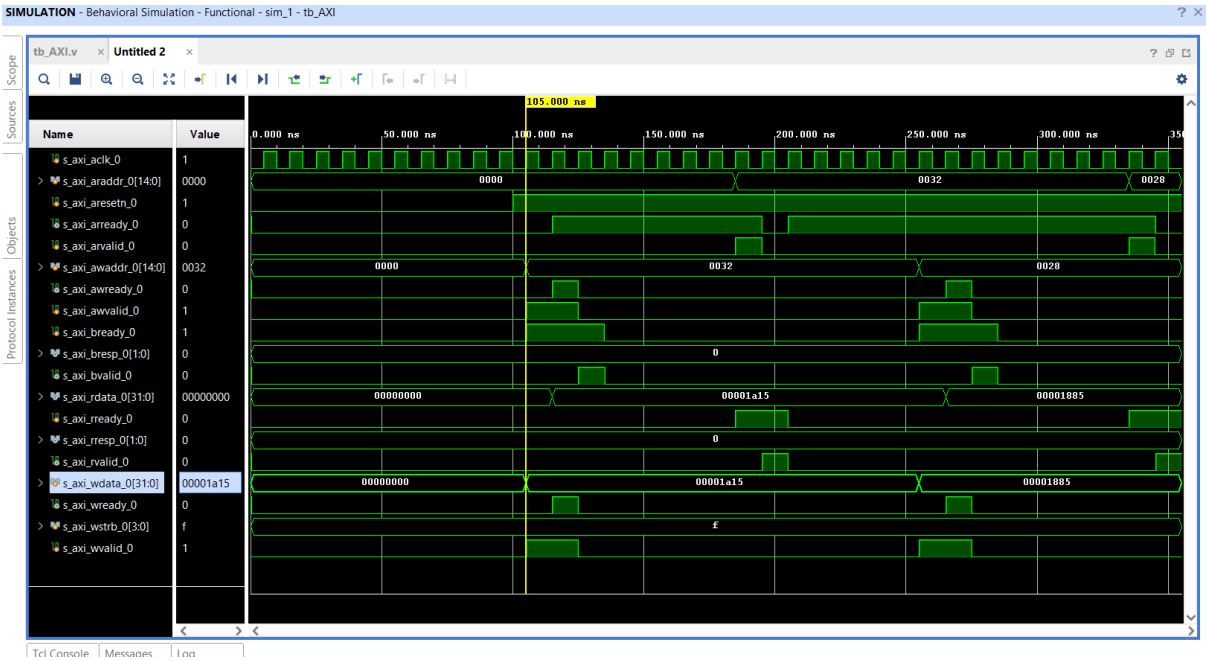

Figure 2: Read and write

2 Question 2

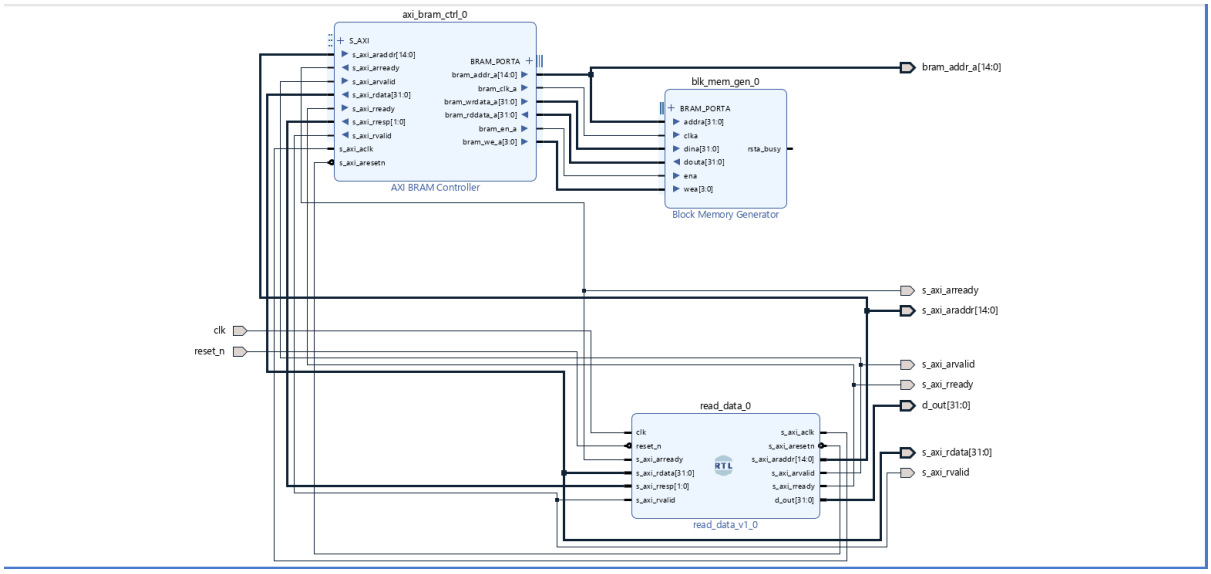

Figure 3: Q2 Block design

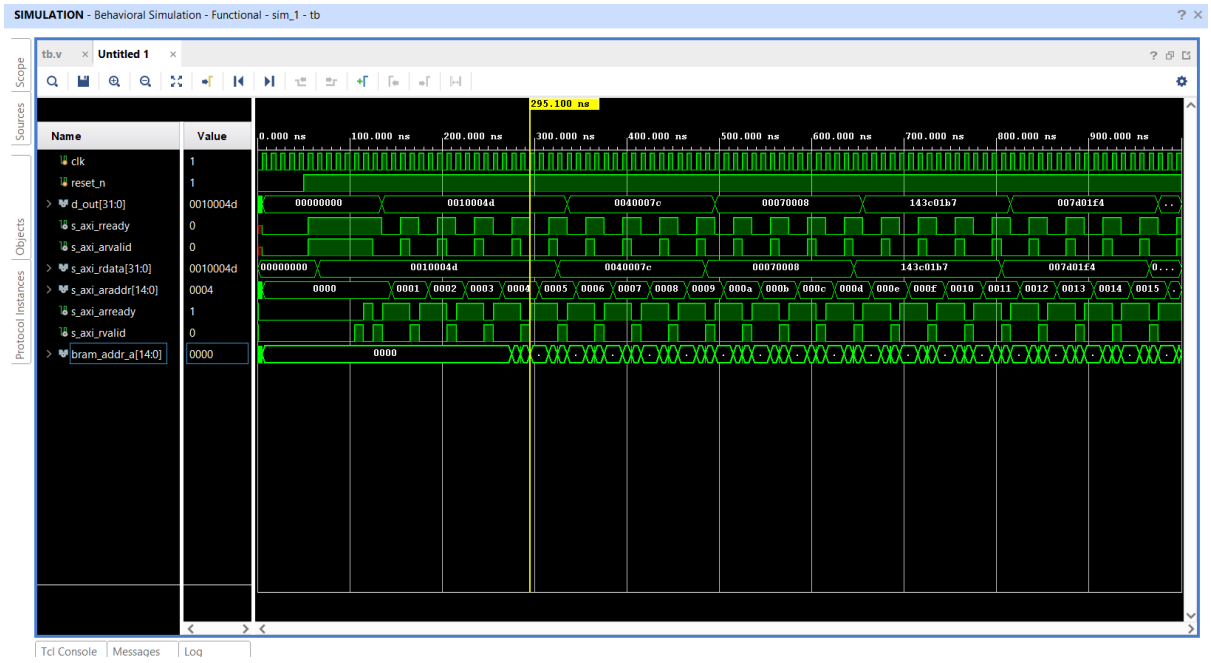

Figure 4: BRAM reader

3 Question 3

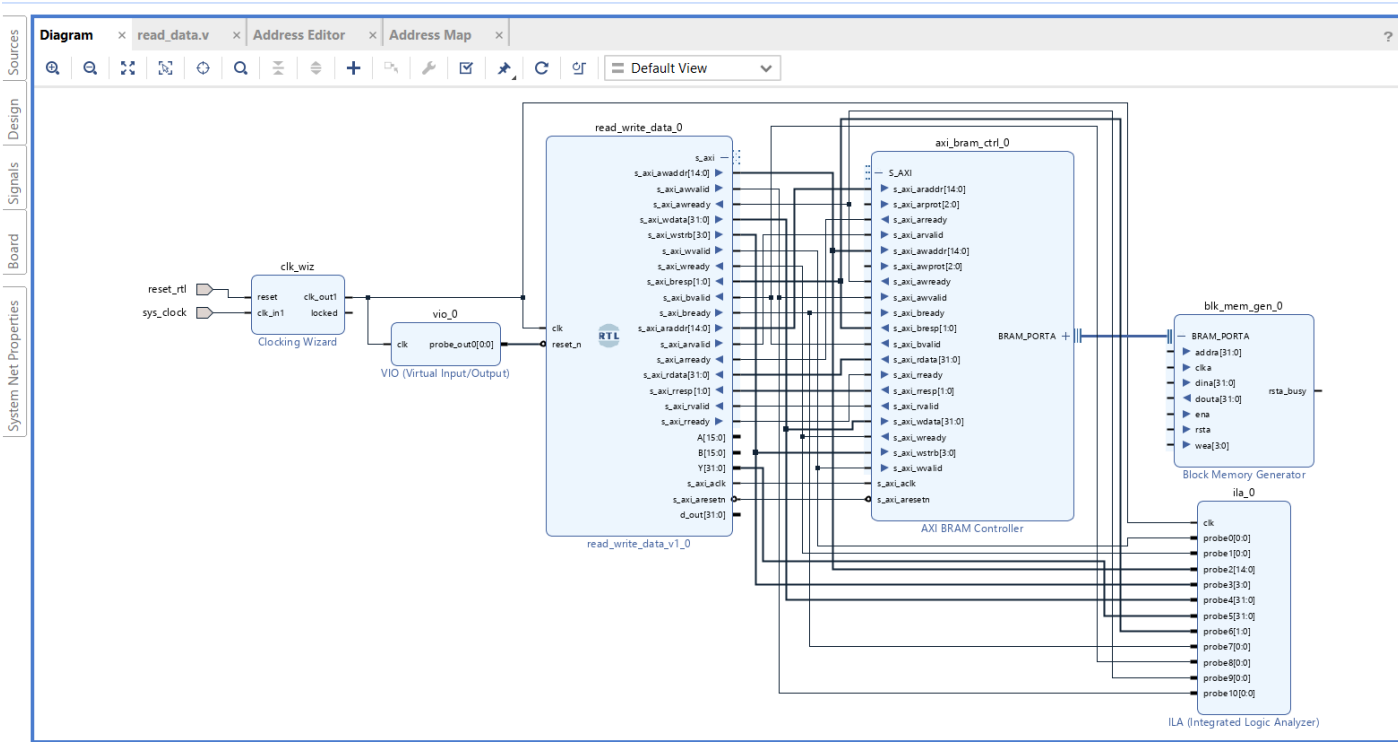

Figure 5: Q3 Block design