EE800 – High Speed Interconnects: Signaling and Synchronization
Assignment 1-A: Phase Detectors, DLL & PLLs

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1 Question 1 : Half-Rate Phase Detector

1.1 Design and Implementation

The phase detector circuit comprises of 4 latches and 2 xor gates as shown in the figure 1 . The two xor gates generate the "Error" and "Reference" signals . The clock frequency is half of data frequency .The output of each latch tracks its input for half a clock period and holds the value for the other half . The transient analysis is shown in figure 3 .

The error pulse start at data transition and ends at the next clock transition where as reference pulse starts at a clock transition and ends at the next clock transition , thus having half clock period . If the clock transitions are aligned at the center of data bit (ideal condition) error pulse width will be half of reference pulse width thus the actual error is defined as : twice the "error" minus "reference" . Thus the phase detector outputs the average value of this actual error .

$$PD_{out} = Average(2XError - Reference)$$

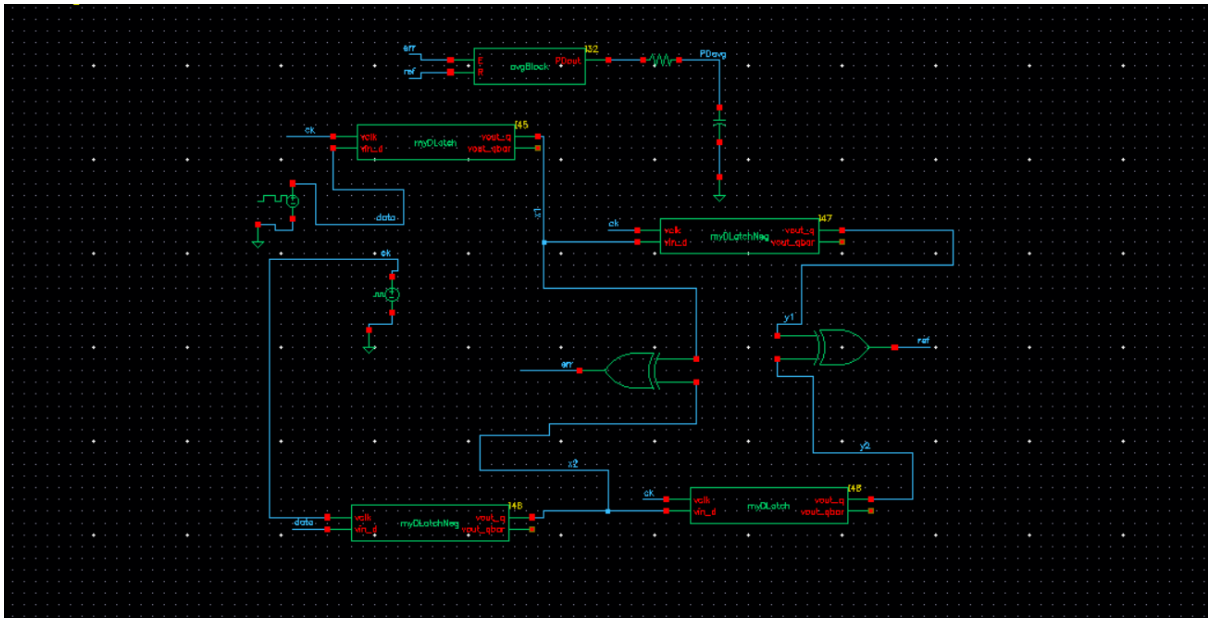

Figure 1: Schematic

1.2 Simulation Setup

To characterize the phase detector, a 20 Gbps binary sequence signal is applied and a 10 GHz clock with 50% duty cycle is applied with an offset of 1 MHz (thus sweeping a phase of 2π in $1\mu s$) . PRBS with a bit period of 50ps and rise-fall times of 10ps was used to model the data sequence . Voltage pulse source of period 99.99ps , rise-fall times 10 ps and pusle width of 39.995ps was used to model the clock . The logic high voltage was set to 1V and the low voltage as 0V . The rise-fall times at the output of xor gate and D latches was set to 5ps and their propogation delay are 8ps . One D latch (named "myDlatch") was designed to read data when the clock is high while the other(named "myDlatchNeg") was designed to do the same when the clock is low . The output of these latches (x1 and x2) were passed through xor gate generating the "error" signal . Thus

error signal outputs 1 if data transition has occured . These signals are further passed to the next latches as shown in the schematic(figure 1) to generate the output signals (y1 and y2) and their xor generates the reference signal .Thus y1 and y2 contain samples of data at both rising and falling edges of clock .

A separate block(named "avgBlock") was designed to compute 2*Error-Reference whose output was passed through RC filter for finding the average . The resistor and capacitor values were set such that the cutoff frequency was approximately 7 times the offset frequency($R = 2.2K\Omega$ and $C = 10pF$) .

$$f_c = \frac{1}{2\pi RC} = 7.234MHz$$

1.3 Results

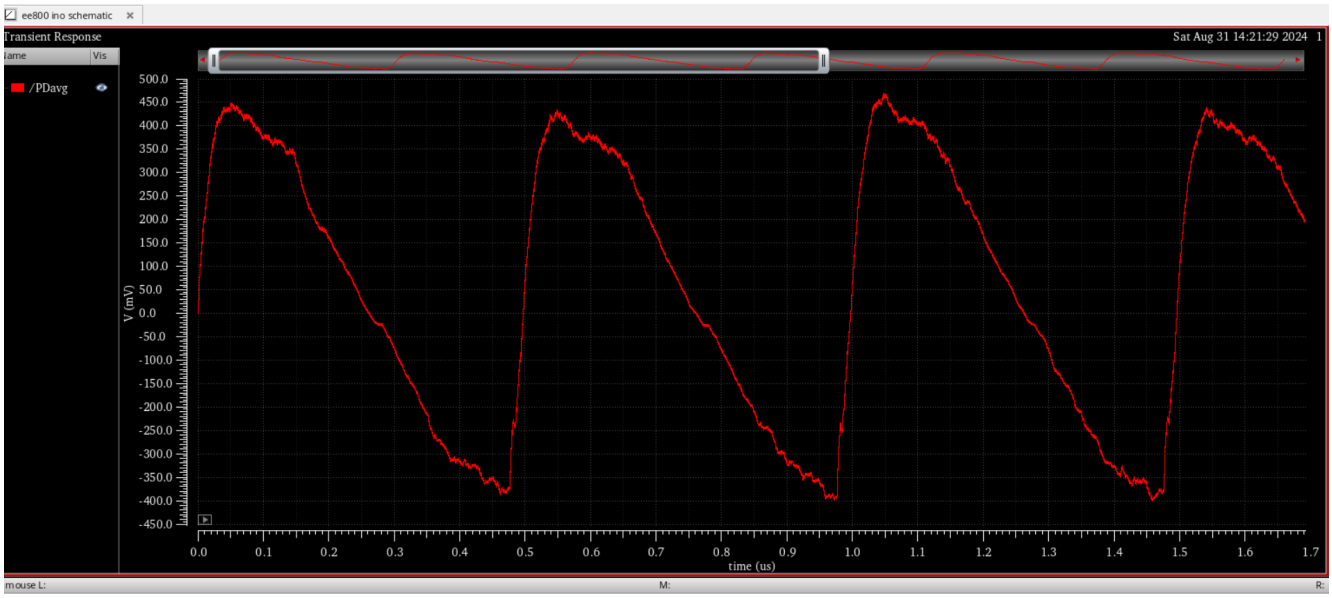

Figure 2: Phase Detector Output

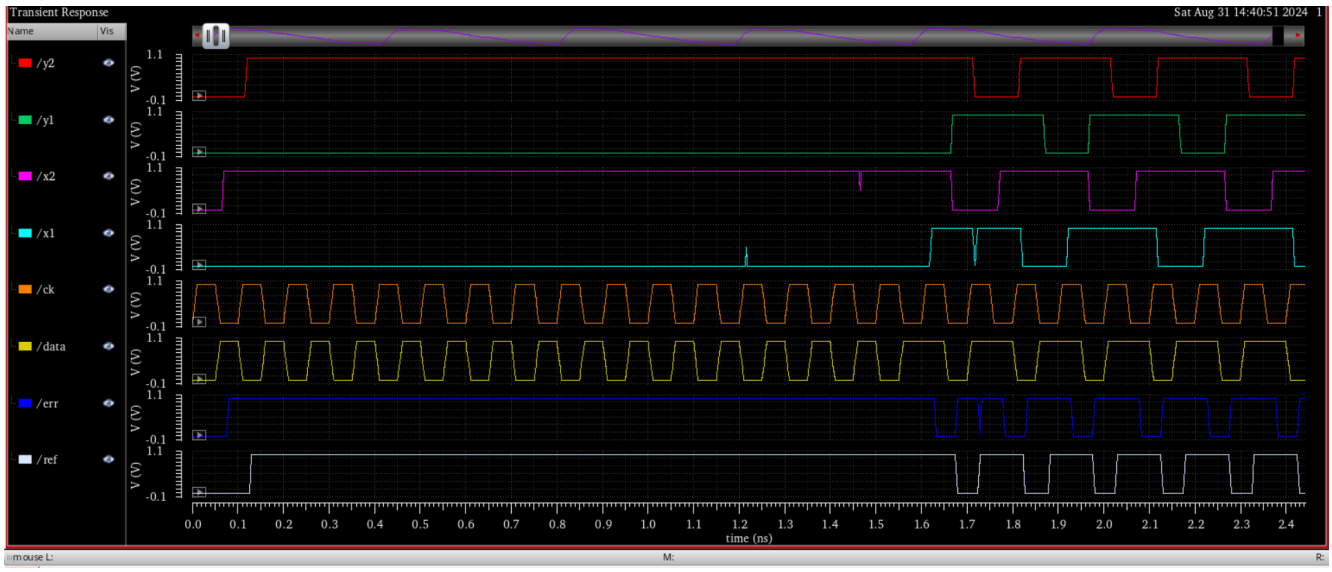

Figure 3: Transient Response

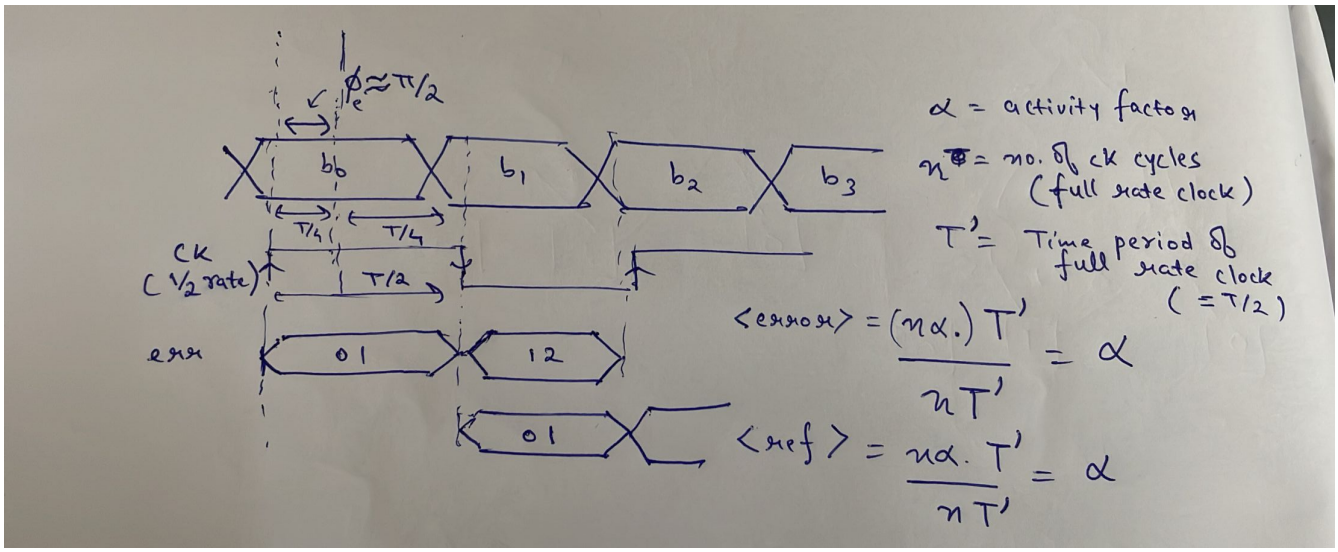

Figure 4: Calculations

1.3.1 Phase Detector Gain

The error pulse width starts at data transition and ends at the next clock transition(either rising or falling edge) and thus error pulse width will have maximum duration(equal to the half the period of clock) at phase error $\phi_e = \pi/2$. Also reference pulse width is always half the clock period . Let the activity factor be α . Therefore at $\phi_e = \pi/2$, $Average(Error) = \alpha$ and $Average(Reference) = \alpha$

$$Avg(2Error - Reference) = 2Avg(Error) - Avg(Reference) = 2\alpha - \alpha = \alpha$$

For $\phi_e = 0$ the clock is aligned perfectly at the center of data bit and Avgerage(2 Error - Reference) = 0 . Thus , the phase detector output rises from 0 (at $\phi_e = 0$) to maximum value of α ($\phi_e = \pi/2$)

$$Gain = \frac{\alpha}{\pi/2} = \frac{2\alpha}{\pi}$$

For random source like PRBS $\alpha = 0.5$. So , theoretically $gain = \frac{1}{\pi}$ which is approximately 0.318 V/rad .

1.4 Discussion

The phase detector gain obtained from simulation is approximately 0.2801 V/rad (reaches peak value of approximately 0.44V from 0V in roughly $0.5\mu s$ corresponding to $\pi/2$ phase sweep) which is slightly lower than the theoretical one assuming ideal components .

The simulation result deviates from the theoretical one because neither the data bits nor the clock have sharp transitions they have non zero rise and fall times which causes fluctuations in data bit sampling by the latches . Also additional delays of xor gates and latches impact this gain .

2 PLL Based Clock and Data Recovery Circuit Design

2.1 VCO Design

2.1.1 Current Starved VCO Design

The design is based on a oscillating feedback of inverters. 3 inverters are connected in series and the final and initial inverters are also connected to close the loop. Depending on the control voltage V_{ctrl}, the output frequency of the pulses generated is varied.

The inverters are created as a CMOS device, with comprising NMOS and PMOS both having width = 45nm and lengths = 120nm and 240nm respectively.

In the schematic, V_{ctrl} controls a Voltage-Controlled Current Source which is set to have 2 μMhos of gain. The parameters are set such that the current is range bound between 0 to 2 μA. Further, a constant DC current source of 13μA is placed in parallel to get the frequency offset. Figure 5 shows the VCO schematic as constructed.

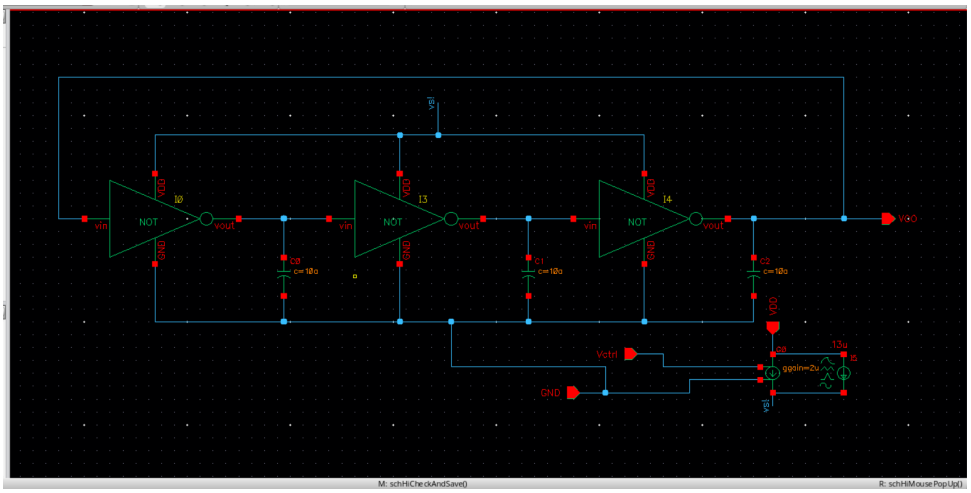

Figure 5: VCO Schematic

2.1.2 VCO Frequency vs Control Voltage

The VCO was characterised by changing V_{ctrl} from 0.6V to 1V. Individual transient analysis was performed at 0.1V steps. The frequency was found by running it through the calculator function $freq$(VT("/out"), "rising"), where *out* is the label for the VCO out line. VCO output is initialized at 0V. Figure 6 shows the characterisation.

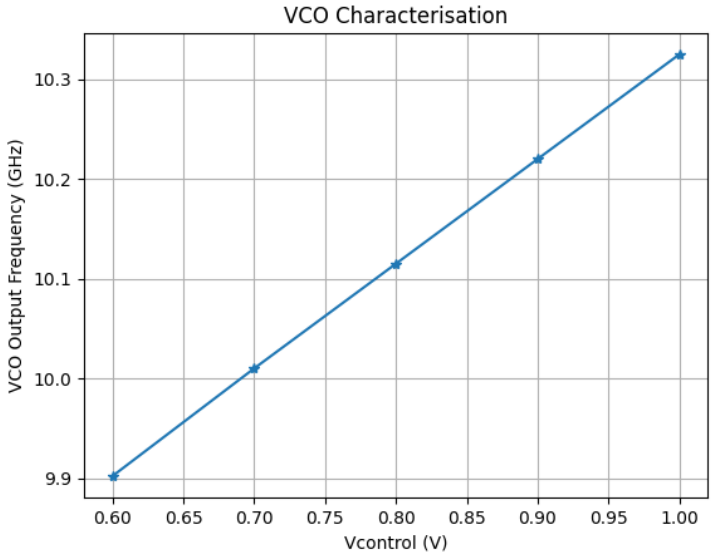

Figure 6: VCO Frequency vs Control Voltage

It can be noted that the frequency is 10.11GHz at 0.8V control. The gain factor is approximately 1.1GHz/V.

2.2 Loop Filter Design

2.2.1 Phase Margin Analysis

The MATLAB code that was given was run and the parameters were fiddled with to get nearly 52.4 degrees of phase margin.

The parameters were: $I_{CP} = 100\mu A$, $C_1 = 5pF$, $R_1 = 10k\Omega$, $C_2 = 0.6pF$, $N = 1$.

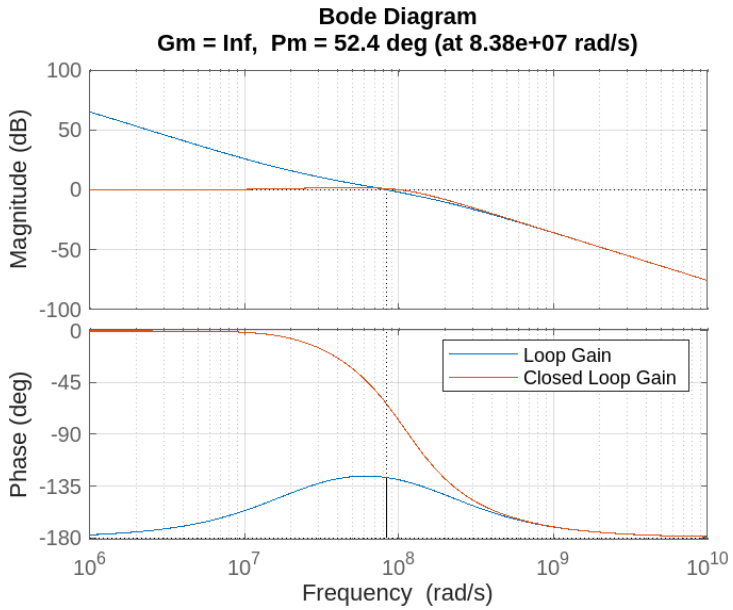

Figure 7: Bode Plot - Magnitude and Phase

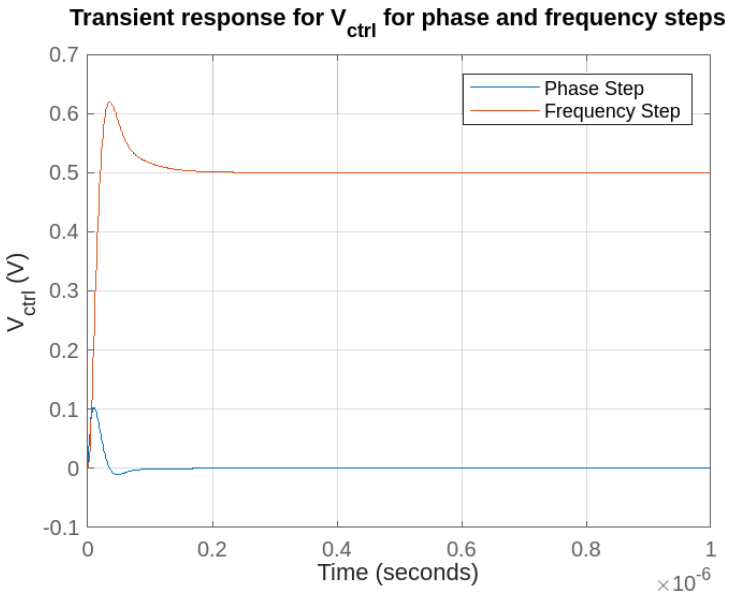

Figure 8: Frequency and Phase Impulse Responses

2.2.2 Transient Simulation

The PLL was now constructed by using the PD from Q1. The smoothened PD output was fed into a VCCS which was set to have a gain of 100μMhos to model the charge pump. This current was fed into a loop filter consisting of RC values as taken from the MATLAB simulation. The filtered voltage is now V_{ctrl} which is fed into the VCO block and the output line is sent to the initial clock.

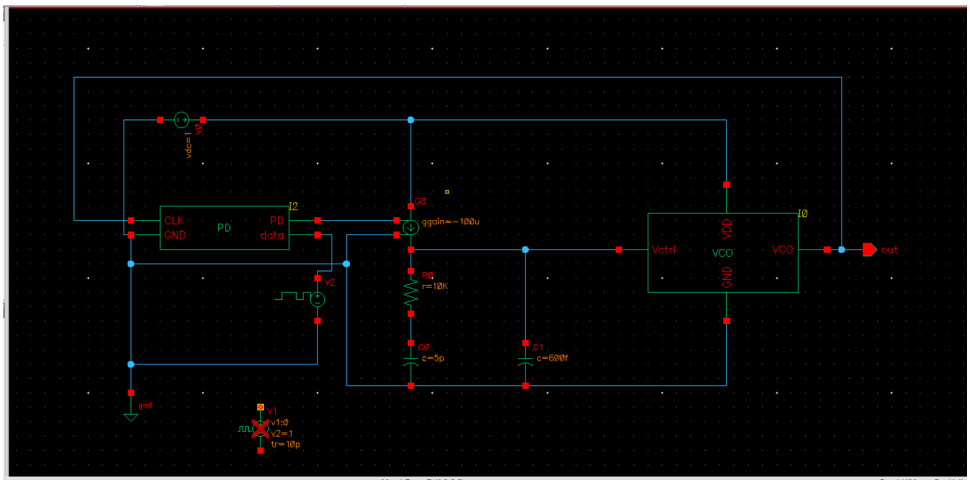

Figure 9: PLL Schematic

The data is ran at 20Gbps using a PRBS generator. The expectation is that the PLL eventually locks at a 10GHz signal as there is a half-rate PD. The VCO output and V_{ctrl} are initially set at 0V and 0.8V respectively for analysis.

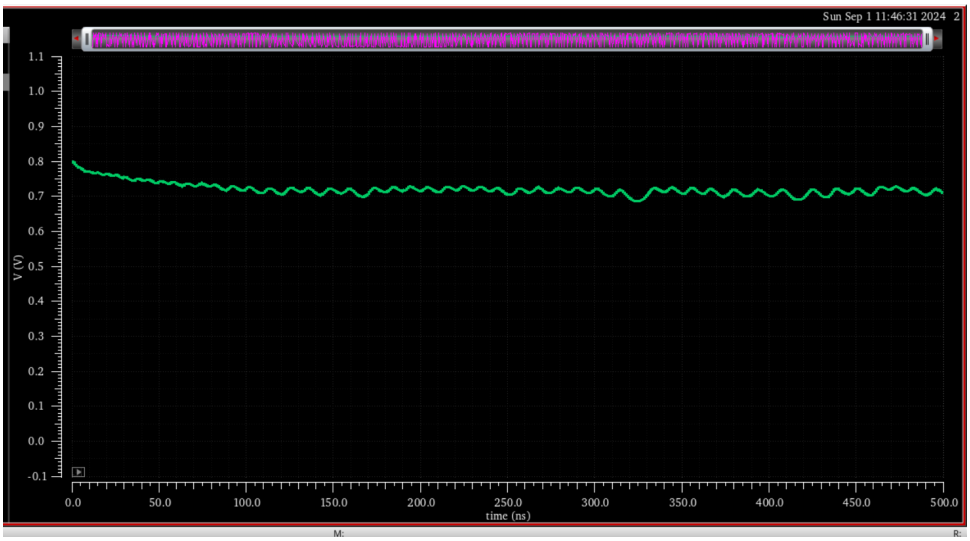

Figure 10: Control Voltage vs Time

2.3 Eye Diagram Analysis

The control voltage stabilises after 300ns. The eye diagram of the data signal and the clock should reveal a eye opening, with the clock signal edges in the middle of a data pulse. Since, the clock is supposed to run at 10GHz, 100ps is considered as the eye period.

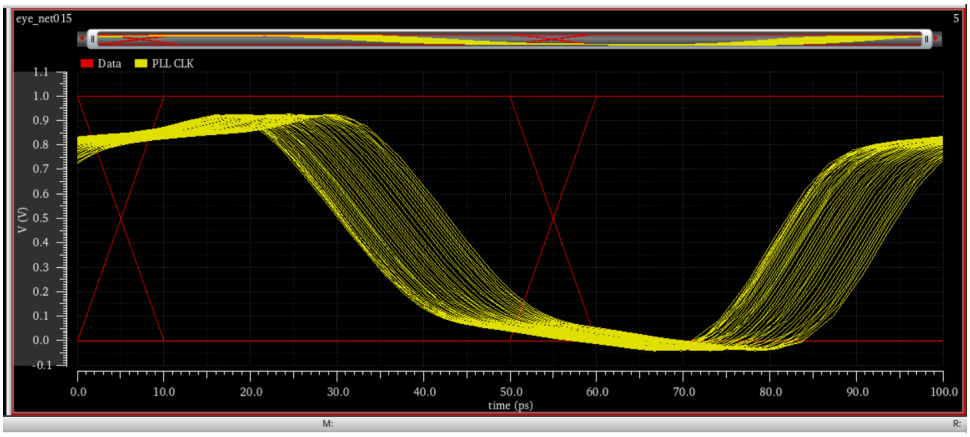

Figure 11: Eye Diagram of Clock and Data Signal