FERROELECTRIC CAPACITANCE MEASUREMENT DEVICE

PROTOTYPE

USER MANUAL

Created By:

TUE-21 Team of EDL 2023-24
Aaryan Sharma, Devesh Soni,
Mrudul Jambhulkar & Aditya Kabare

Contents:

PRELIMINARY INSTALLATIONS

Before using the device, certain software needs to be installed. These are:

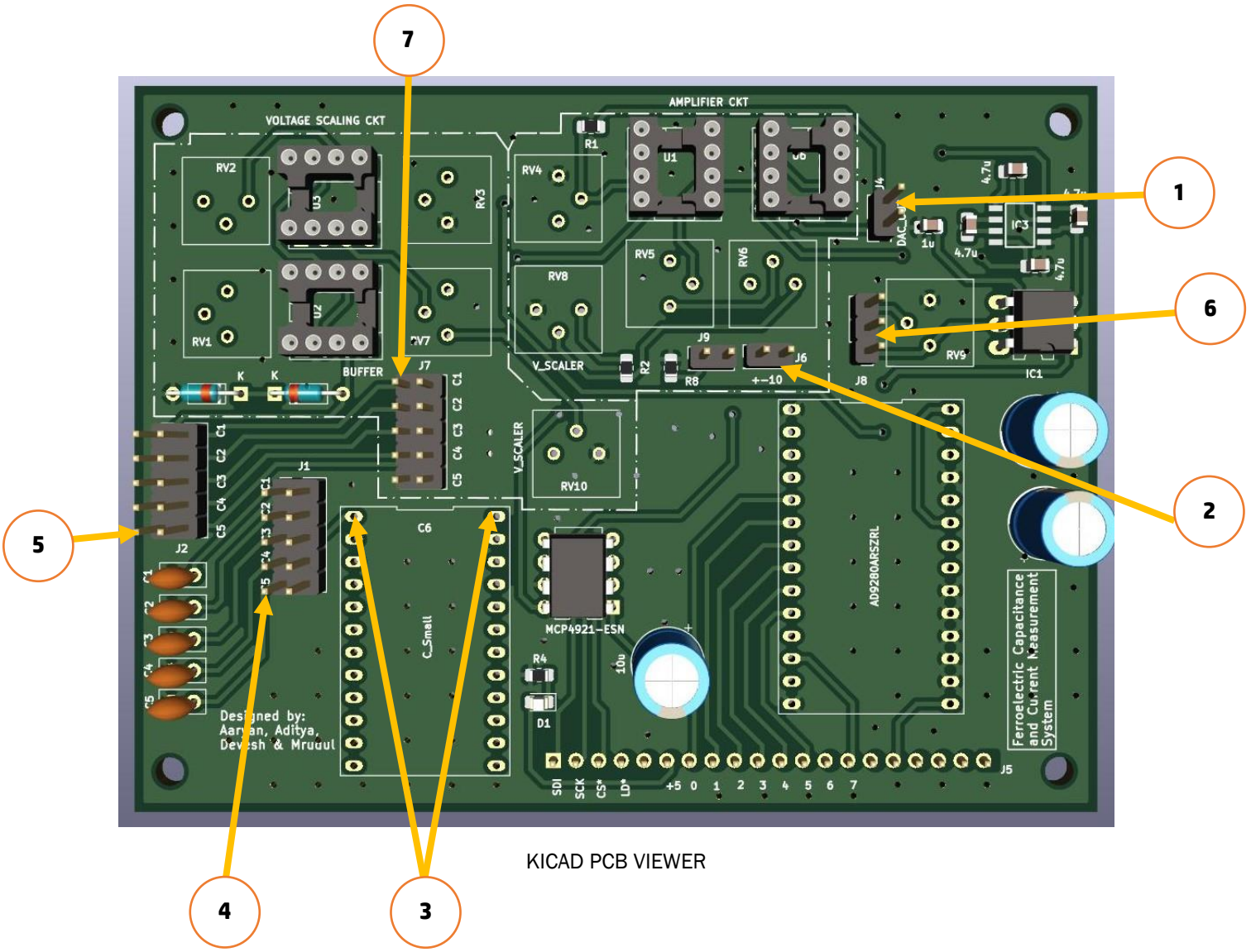
1. Quartus Prime Lite*
2. Intel® Cyclone® IV Device Support
3. Prolific Serial PL2303 Driver

Windows sometimes auto-updates this driver which renders it unusable. The ‘Device Manager’ will show this device to be PHASED OUT SINCE 2012. Simply, uninstall the device. Disconnect the driver and install it again.

4. Python
    a. (Additional Libraries Required: PyQt5, serial, matplotlib, numpy, scipy)

** Latest Edition is preferable, if not, then the latest “Programmer” software needs to be separately installed and the “USB-Blaster” driver in its files needs to be installed*

SETTING UP THE DEVICE



KICAD PCB VIEWER

First, the board has connections to be made. Forward direction of flow in circuit design is mentioned in brackets.

1. ***To feed output of DAC into Amplifier Circuit:***
   Connect the two pins on J4 in the top-right area of PCB.
   (Flow is from bottom pin to top pin)

2. ***To supply amplifier output to capacitor line:***
   Connect the two pins on J6 in the center-right area of PCB
   (Flow is from left pin to right pin)
3. ***Connect Test Capacitor:***
   Connect test capacitor across the top-most horizontal row of C6. (Flow is from right pin to left pin)

4. *Choose Reference Capacitor:*
   Connect the pins on the same horizontal row of J1 to connect test and reference caps. The reference capacitors are in the same order on J1 as they are visually seen from the same orientation.

   For example, in the picture above, connecting pins on the last row means choosing the last capacitor C5.
   (Flow is from right pin to left pin)

5. *To tap voltage at Reference capacitor:*
   Connect the pins on the same horizontal row of J2 feed voltage to ADC. The row to be connected is at same position as the reference capacitor.

   If C5 was chosen, as mentioned before, then the last row on J2 should be connected.
   (Flow is from right pin to left pin)

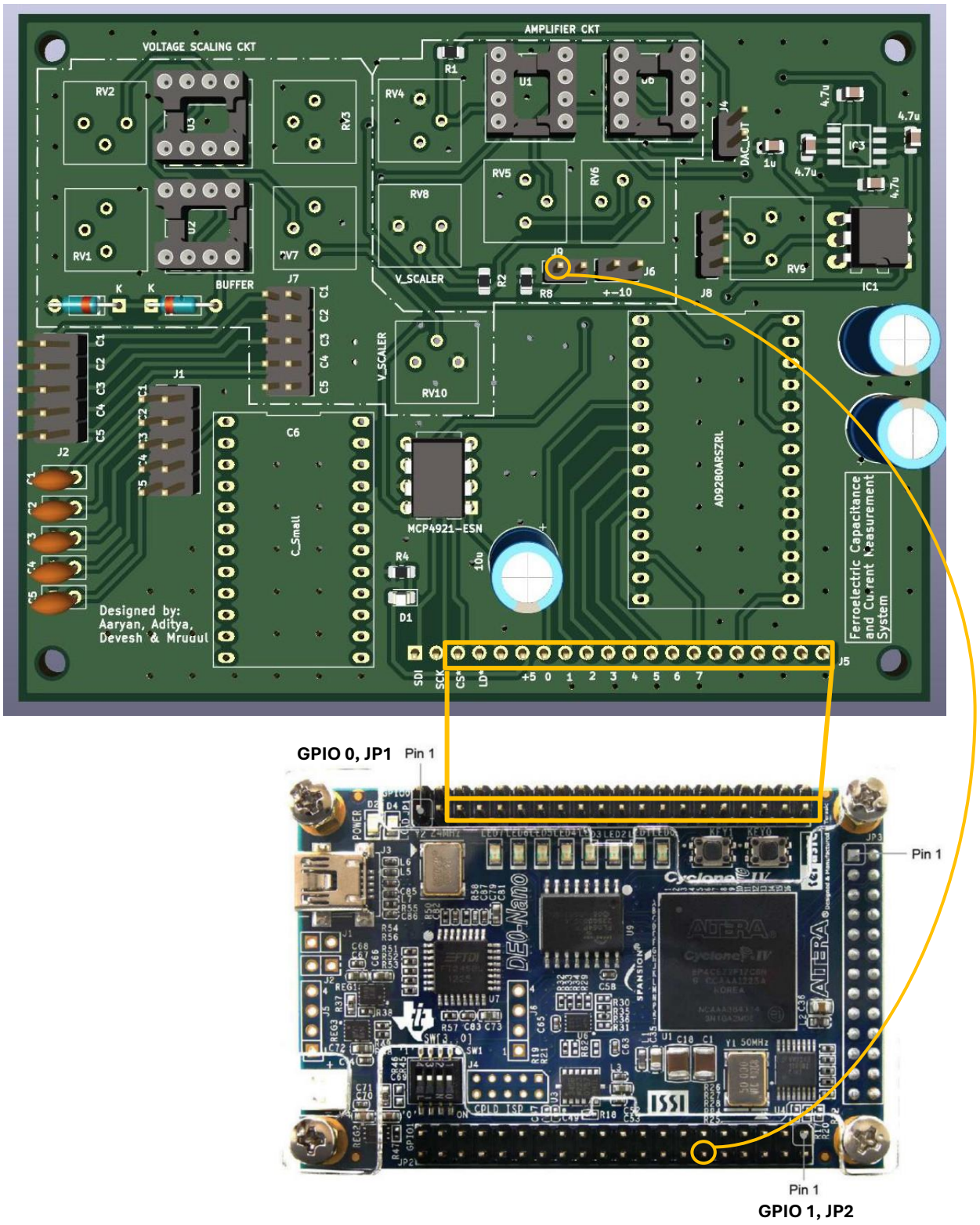
6. *Powering the ADC:*
   Connect bottom two pins of J8 in the right area of PCB, beside J6
   (Power flow is from bottom pin to middle pin)

Note:

7. *In case a reference capacitor is needed to be discharged for any reason, remove connections on J1 and J2 done in step 4 and 5, and connect pins of the corresponding horizontal row in J7 (center-left on PCB)*

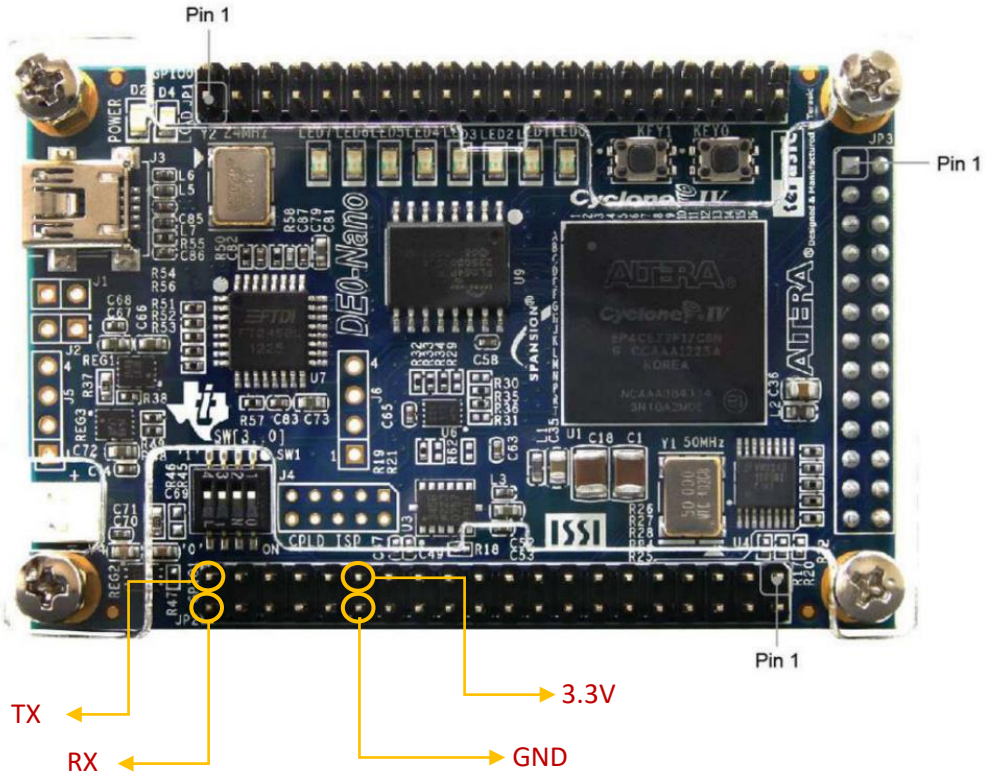
Next, the PCB board has header pins J5 at the bottom of the PCB to be inserted into the GPIO-0 expansion header of the FPGA board as shown in the below figure.

Also, connect the GND pin on GPIO-1, with the left pin of J9 on PCB



Once the FPGA is powered through its separate USB cable, the green light on the PCB will light up, signifying the connections of PCB to FPGA are proper.

Finally, FPGA – UART module connection is to be made. The UART module is the Prolific PL2303 USB-UART connector.



Connections are on the 15th and 20th row of **GPIO-1**. PL2303 also contains a 5V pin which need not be connected.

The device is now ready to use. Plug PL2303 and the USB connection of FPGA to power the devices.

A PICTURE OF THE FINAL ASSEMBLY IS SHOWN ON THE LAST PAGE

OPERATING THE DEVICE

ON QUARTUS PRIME

1. Open MCP4921.qpf file through Quartus.

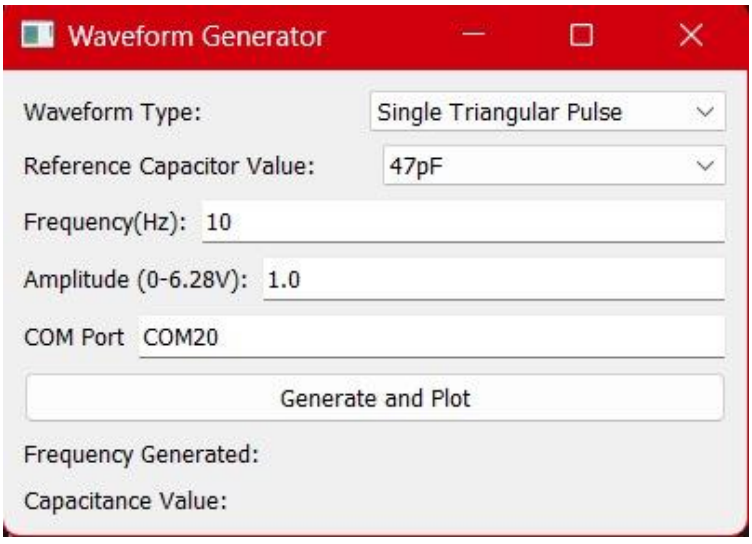
2. On the top pane, do Tools > Programmer to open the Programmer.

3. The programmer window shows MCP4921.sof file loaded. Go to hardware setup and select USB-Blaster as currently selected hardware.
   If the USB-Blaster option does not come, its driver needs to be installed.

4. After this, the start button on the left pane should be active. Press it, and in a short duration, the bar on the top-right should show 100% successful.

5. The code is now successfully put on the FPGA. Do not disconnect the FPGA cable, otherwise the process needs to be repeated.

ON GUI



1. Run the GUI.py file

2. This opens a window where the parameters can be specified

   a. Waveform Type: Single Triangular, Double-Up Double-Down Triangular (PUND) and Continuous Triangular

*(Note: Generating a continuous wave does not produce any output on interface, however a continuous triangular wave is generated. It **cannot be stopped** through GUI. The FPGA needs to be powered down)*

b. Reference Capacitor Value: Select the reference capacitor connected. This does **not** select the capacitor on the board, this is merely for plotting and analysis.

c. Frequency: Up-to 13900 Hz can be specified. Since any arbitrary frequency is not possible, the nearest possible is generated and shown at the bottom of the GUI when generated.

d. Magnitude: Range is specified on the GUI. This is the peak voltage magnitude generated for the series capacitors.

   (*Note that this **not** the voltage range that the test capacitor will go through. The test capacitor voltage magnitude will be strictly less than this)*

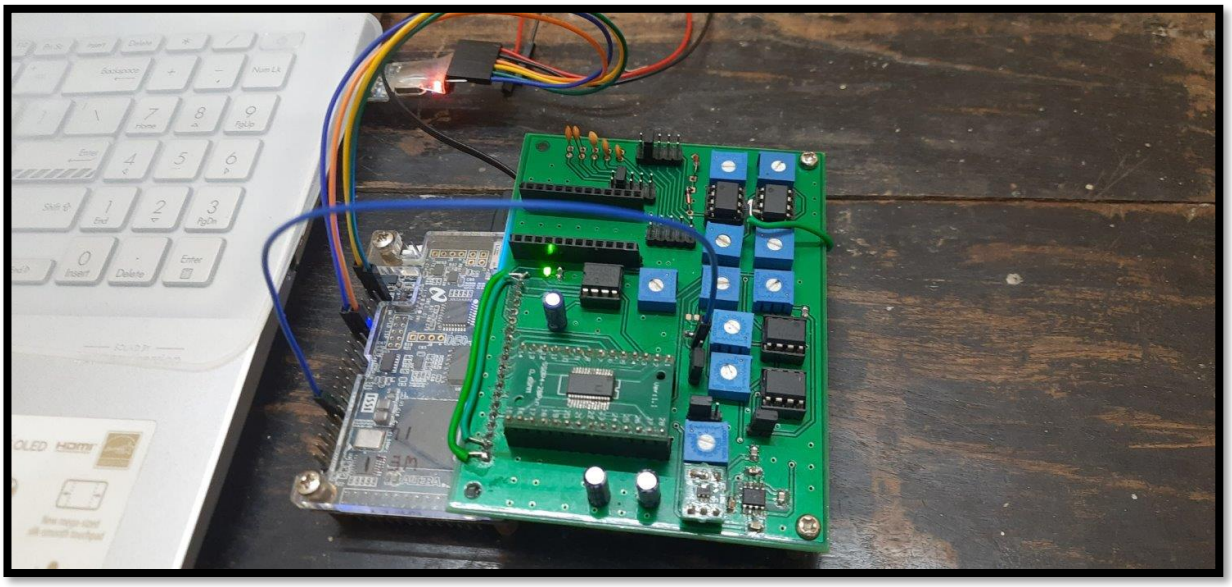
e. COM Port: This is the port in which the PL-2303 is inserted. This can be found through the Device Manager.

3. Pressing ***'Generate and Plot'*** will send the required pulse for the first two wave types and plot three different graphs. Voltage output to the series caps, voltage at reference cap and Q-V curve of the Test Capacitor.

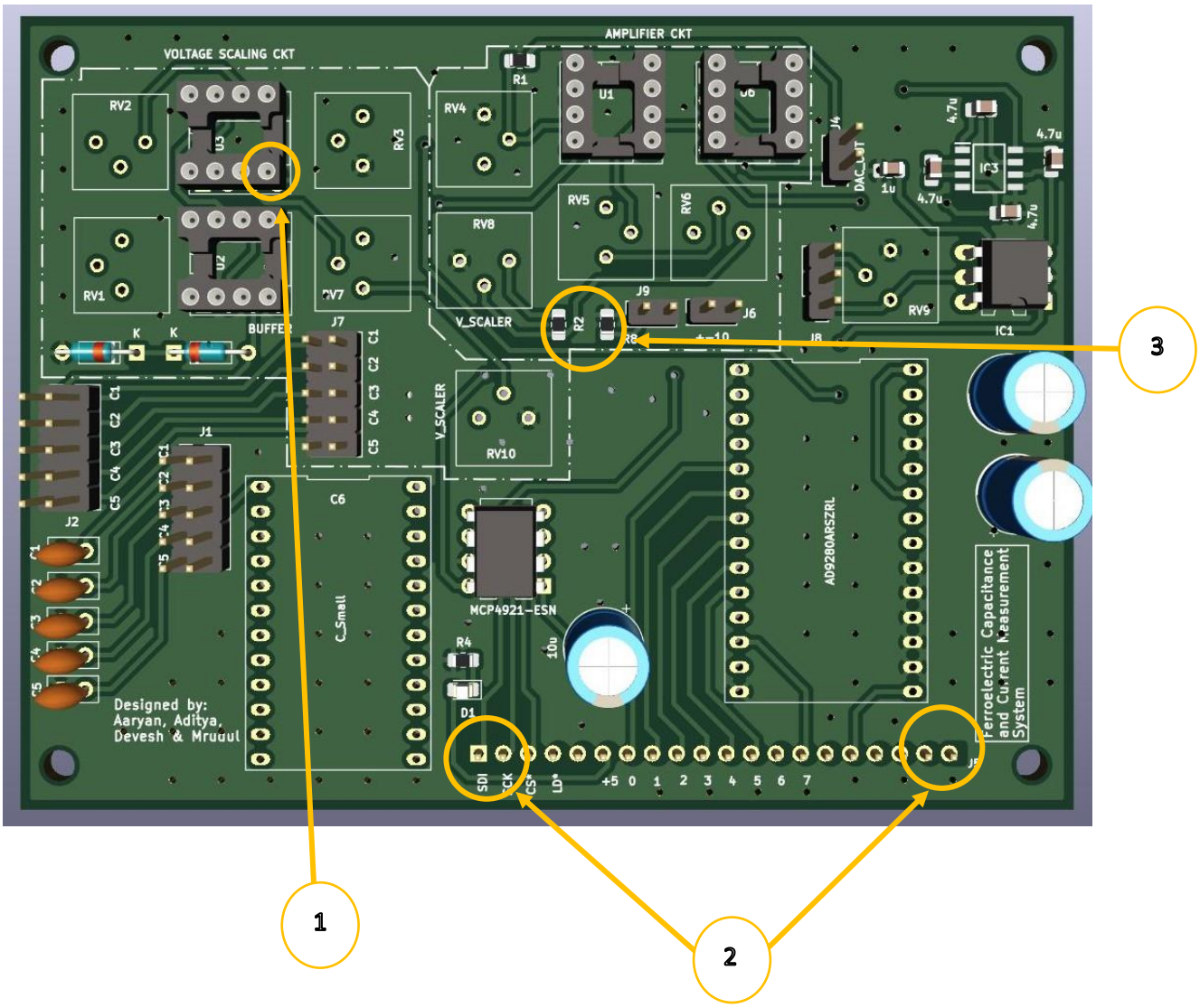
   (*The first generation after code dump produces noisy output initially. Hence the first run should be discarded)*

4. For a linear test capacitor, the capacitance value is shown by line-fitting of obtained plot.

FINAL ASSEMBLY



SOME PCB CORRECTIONS



1. V- pin of TL071 amplifier was connected to -12V externally. Through traces, it is grounded so we made sure to first remove the trace and then connect -12V from nearby source through single strand wire.
2. Position of SDI and SCK have been shifted to last 2 pin headers.
3. Resistor R8 and R2 have been desoldered and the pads are shorted to ground.