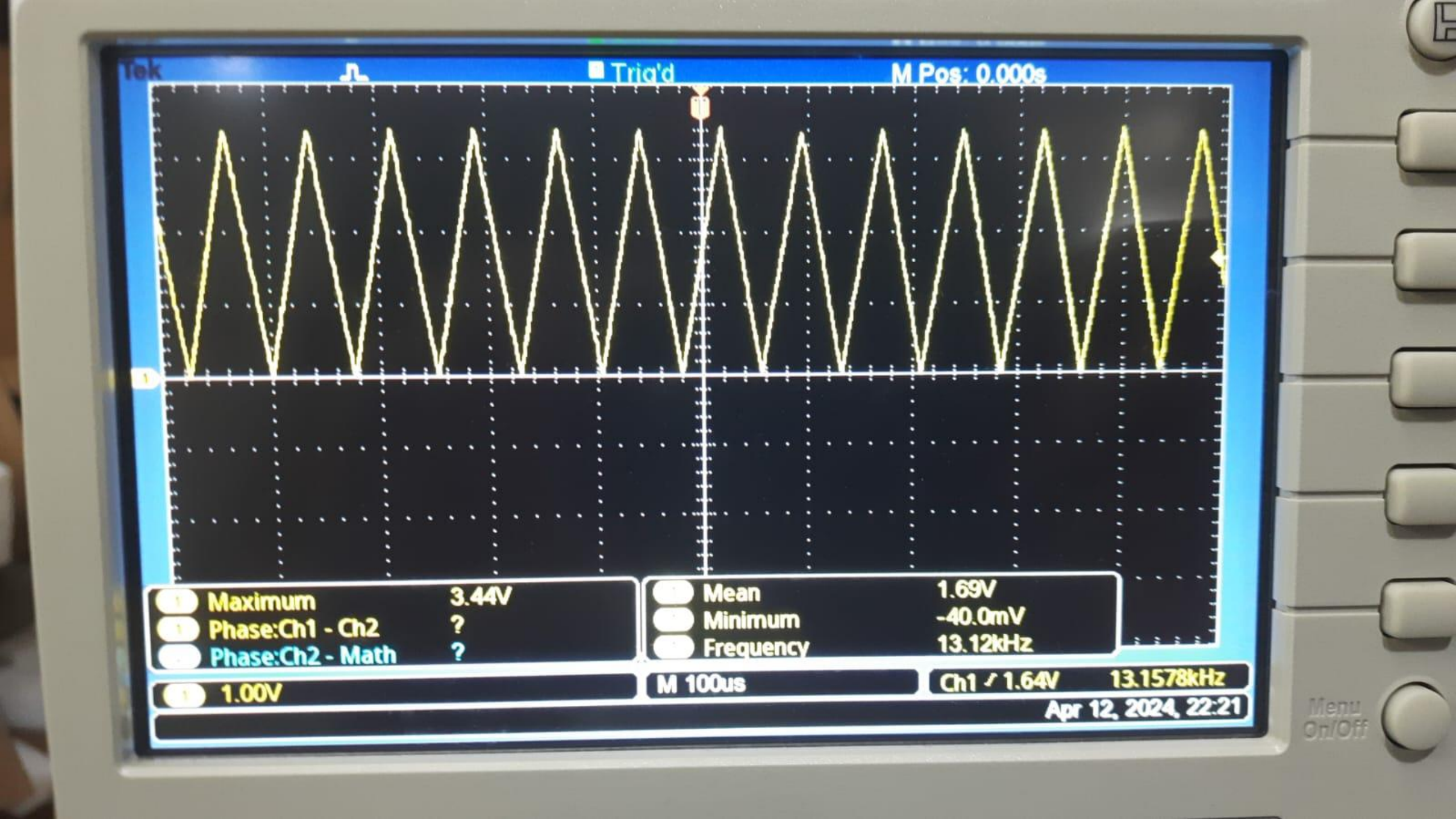
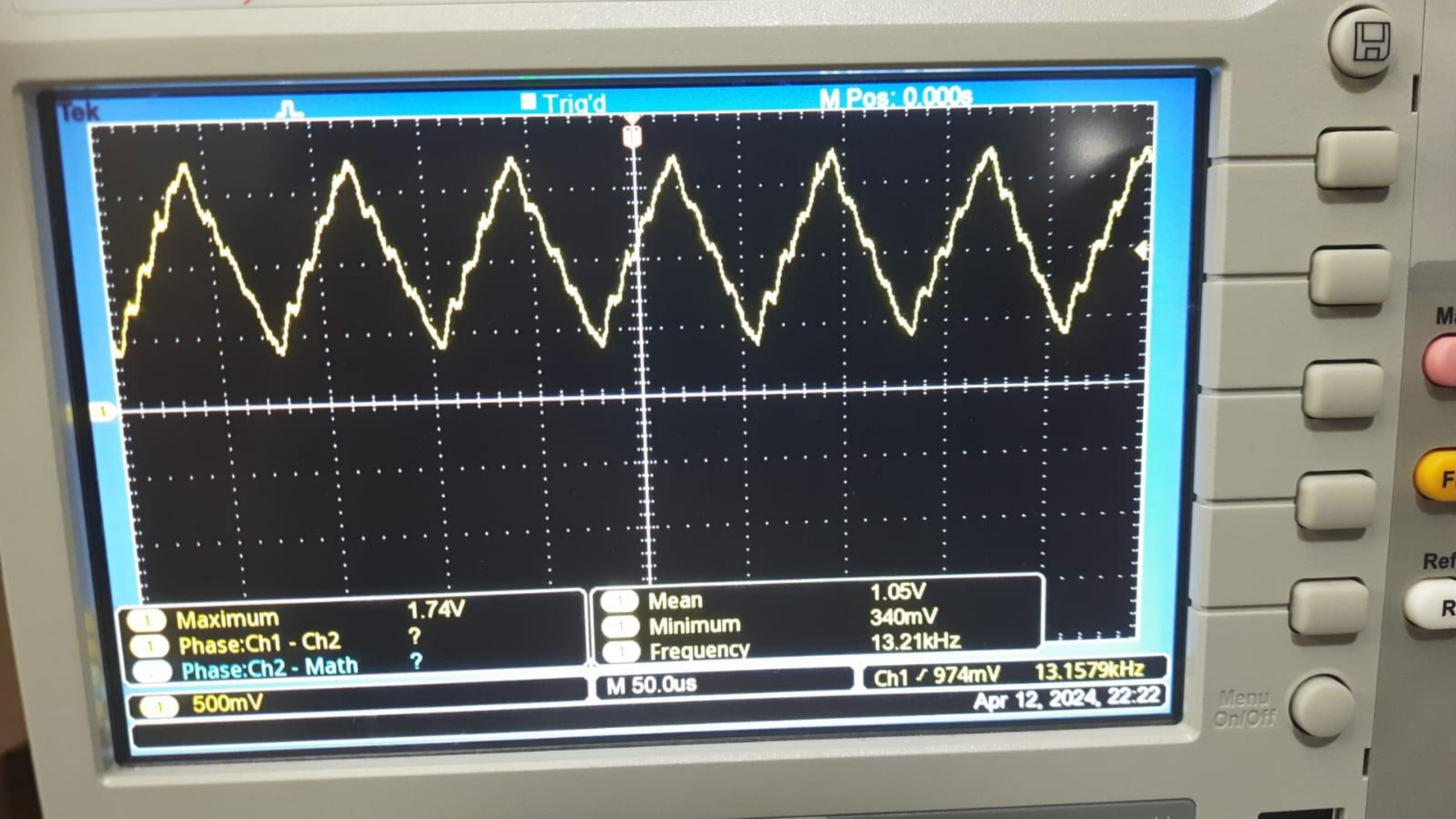
Ferro-electric Capacitance and Current Measuring system

Aaryan Sharma (210110003), Aditya Kabare (21d070009), Devesh Soni (21d070025),
Mrudul Jambhulkar (21d070044)

We present a ferro-electric capacitance measurement device, that automates data collection and analysis, eliminating the requirement of large lab instruments and their high costs. Enhancing materials science research with affordable features.

- Test capacitor value = 100pF
- 3 experiments will be performed
- Expected Q-V graph = linear
- Additional graphs shown - DAC output, ADC input (@ 2kHz)
- Maximum achievable frequency by DAC (*Shown on DSO*)


Tek
Trig'd
M Pos: 0.000s
Maximum 3.44V
Phase:Ch1 - Ch2 ?
Phase:Ch2 - Math ?
Mean 1.69V
Minimum -40.0mV
Frequency 13.12kHz
1.00V
M 100us
Ch1 ∕ 1.64V 13.1578kHz
Apr 12, 2024, 22:21
Menu On/Off


Tek
Trig'd
M Pos: 0.000s
Maximum 1.74V
Phase:Ch1 - Ch2 ?
Phase:Ch2 - Math ?
Mean 1.05V
Minimum 340mV
Frequency 13.21kHz
500mV
M 50.0us
Ch1 ƒ 974mV 13.1579kHz
Apr 12, 2024 22:22
Menu On/Off

Target specifications achieved

- Max amplitude (-6.28 to 6.28V)
- Max frequency at DAC output = 13.12kHz
- Can measure capacitance as low as 100pF reliably (*rough data for lower values available)*

Overview of Methodology

FUNCTION GENERATOR

Generates high frequency triangular wave pulse for 3 different experiments. Achieves frequency change by changing counter values in FPGA

- Low-Cost DAC (MCP4921)
  - 12-bit precision
  - SPI (20MHz)
- **Amplifier circuit:**
  - Scalers and Shifters with fine and coarse adjustments

BUFFER CIRCUIT
to prevent loading

TEST CAPACITOR

REFERENCE CAPACITOR BANK

Collection of 5 different ceramic capacitors. Value of reference capacitor is always higher or equal to test capacitor

POSSIBLE VALUES

- 220pF
- 150pF
- 100pF
- 68pF
- 47pF

Additionally added discharge resistors, to discharge capacitors when not in use

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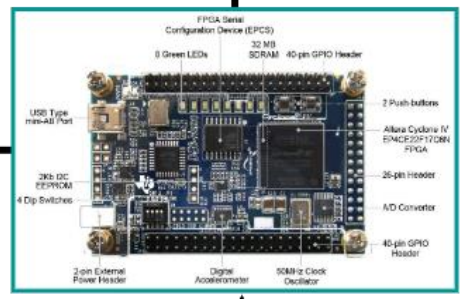
DATA COLLECTION AND ANALYSIS

ADC (AD9280)

- Sampling rate- 32MSPS
- 8-bit parallel data transfer
- Operates between 2.7V - 5.5V
- Input voltage range from 0-3.3V, so requires a **voltage scaling circuit**

GUI

- Sending experiments settings using **UART.**
- Plotting Q-V curve using python libraries

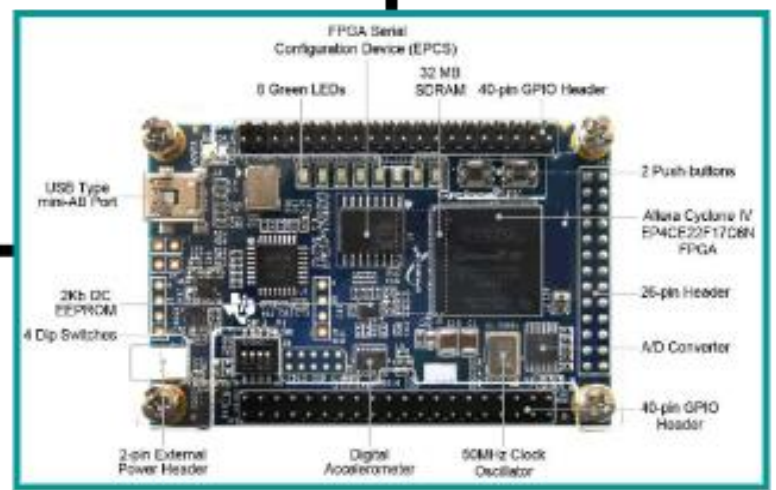


POWER BLOCK

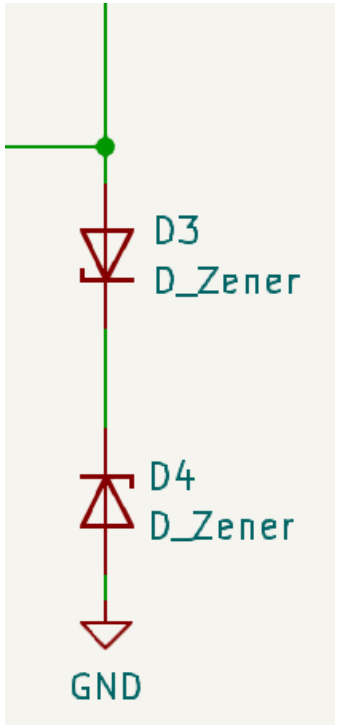
5V Power supply from FPGA pin itself as current requirements are very low

- 5V voltage regulator (L7805)
- 3.3V voltage regulator(AP2112K)
- 5 to 10V voltage regulator (MAX680)

coarse adjustments



DATA COLLECTION



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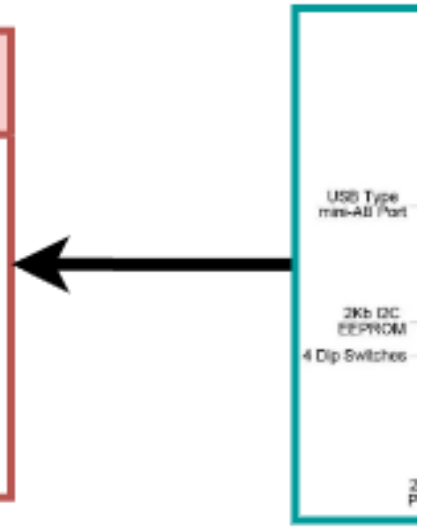

5V –Zener diodes makes clipper circuit and drains excess current , thus protecting the circuit and components like ADC

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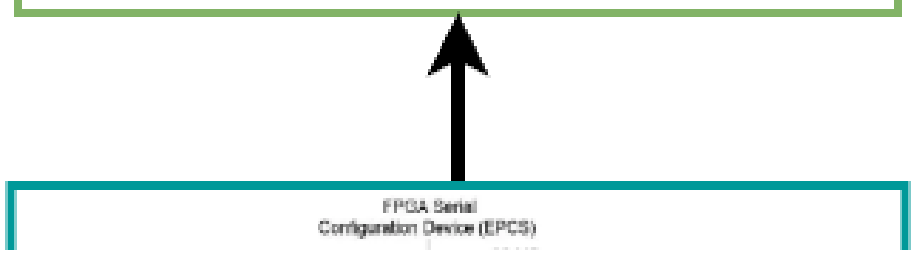

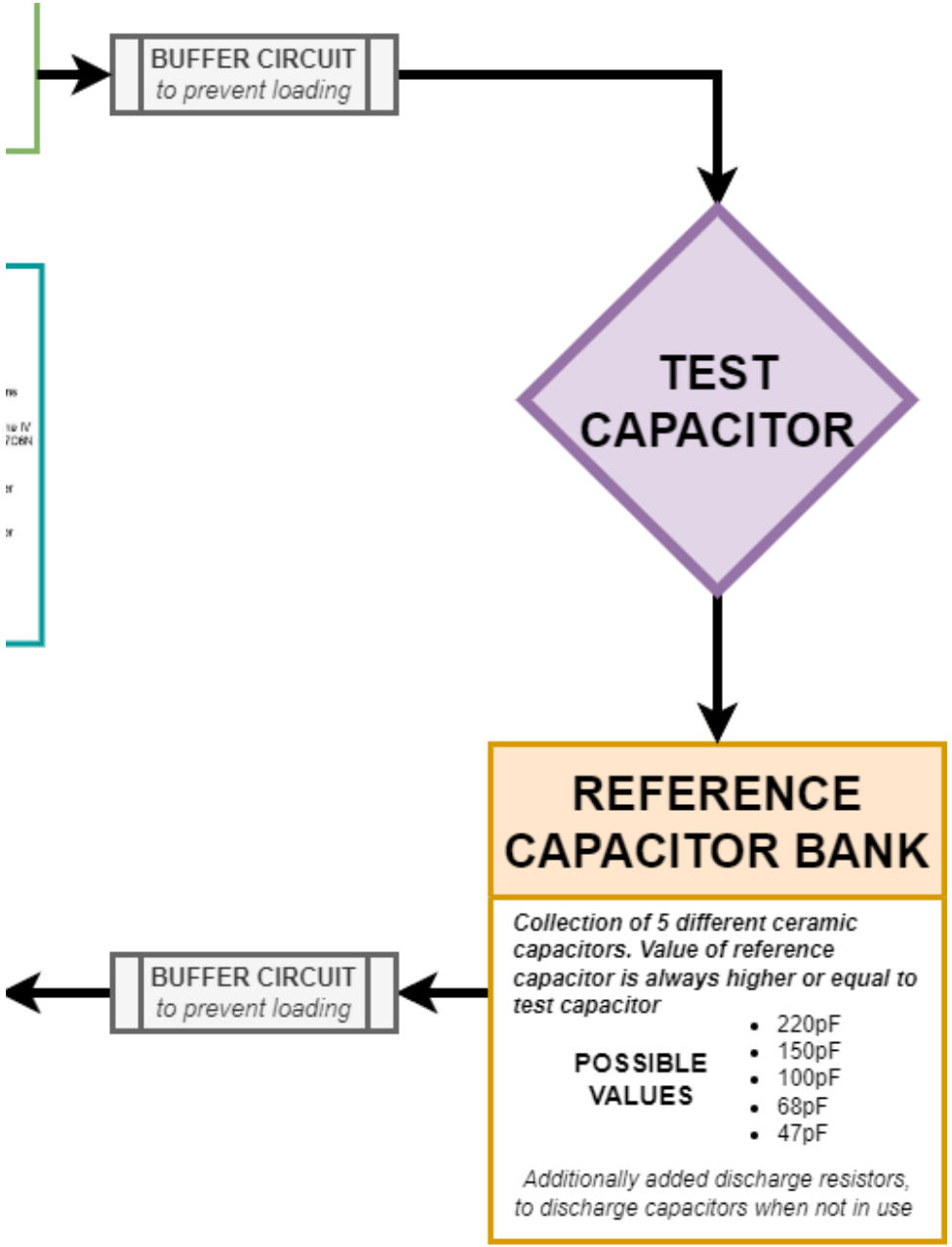
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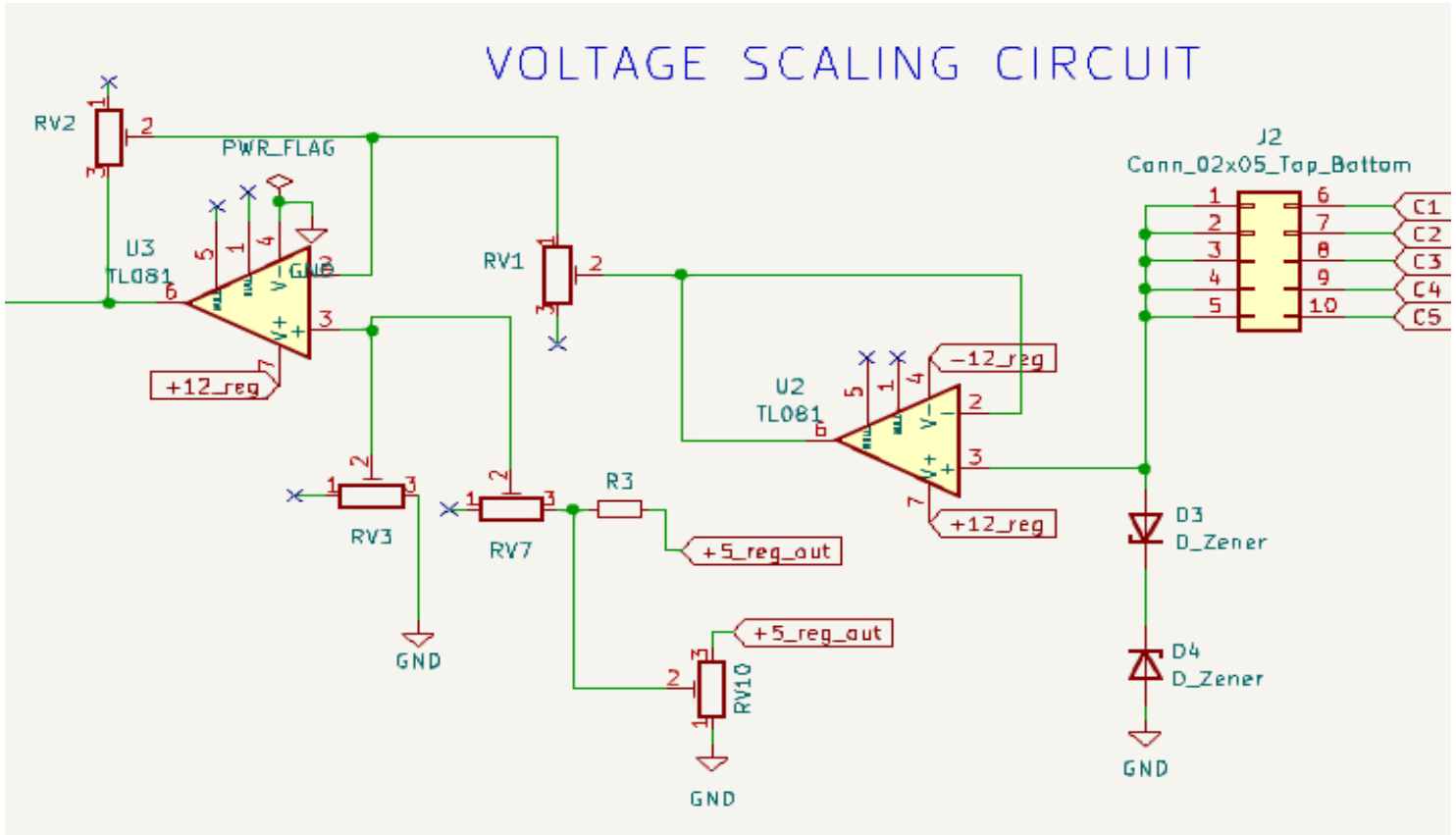

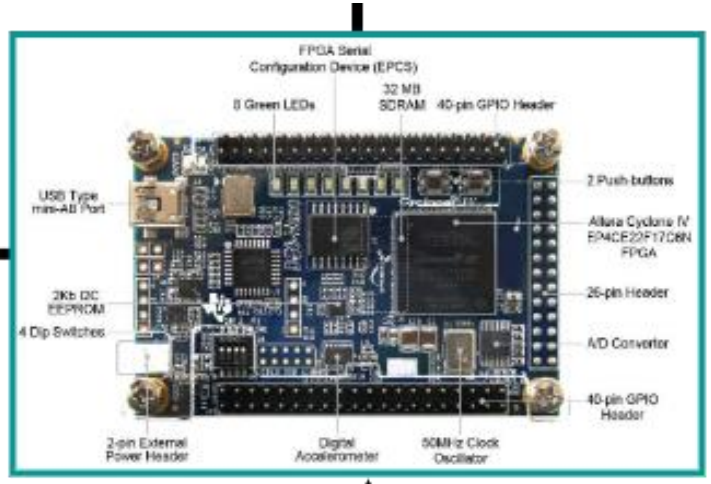

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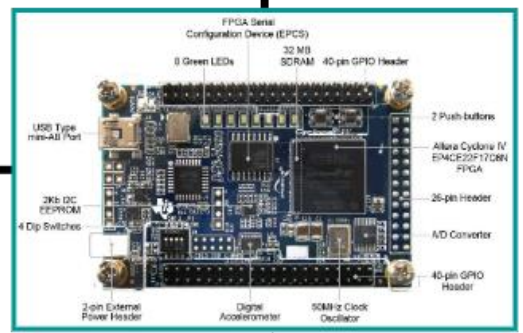

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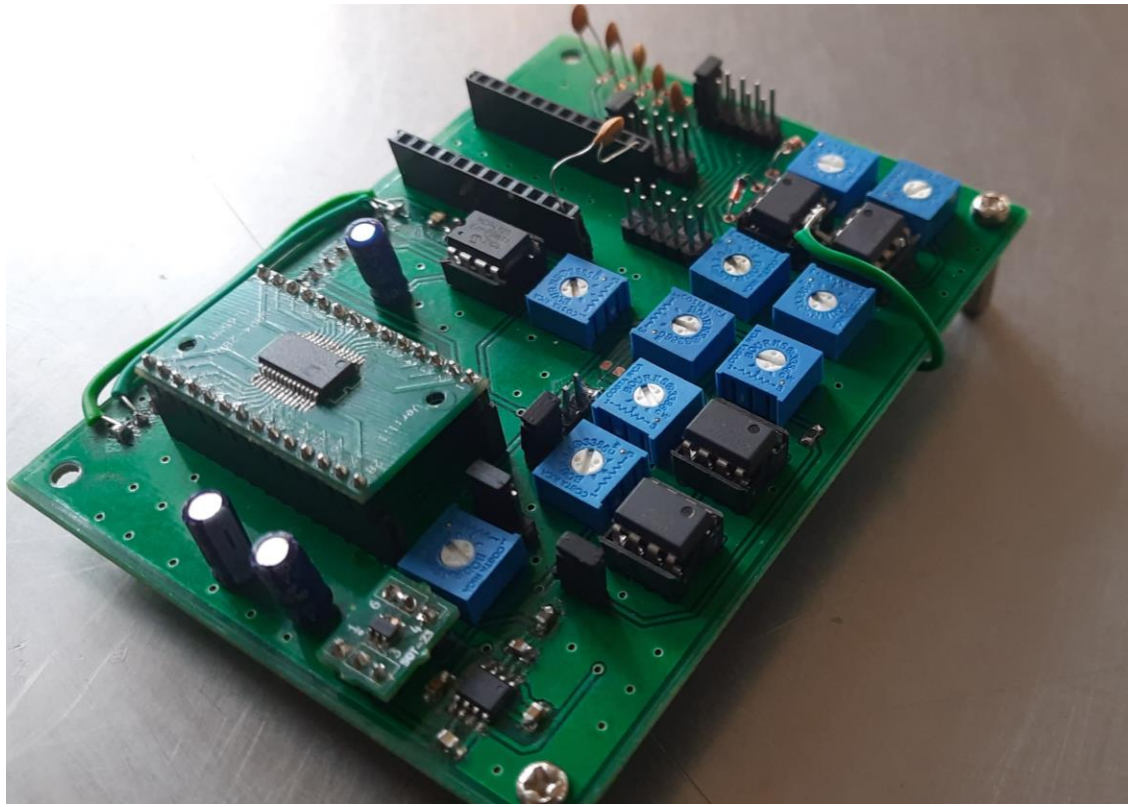
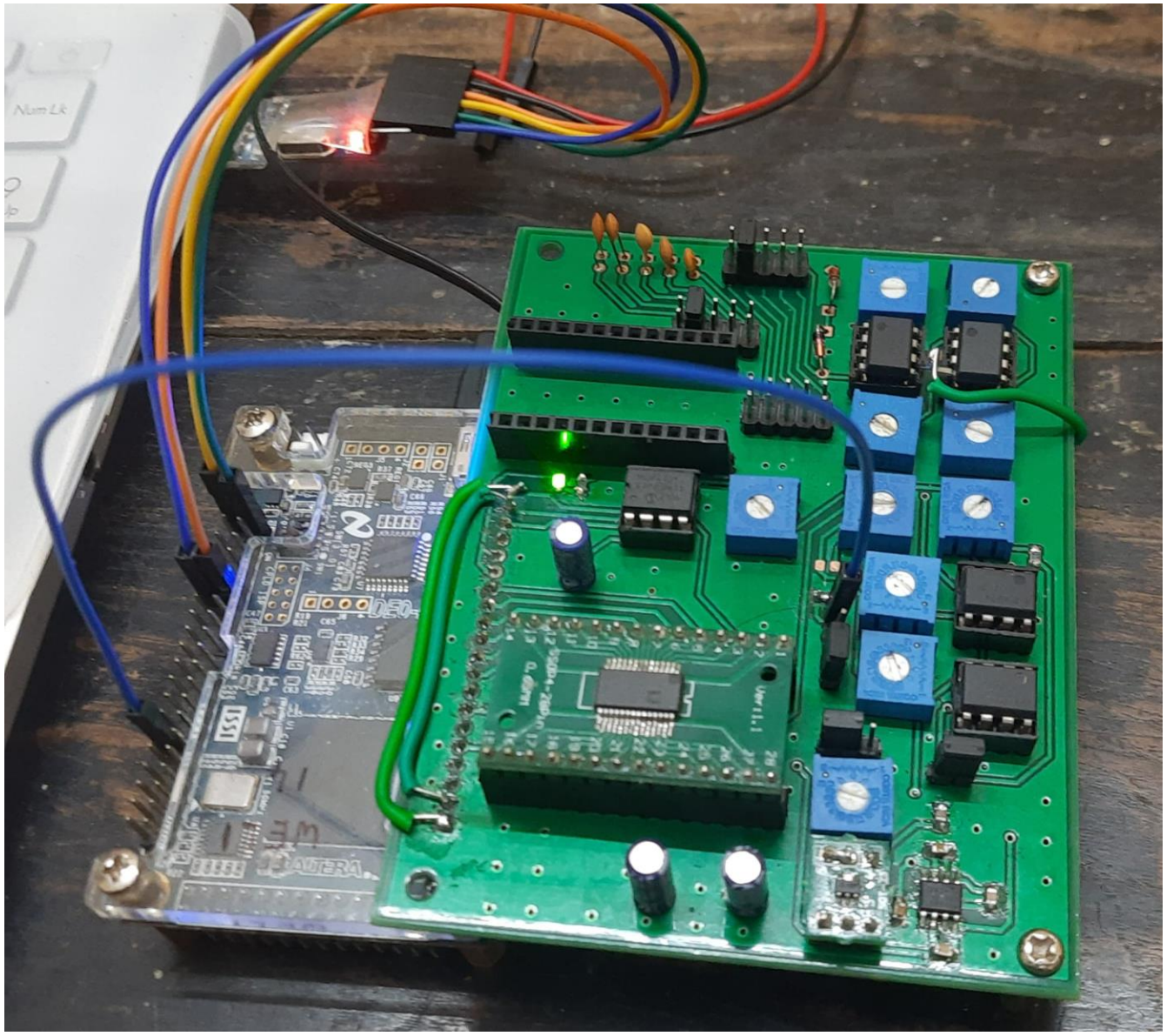


Fig.1 Individual Device

Fig.2 Final assembly



Challenges Faced and Potential Solutions

Challenges	Solution	Remarks
Unexpected voltage division across the capacitors of pF order	Use low leakage current diodes	Partial success, problems persist for <100 pF capacitors
Allowing sufficient choice of frequencies	Use of counter delays for finer division alongside clock division	Successful, now allows frequencies in steps of 1kHz up to max
DAC voltage scaling circuit not generating proper triangle wave	Introduce unity buffer before capacitors	Successful, prevents loading effects on voltage scaler
Sampling enough values quickly to plot a good Q-V graph	Use high sampling ADC	Works, bought reasonably priced ADC with high MSPS, trade off on bits
L7805 & MAX680 regulators are inefficient	Bypassed L7805, MAX680 left as is	In-built regulators in FPGA sufficient, MAX680 performs sufficiently at 72%

Conclusion

- **Key functionalities demonstrated**
  - User can give frequency, type of waveform and amplitude as input to perform three different experiments
  - User can visualize different waveforms and its characteristics and thus will obtain a Q-V plot for ferro-electric capacitance.
    **Currently demonstrated on Normal capacitor (Linear graph)*
- **Key lessons learnt**
  - Analysis of datasheet is important !!
  - Early testing and debugging is must.
- **Key gaps**
  - Cannot handle low capacitance values accurately, though rough readings available.
  - ADC signal gets distorted for clock frequency above ~25Mhz
  - Can achieve more number of samples