# fUll ADDER USING HALF ADDER

**full\_adderst:**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity full\_adderst is

Port ( a : in STD\_LOGIC;

b : in STD\_LOGIC;

cin : in STD\_LOGIC; s : out STD\_LOGIC;

cout : out STD\_LOGIC); end full\_adderst;

architecture Structural of full\_adderst is component HA\_normal is

Port ( a : in STD\_LOGIC;

b : in STD\_LOGIC;

sum : out STD\_LOGIC; carry : out STD\_LOGIC);

end component;

component or\_gate is

Port ( A : in STD\_LOGIC;

B : in STD\_LOGIC;

Y : out STD\_LOGIC);

end component;

u1: HA\_normal port map(a,b,temp1,temp2); u2: HA\_normal port map(temp1,cin,s,temp3); u3: or\_gate port map(temp2,temp3,cout); end Structural;

# full\_addertb:

library ieee;

use IEEE.STD\_LOGIC\_1164.ALL;

entity full\_addertb is end full\_addertb;

architecture Behavioral of full\_addertb is component full\_adderst is

Port ( a : in STD\_LOGIC;

b : in STD\_LOGIC;

cin : in STD\_LOGIC; s : out STD\_LOGIC;

cout : out STD\_LOGIC); end component;

signal a,b,cin,s,cout : std\_logic;

begin

u1 : full\_adderst port map(a,b,cin,s,cout);

--stimuli generation a<='0';

b<='0';

cin<='0';

wait for 100ns; a<='0';

b<='0';

cin<='1';

wait for 100ns; a<='0';

b<='1';

cin<='0';

wait for 100ns; a<='0';

b<='1';

cin<='1';

wait for 100ns; a<='1';

b<='0';

cin<='0';

wait for 100ns; a<='1';

b<='0';

cin<='1';

a<='1';

b<='1';

cin<='0';

wait for 100ns; a<='1';

b<='1';

cin<='1';

wait for 100ns; end process; end Behavioral;

# HA\_normal

library ieee;

use IEEE.STD\_LOGIC\_1164.ALL;

entity HA\_normal is

Port ( a : in STD\_LOGIC;

b : in STD\_LOGIC;

sum : out STD\_LOGIC; carry : out STD\_LOGIC);

end HA\_normal;

architecture Behavioral of HA\_normal is

begin

sum<= a xor b; carry<= a and b;

end Behavioral;

# or\_gate :

library IEEE;

use IEEE.std\_logic\_1164.all;

-- Entity declaration

entity or\_gate is

port(A : in std\_logic; -- OR gate input B : in std\_logic; -- OR gate input

Y : out std\_logic); -- OR gate output

end or\_gate;

-- Dataflow Modelling Style

-- Architecture definition

architecture orLogic of or\_gate is

begin

Y <= A OR B;

end orLogic;

