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# hALF ADDER

library ieee;

use IEEE.STD\_LOGIC\_1164.ALL;

entity HA\_normal is

Port ( a : in STD\_LOGIC;

b : in STD\_LOGIC;

sum : out STD\_LOGIC; carry : out STD\_LOGIC);

end HA\_normal;

architecture Behavioral of HA\_normal is

begin

sum<= a xor b; carry<= a and b;

end Behavioral;

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# FULL ADDER

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity full\_adderst is

Port ( a : in STD\_LOGIC;

b : in STD\_LOGIC;

cin : in STD\_LOGIC; sum : out STD\_LOGIC; cout : out STD\_LOGIC);

end full\_adderst;

architecture Structural of full\_adderst is component HA\_normal is

Port ( a : in STD\_LOGIC;

b : in STD\_LOGIC;

sum : out STD\_LOGIC; carry : out STD\_LOGIC);

end component;

component or\_gate is

Port ( A : in STD\_LOGIC;

B : in STD\_LOGIC;

Y : out STD\_LOGIC);

end component;

signal temp1,temp2,temp3 : std\_logic; begin

u1: HA\_normal port map(a,b,temp1,temp2);

u2: HA\_normal port map(temp1,cin,sum,temp3); u3: or\_gate port map(temp2,temp3,cout);

end Structural;

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# or\_gate

library IEEE;

use IEEE.std\_logic\_1164.all;

-- Entity declaration

entity or\_gate is

port(A : in std\_logic; -- OR gate input B : in std\_logic; -- OR gate input

Y : out std\_logic); -- OR gate output

end or\_gate;

-- Dataflow Modelling Style

-- Architecture definition

architecture orLogic of or\_gate is

begin

Y <= A OR B;

end orLogic;

# rca

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-- Company:

-- Engineer:

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-- Create Date: 21.08.2023 15:29:27

-- Design Name:

-- Module Name: RCA - Behavioral

-- Project Name:

-- Target Devices:

-- Tool Versions:

-- Description:

--

-- Dependencies:

--

-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

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library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx leaf cells in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity rca is

Port ( a : in STD\_LOGIC\_vector(3 downto 0); b : in STD\_LOGIC\_vector(3 downto 0); cin : in STD\_LOGIC;

sum : out STD\_LOGIC\_vector(3 downto 0); cout : out STD\_LOGIC);

end rca;

architecture Behavioral of rca is COMPONENT full\_adderst is

Port ( a : in STD\_LOGIC;

b : in STD\_LOGIC;

cin : in STD\_LOGIC; sum : out STD\_LOGIC;

cout : out STD\_LOGIC); end COMPONENT;

signal temp:std\_logic\_vector(3 downto 0); begin

u1: full\_adderst port map(a(0),b(0),cin,sum(0),temp(0));

u2: full\_adderst port map(a(1),b(1),temp(0),sum(1),temp(1));

u3: full\_adderst port map(a(2),b(2),temp(1),sum(2),temp(2)); u4: full\_adderst port map(a(3),b(3),temp(2),sum(3),cout);

end Behavioral;

# RCA\_testbench

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**-- Company:**

**-- Engineer:**

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**-- Create Date: 21.08.2023 15:56:54**

**-- Design Name:**

**-- Module Name: RCA\_tb - Behavioral**

**-- Project Name:**

**-- Target Devices:**

**-- Tool Versions:**

**-- Description:**

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**-- Dependencies:**

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**-- Revision:**

**-- Revision 0.01 - File Created**

**-- Additional Comments:**

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**----------------------------------------------------------------------------------**

**library IEEE;**

**use IEEE.STD\_LOGIC\_1164.ALL;**

**-- Uncomment the following library declaration if using**

**-- arithmetic functions with Signed or Unsigned values**

**--use IEEE.NUMERIC\_STD.ALL;**

**-- Uncomment the following library declaration if instantiating**

**-- any Xilinx leaf cells in this code.**

**--library UNISIM;**

**--use UNISIM.VComponents.all;**

**entity rca\_tb is**

**-- Port ( ); end rca\_tb;**

**architecture Behavioral of RCA\_tb is**

**component rca is**

**Port ( a : in STD\_LOGIC\_VECTOR (3 downto 0);**

**b : in STD\_LOGIC\_VECTOR (3 downto 0); Sum : out STD\_LOGIC\_VECTOR (3 downto 0); Cout : out STD\_LOGIC;**

**Cin : in STD\_LOGIC);**

**end component;**

**signal a,b,sum : std\_logic\_vector(3 downto 0); signal cout,cin : std\_logic;**

**begin**

**u1: rca port map(a,b,sum,cout,cin); process**

**begin a<="0101"; b<="1010";**

**cin<='1';**

**wait for 200 ns;**

**a<="1101"; b<="1000";**

**cin<='0';**

**wait for 200 ns;**

**end process; end Behavioral;**