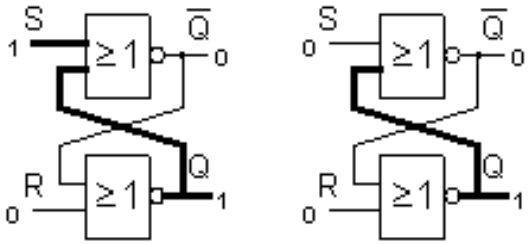
Latches and Flip-flops

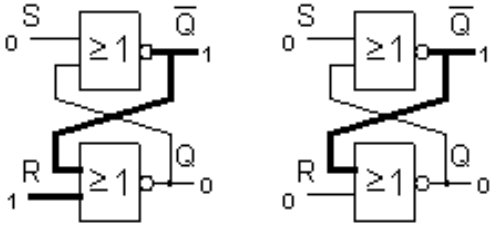
Latches and flip-flops are circuits with memory function. They are part of the computer's memory and processor’s registers.

- SR latch is basically the computer memory cell

Q=1



Q=0



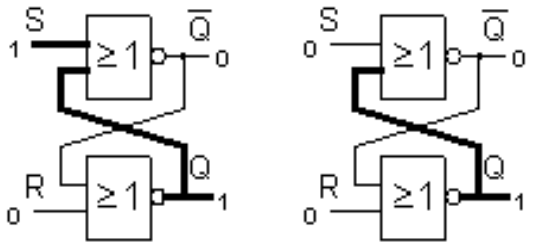
William Sandqvist william@kth.se

SR latch with two NOR-gates

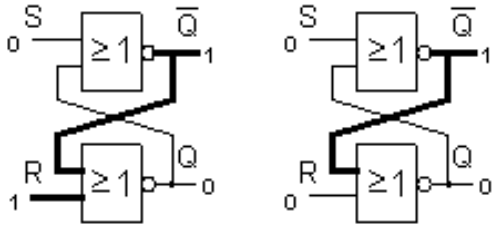
If S = 1 and R = 0 it causes the upper gate to "0". The lower gate inputs then becomes 00 and it's output Q = 1. Since the upper gate now get "1" from both inputs, it now does not matter if S = 0. Q remains locked to output "1".

If R = 1 and S = 0 it causes the lower gate to "0". Output is Q = 0. The upper gate inputs becomes 00 giving "1" at it's output and "1" at the input of the lower gate. Since the lower gate now get "1" from both inputs, it now does not matter if R = 0. Q remains unlocked to "0".

Q=1



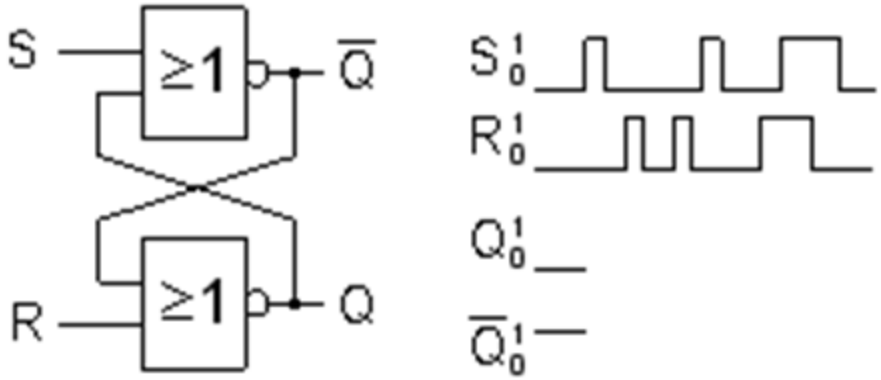
Q=0



William Sandqvist william@kth.se

Ex 9.1

Complete the timing diagram for the output signals Q and $\overline{Q}$.
The distance between the pulses is much longer than the gate delay.
(Hint, what is the locking input signal for NOR gates?)



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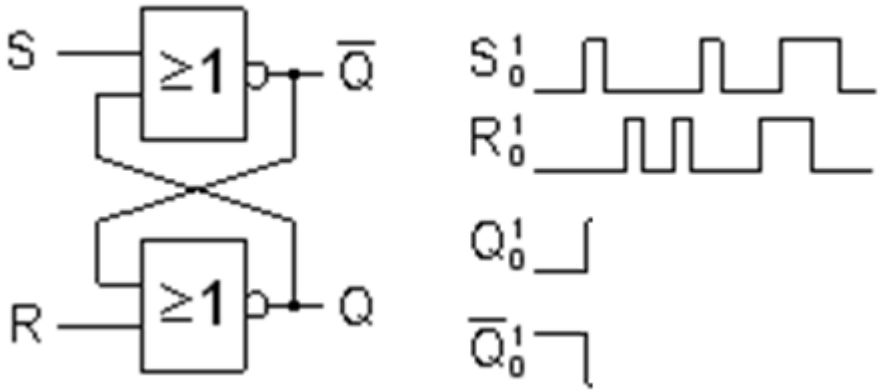

William Sandqvist william@kth.se

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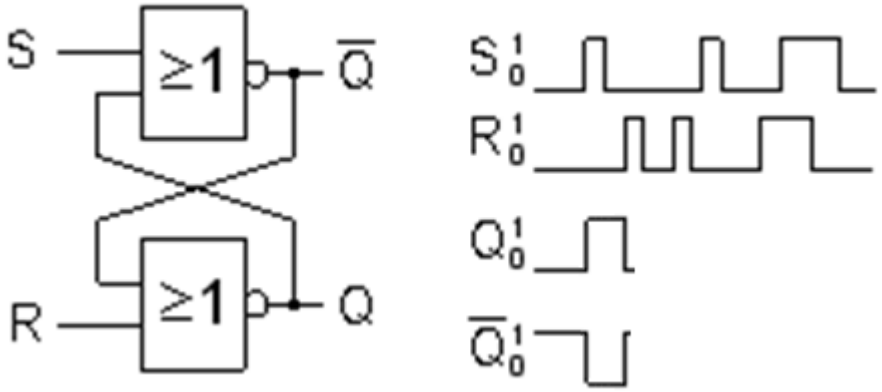

William Sandqvist william@kth.se

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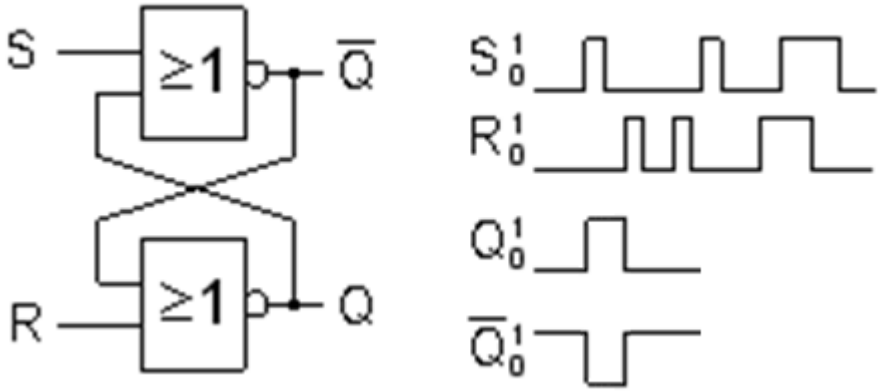

William Sandqvist william@kth.se

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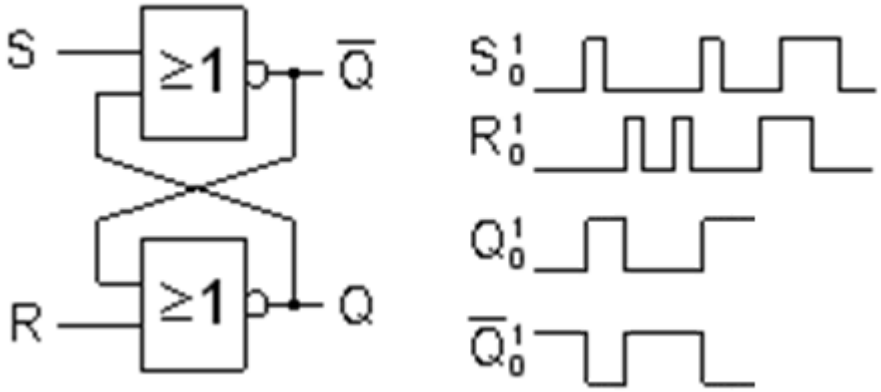

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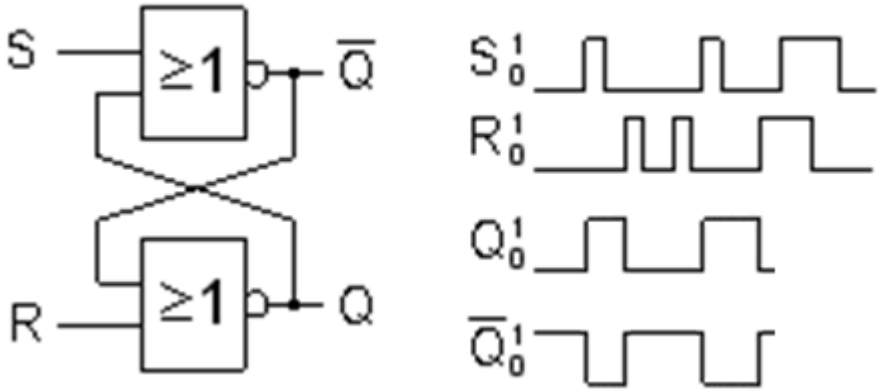

William Sandqvist william@kth.se

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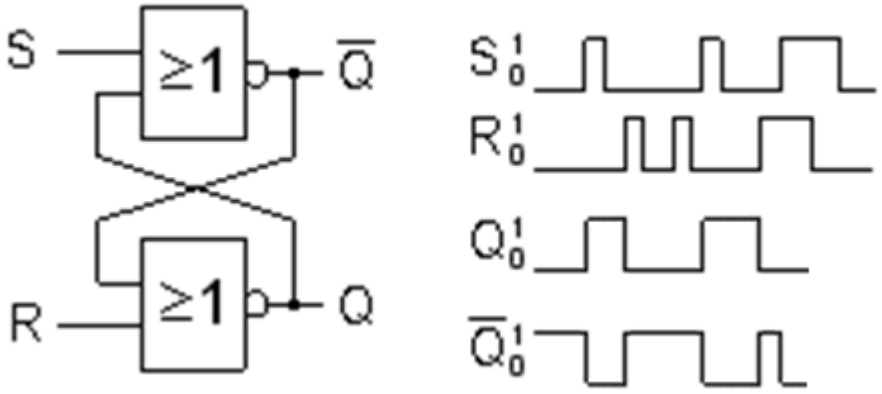

William Sandqvist william@kth.se

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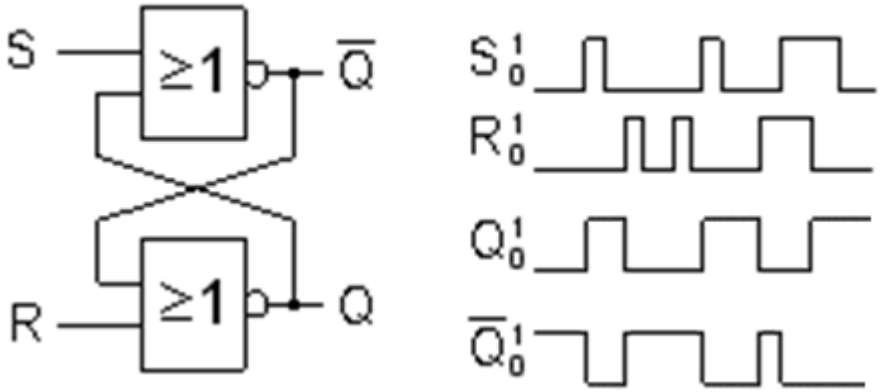

William Sandqvist william@kth.se

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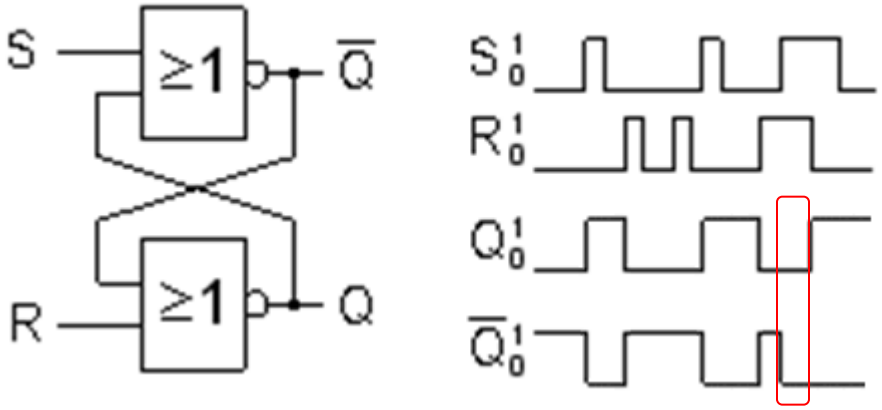
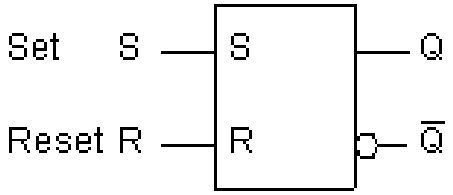


For S = 1 and R = 1 the latch does not work, the outputs will then not be each others inverses, but both will be 0.

William Sandqvist william@kth.se

SR-latch characteristic table



S	R	Q
0	0	Q_n same
0	1	0
1	0	1
1	1	?, forbidden

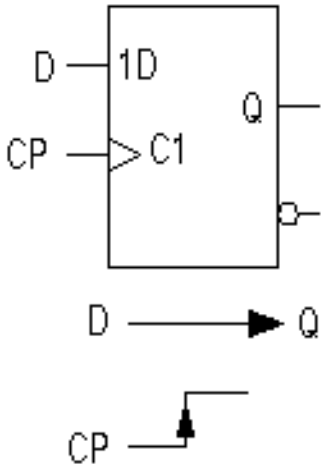
A short "pulse" S = 1 "sets" the latch circuit and a short "pulse" R = 1 "resets" it. As long as the S = 0 and R = 0, the latch retains its value

In the characteristic table the input combination S = 1 and R = 1 is forbidden!. For this combination would both gates outputs become "0" at the same time. For the other input combinations it applies that the outputs are each other's inverses. If you want to guarantee that the "other" output is always inverted, you have to "ban" the forbidden input signal combination.

Edge triggered Flip-flop

In digital technology there is a distinction between simple latches and clocked flip-flops. ? The limitation of the simple latch is that one can not enter a new value to the input while reading the output. The high speed of electronic circuits has made it necessary to develop more sophisticated circuits.

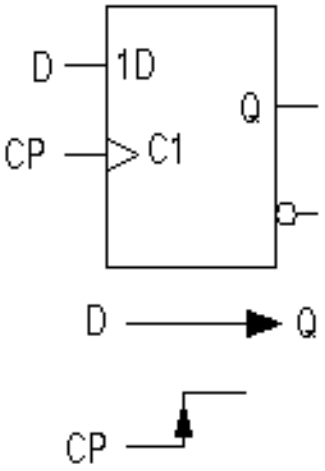
Edge-triggered D flip-flop. D input is the data input, C input is the clock pulse input, hence the designation CP. The control input C has an edge trigger sign, a triangle. When the C input is reached by a positive edge, ie. the short period of time when C goes from "0" to "1", the D-input value is copied to the output Q. The output value is then locked until a new edge of the clock pulse is received.



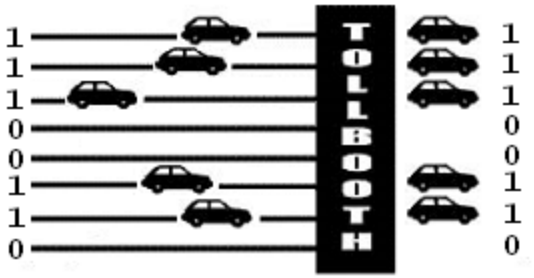
William Sandqvist william@kth.se

Synchronization with D flip-flops

- D flip-flop used to synchronize the signal flow between the different parts of the computer.



D flip-flops are used to stop the race between signals for the value to become stable. (Compare with the tollbooth that stops the cars).



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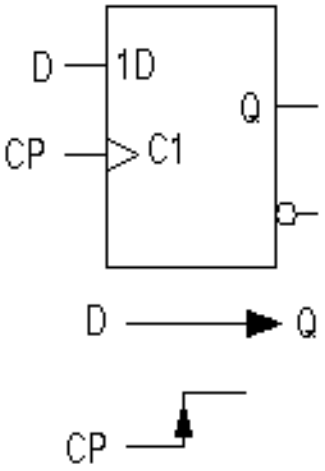

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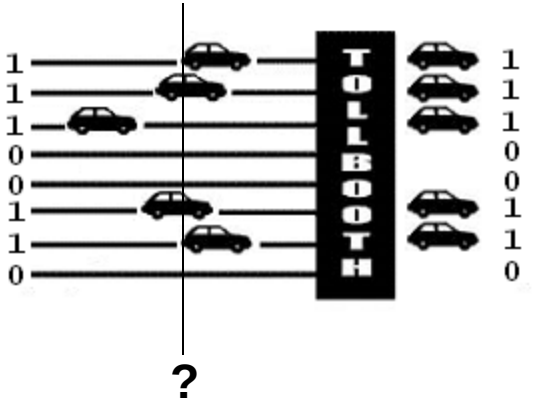

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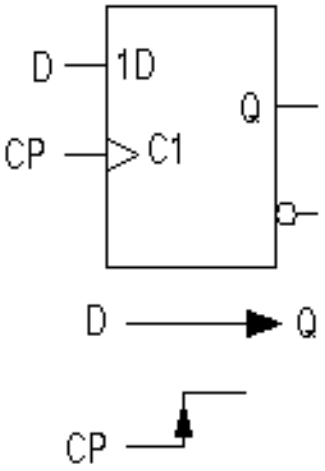

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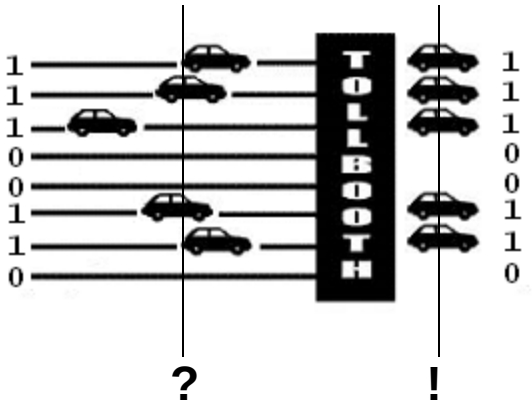
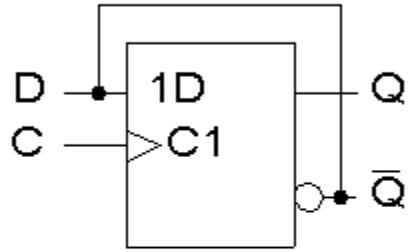


William Sandqvist william@kth.se

(9.4)

Draw output Q in this timing diagram



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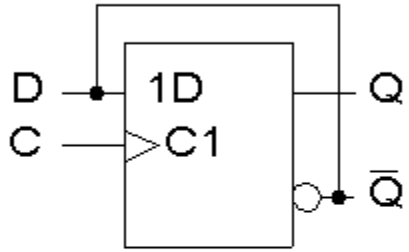
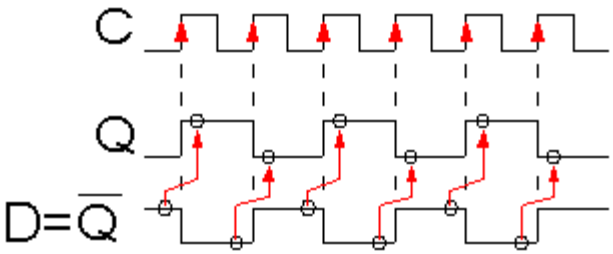
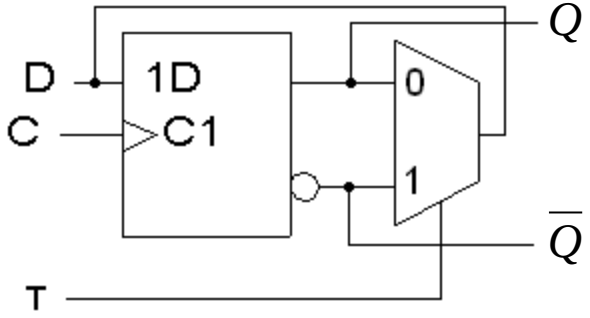




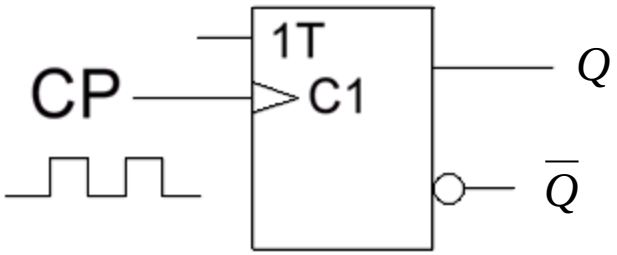
William Sandqvist william@kth.se

T-function

T=0 Same
T=1 Change, Toggle

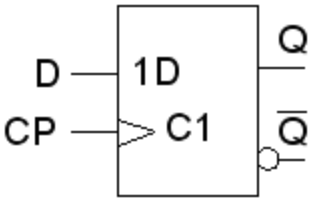


Sometimes this symbol of T-function is used.
The T-flip-flop.

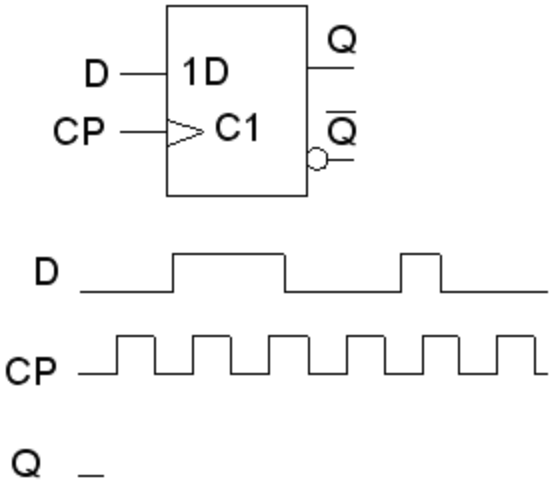


William Sandqvist william@kth.se

Ex 9.3



Draw the timing diagram for the output Q of the D flip-flop.



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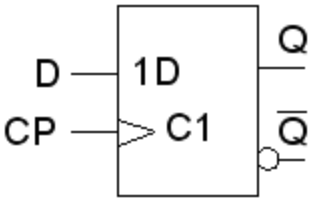

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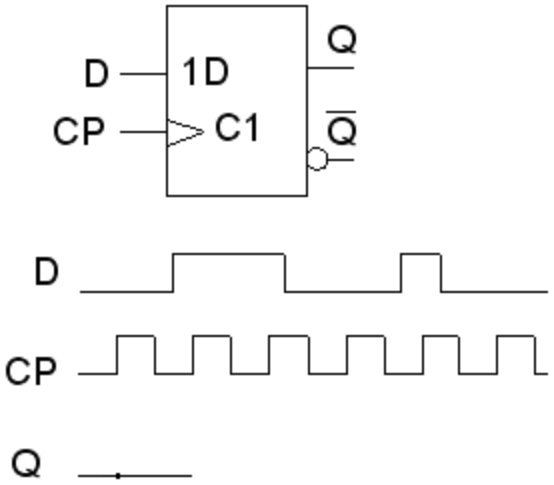

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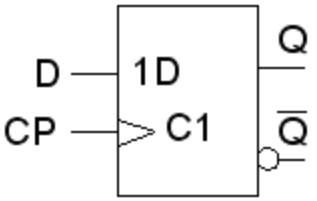

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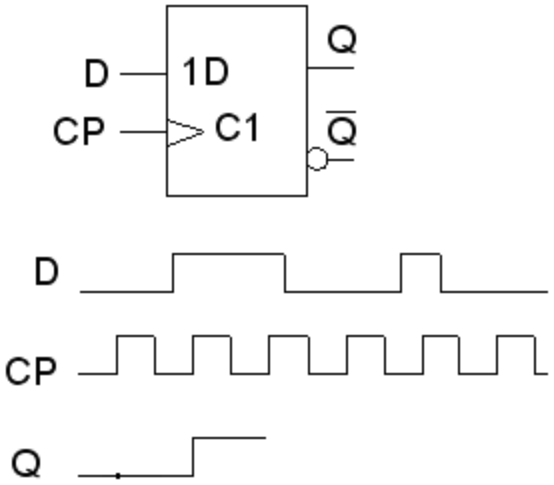

William Sandqvist william@kth.se

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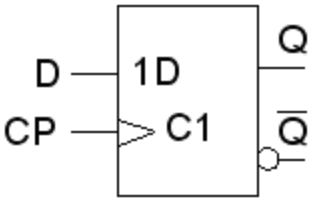

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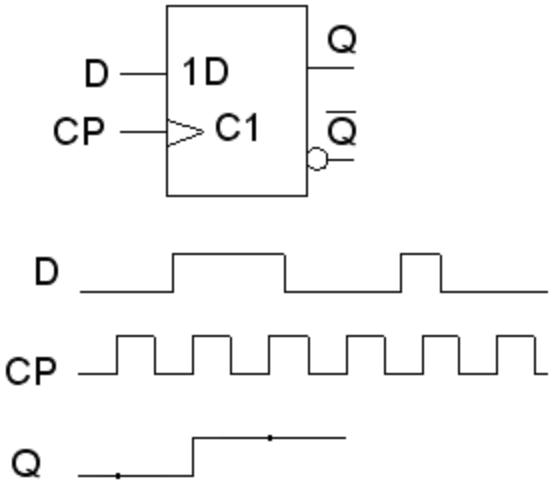

William Sandqvist william@kth.se

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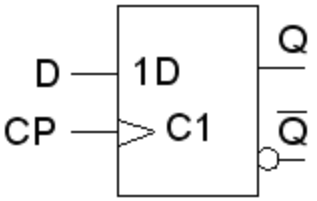

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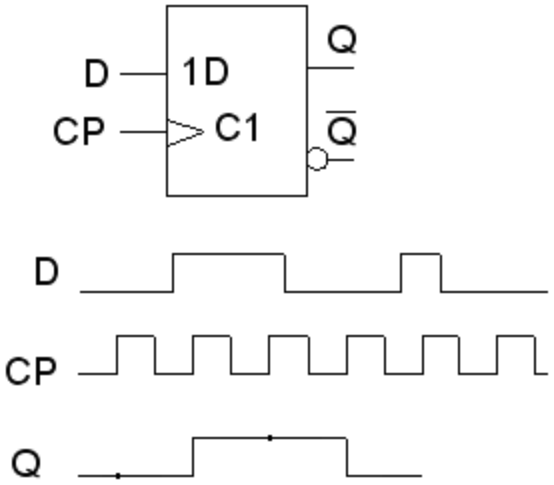

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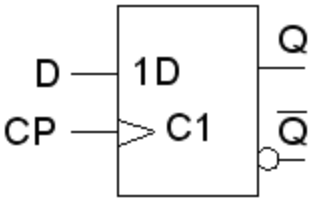

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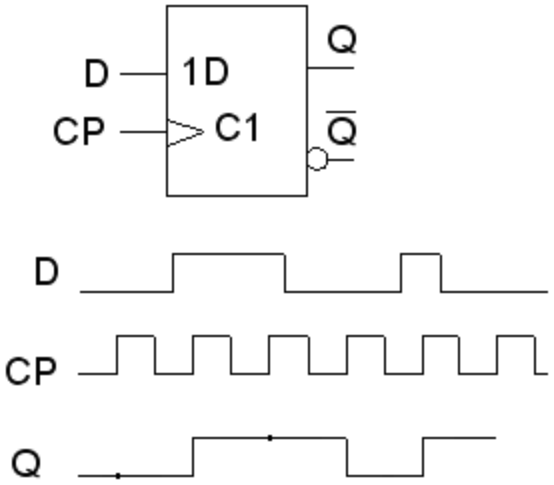

William Sandqvist william@kth.se

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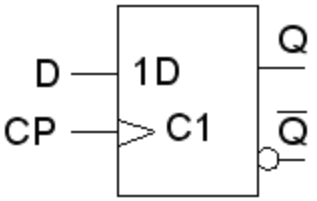

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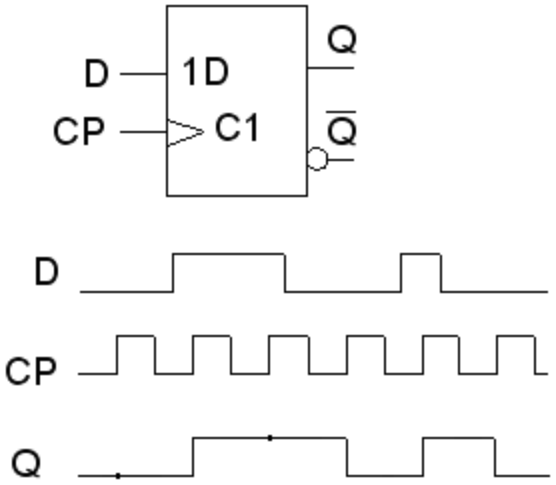
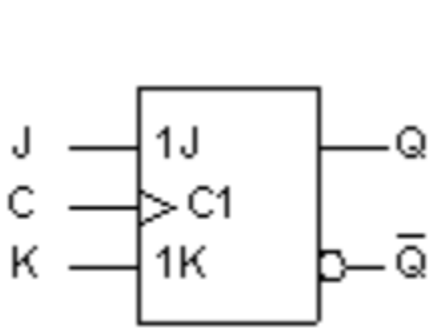


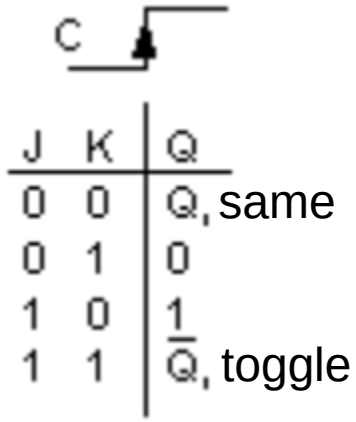
William Sandqvist william@kth.se

Ex 9.5

JK flip-flop was an older type of "universal flip-flop". Show how it can be used as the T-flip-flop and as D-flip-flop.



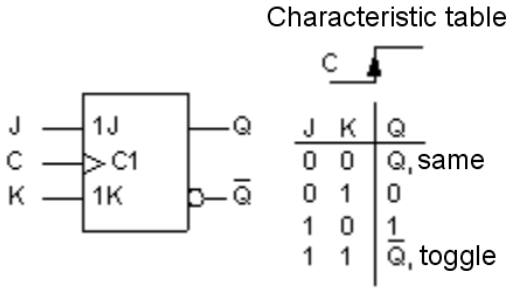
Characteristic table

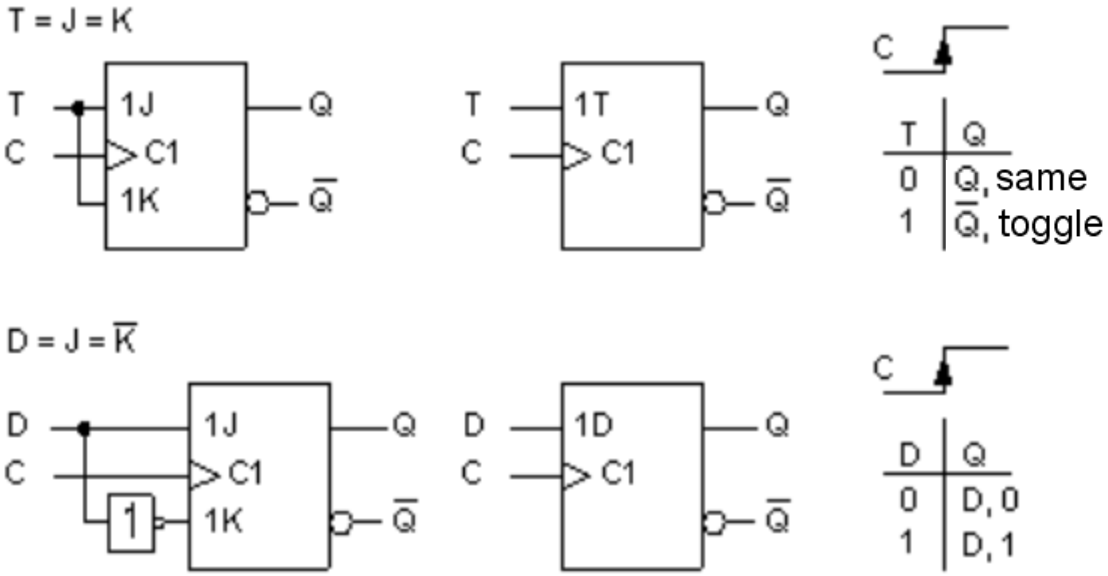


J	K	Q
0	0	Q, same
0	1	0
1	0	1
1	1	$\overline{Q}$, toggle

William Sandqvist william@kth.se

Ex 9.5

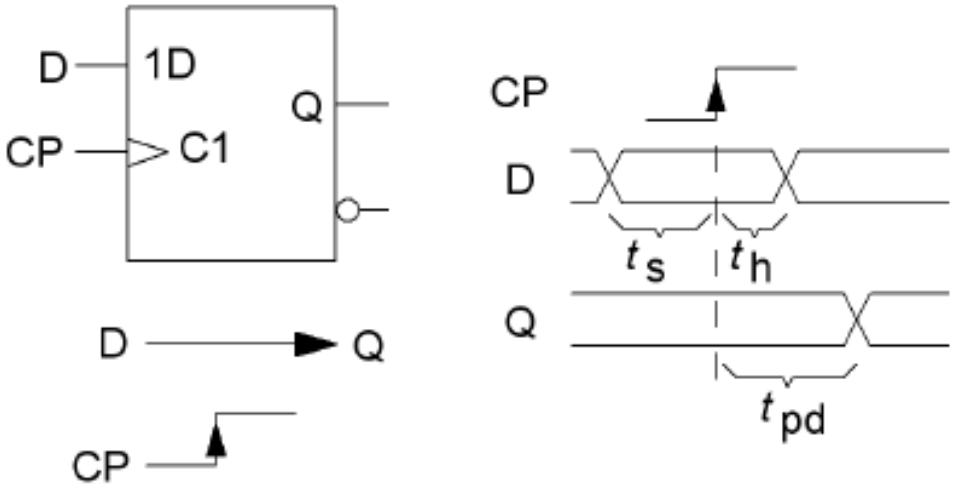




JK flip-flop can be used as the T flip-flop or D flip-flop. (When flip-flops are connected to each other there are usually the inverted outputs available, you will then not require the inverter to make the JK flip flop to D flip-flop.)

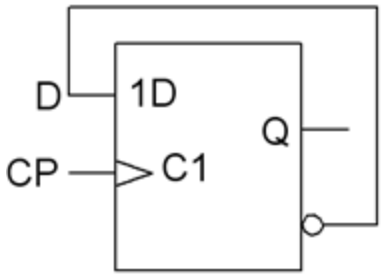
William Sandqvist william@kth.se

Ex 9.6



What is the maximum clock frequency that can be used to the circuit in the figure without the risk of failure?
Suppose that

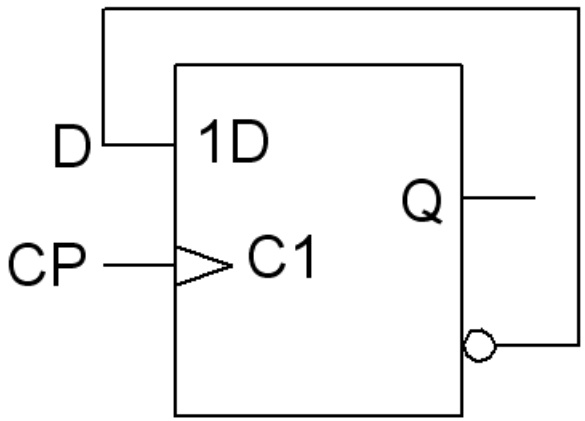
t_s = 20 ns t_h = 5 ns t_{pd} = 30 ns

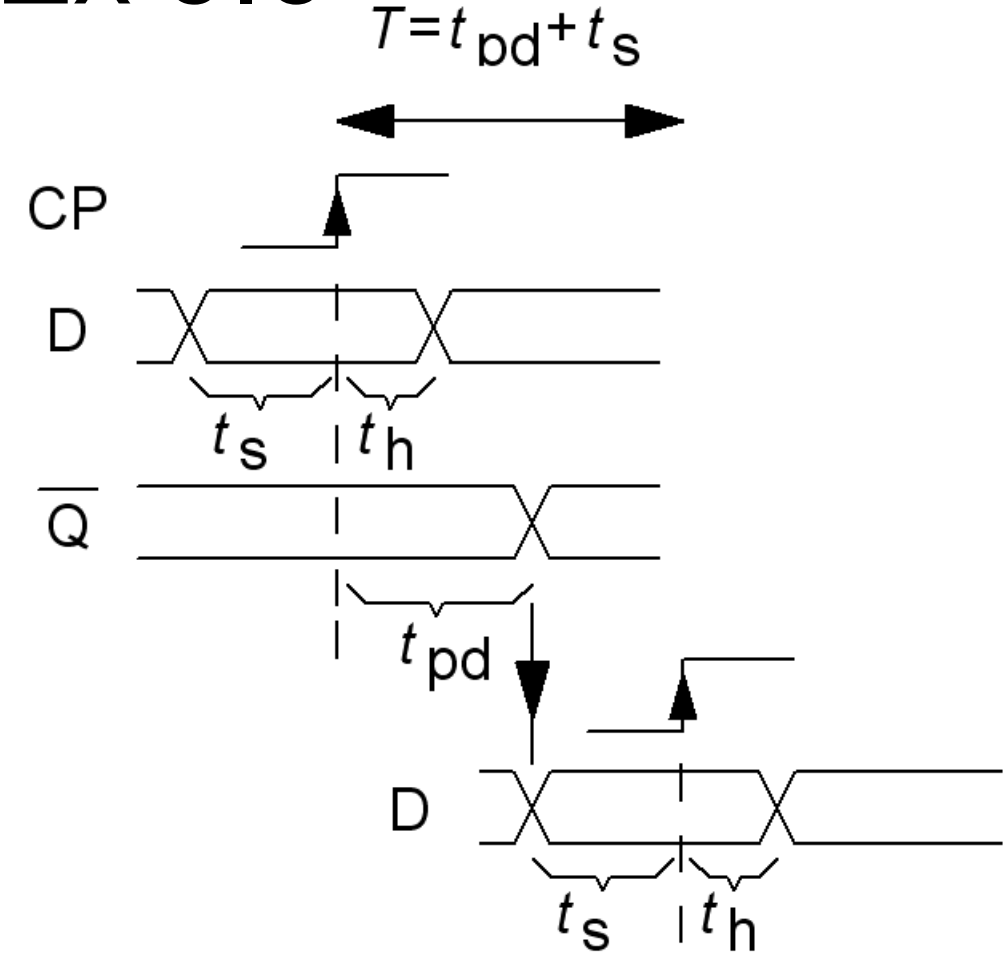


William Sandqvist william@kth.se

Ex 9.6

t_s = 20 ns t_h = 5 ns t_{pd} = 30 ns

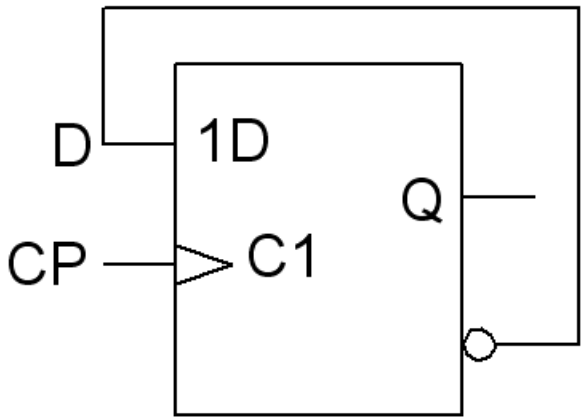


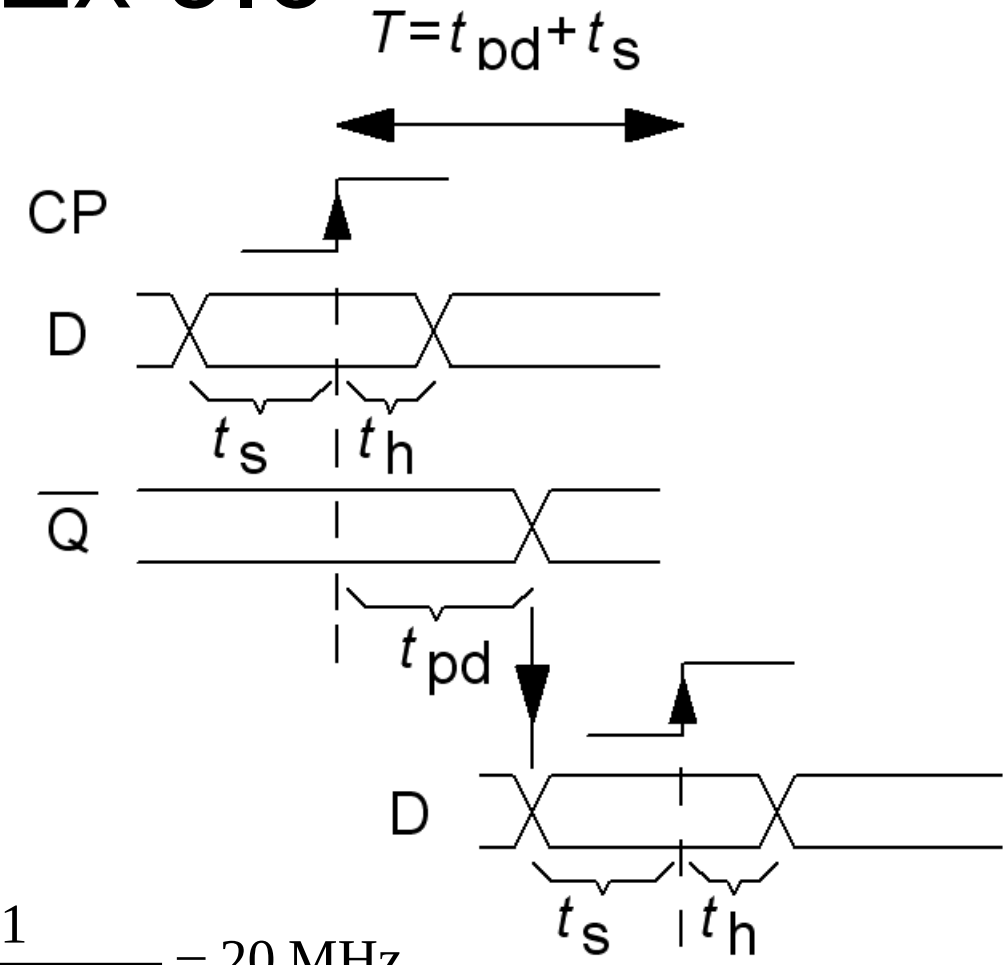


William Sandqvist william@kth.se

Ex 9.6

t_s = 20 ns t_h = 5 ns t_{pd} = 30 ns





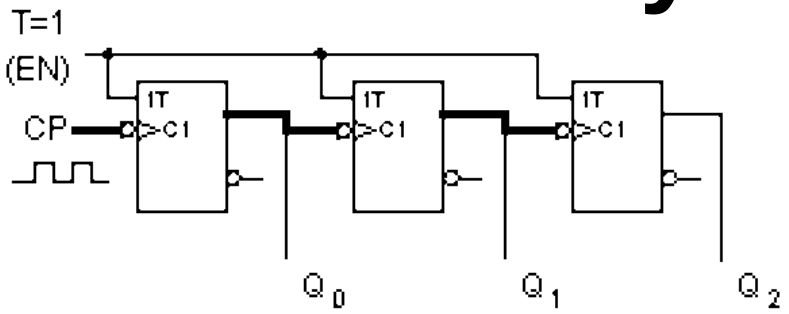
$$T = t_{pd} + t_s$$

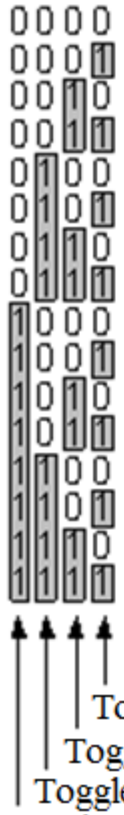
$$f = \frac{1}{T} = \frac{1}{t_{pd} + t_s} = \frac{1}{(20+30)\,[\text{ns}]} = 20\ \text{MHz}$$

William Sandqvist william@kth.se

William Sandqvist william@kth.se

Asynchronous binary counter





The figure above shows a binary counter with three flip-flops, the counting cycle has eight states so it is a modulo-8 counter. The counter is built of T-flip-flops, as they all have T = 1 they "toggles" at each clock pulse. The first flip-flop Q_0 "toggles" every clock pulse. The flip-flop Q_1 is clocked by the first flip-flop. It will therefore only "toggle" for every other clock pulse. The third flip-flop Q_2 will "toggle" for every other every other clock pulse.

According to the binary table, the counter is counting in binary code. ($Q_2Q_1Q_0$: 000 001 010 011 100 101 110 111 000 ...).

William Sandqvist william@kth.se

Asynchronous counter weakness

Asynchronous counter has the simplest possible structure. Since the clock pulses are routed through the flip-flops so they can not change state on exactly the same time. If you read the binary code on the outputs of flip-flops during the transition, then “any” code can appear for a short time!

The flip-flops changes output one after another and you could say that the clock pulse "ripples" through the flip-flops (asynchronous counters are therefore sometimes called **ripple counters**).

This problem has been solved with the **synchronous counters**.

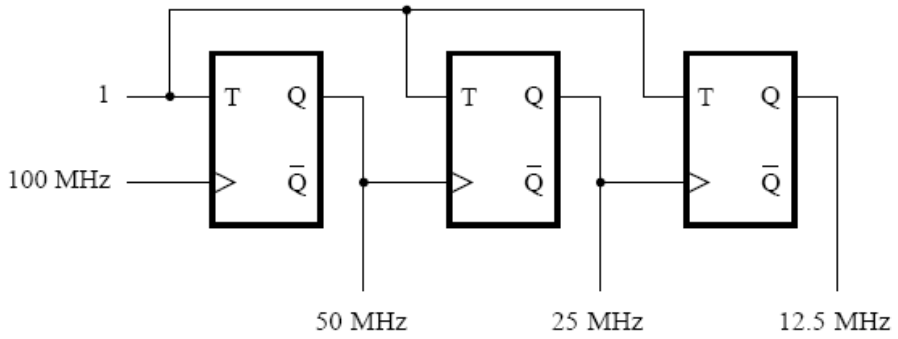
BV 7.5

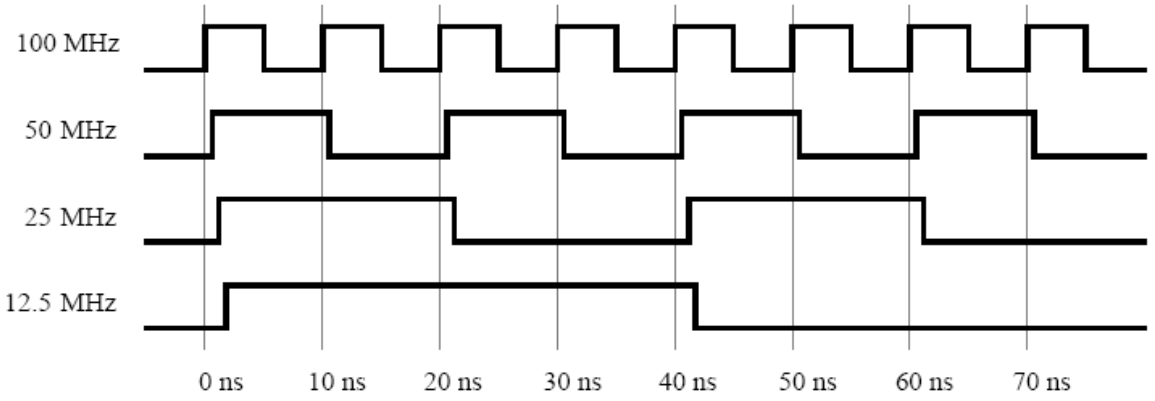
Given a 100-MHz clock signal, derive a circuit using T flip-flops to generate 50-MHz and 25-MHz clock signals. Draw a timing diagram for all three clock signals, assuming resonable delays.

William Sandqvist william@kth.se

BV 7.5

Given a 100-MHz clock signal, derive a circuit using T flip-flops to generate 50-MHz and 25-MHz clock signals. Draw a timing diagram for all three clock signals, assuming resonable delays.

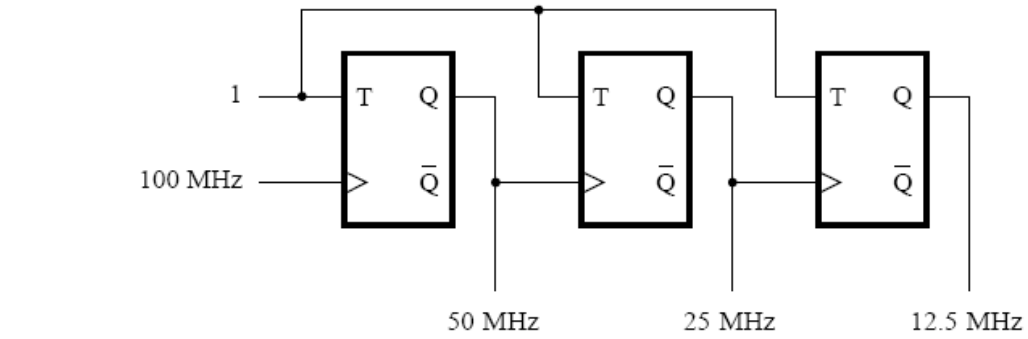


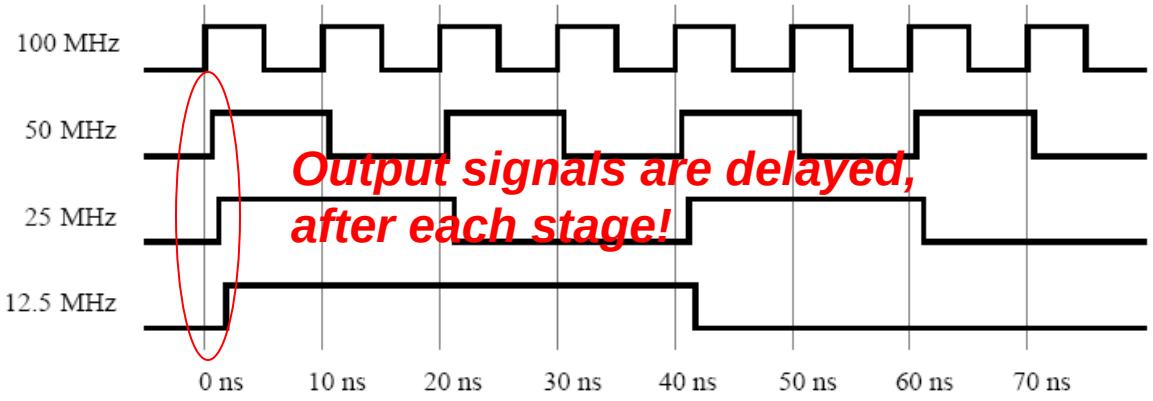


William Sandqvist william@kth.se

BV 7.5

Given a 100-MHz clock signal, derive a circuit using T flip-flops to generate 50-MHz and 25-MHz clock signals. Draw a timing diagram for all three clock signals, assuming resonable delays.

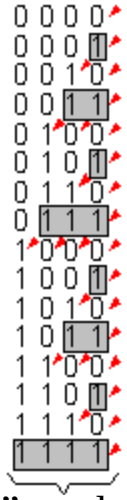




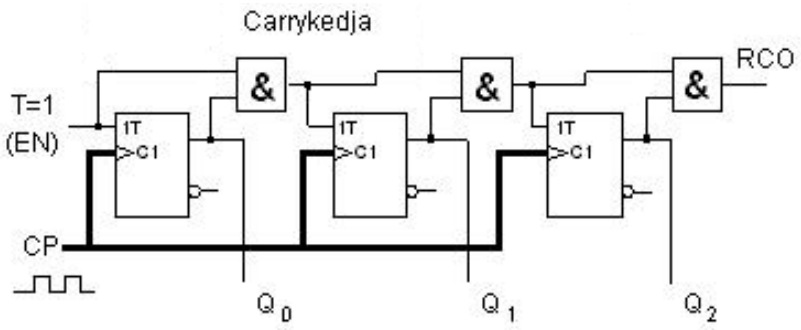
William Sandqvist william@kth.se

Synchronous binary-counter

The clock pulses go directly to all the flip-flops and therefore they change state at the same time. What flip-flop to turn on or not is controlled by T-inputs. The first flip-flop has T = 1, and it will toggle on every clock pulse. From the binary table, one can see that a certain flip-flop should toggle is when all previous flip-flops outputs "1".



”toggle” when all previous are 1



You get this condition from the AND gates in the so-called Carry-chain and they control the T-inputs. If you want to expand the counter it is done with one flip-flop and one AND gate per stage (bit).

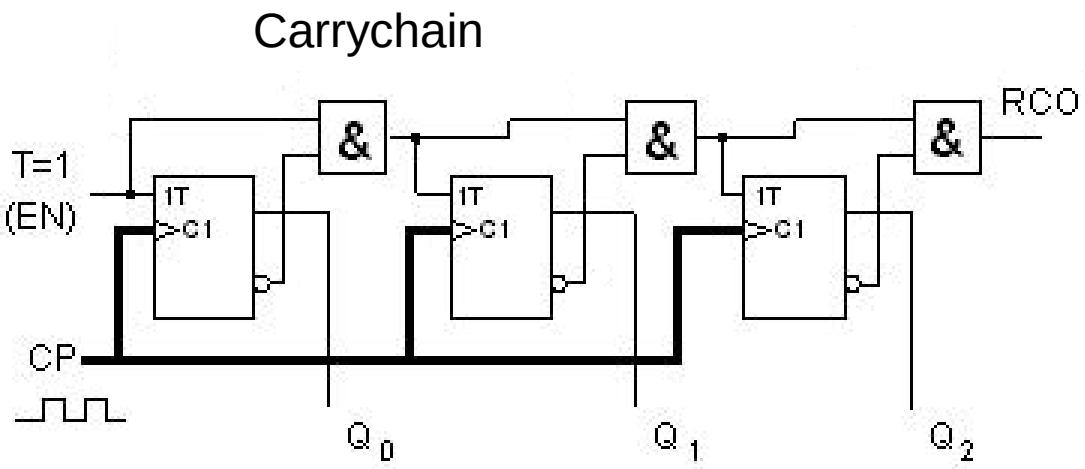
Up: *Toggle if all previous are 1*

William Sandqvist william@kth.se

Synchronous down-counter

1111
1110
1101
1100
1011
1010
1001
1000
0111
0110
0101
0100
0011
0010
0001
0000

”toggle” when all previous are 0

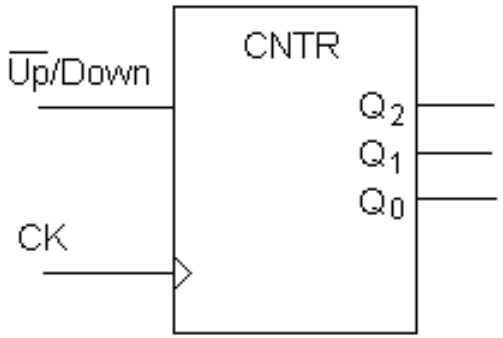


Down: *Toggle if all previous are 0*

William Sandqvist william@kth.se

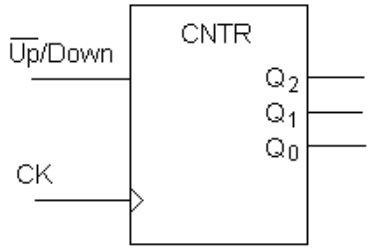
BV 7.16

Design a three-bit up/down counter using T flip-flops. It should include a control input called UP/Down. If UP/Down = 0, then the circuit should behave as an up-counter. If UP/Down = 1, then the circuit should behave as a down –counter.

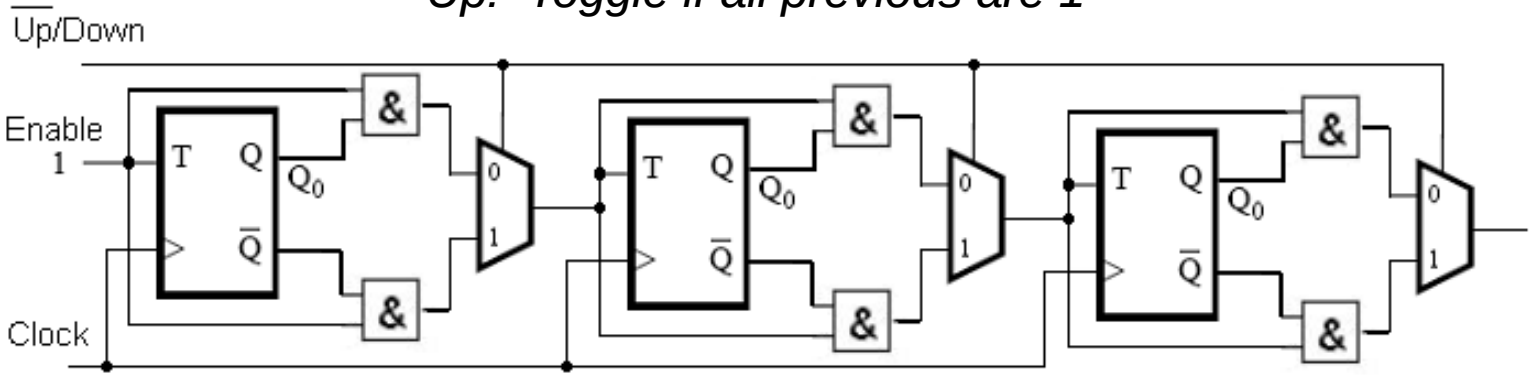


William Sandqvist william@kth.se

BV 7.16



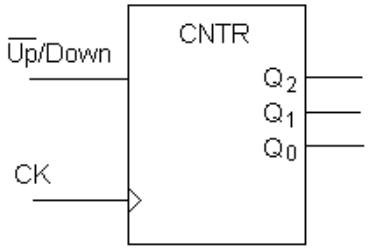
Up: Toggle if all previous are 1



Down: Toggle if all previous are 0

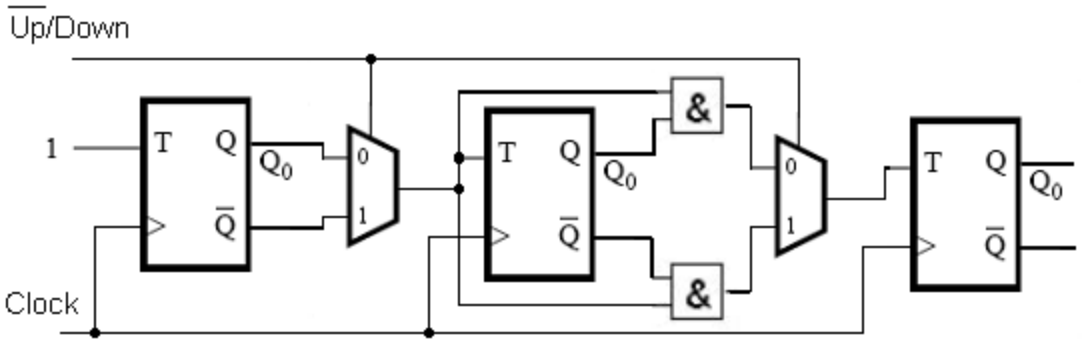
William Sandqvist william@kth.se

BV 7.16



- There is no requirement that the counter will be expanded with more bits.
- There is no requirement that the counter can be enabled.

The circuit can be simplified :

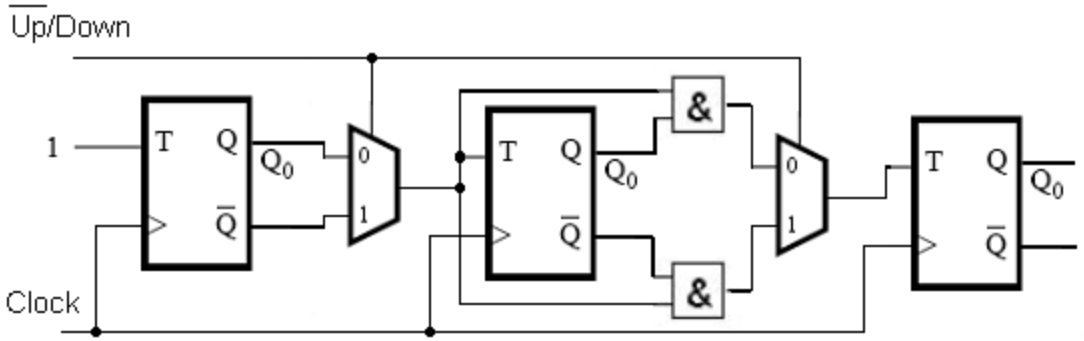


William Sandqvist william@kth.se

BV 7.17

Repeat problem 7.16 using D flip-flops.

T:

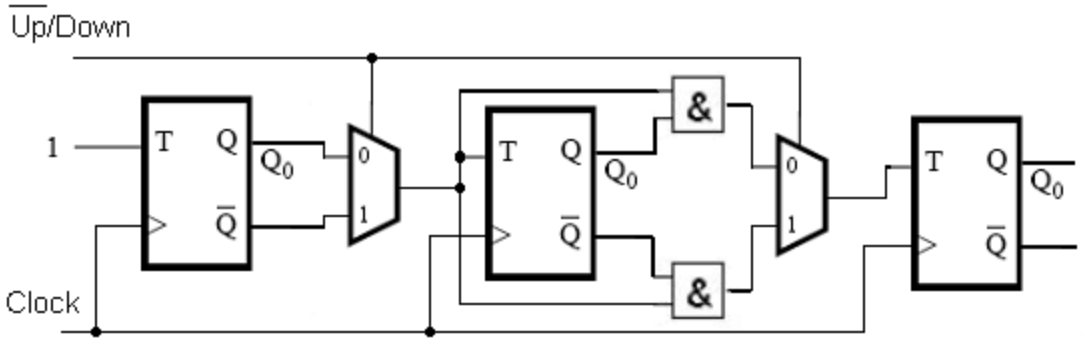


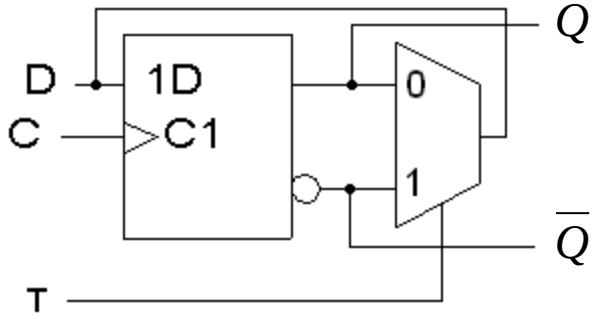
William Sandqvist william@kth.se

BV 7.17

Repeat problem 7.16 using D flip-flops.

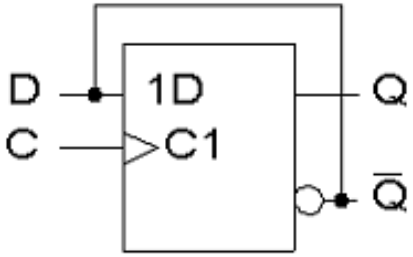
T:



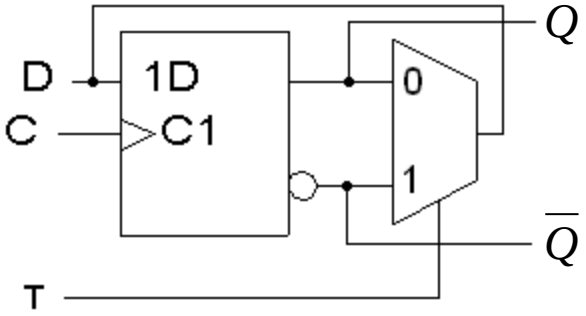


William Sandqvist william@kth.se

BV 7.17

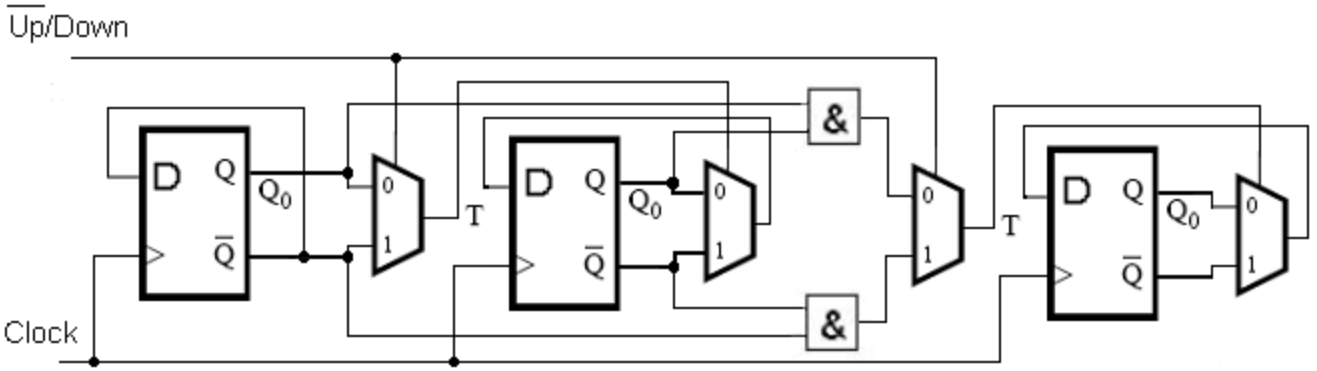


Toggle

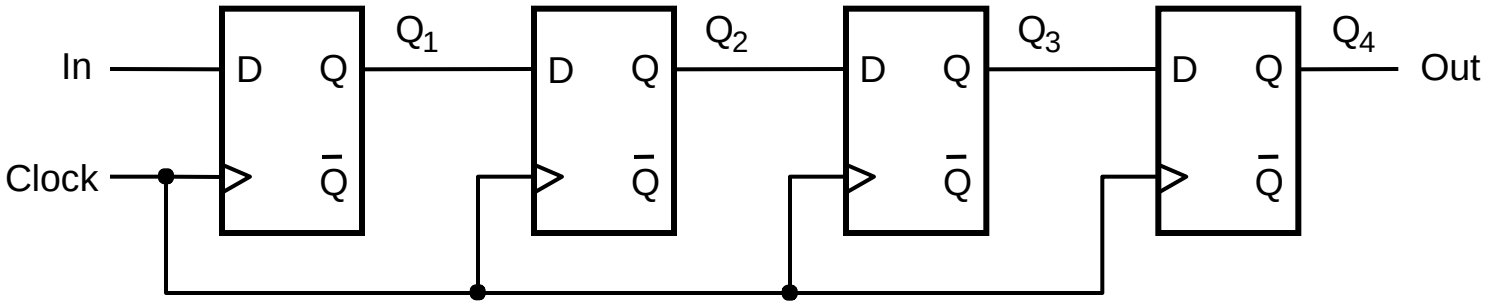


T: Hold/Toggle

D:



William Sandqvist william@kth.se



(a) Circuit

A shift-register with a typical sequence.

	In	Q_1	Q_2	Q_3	Q_4 = Out
t_0	1	0	0	0	0
t_1	0	1	0	0	0
t_2	1	0	1	0	0
t_3	1	1	0	1	0
t_4	1	1	1	0	1
t_5	0	1	1	1	0
t_6	0	0	1	1	1
t_7	0	0	0	1	1

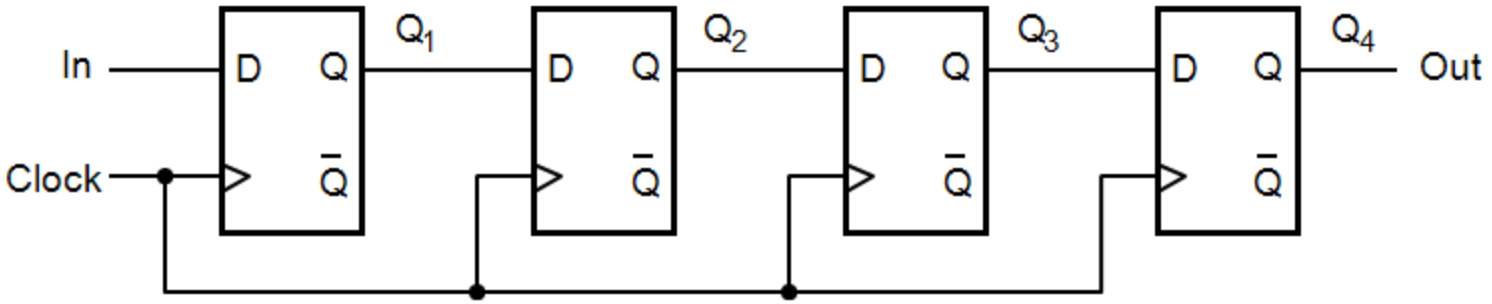
(b) A sample sequence

Figure 7.18. A simple shift register.

BV 7.13

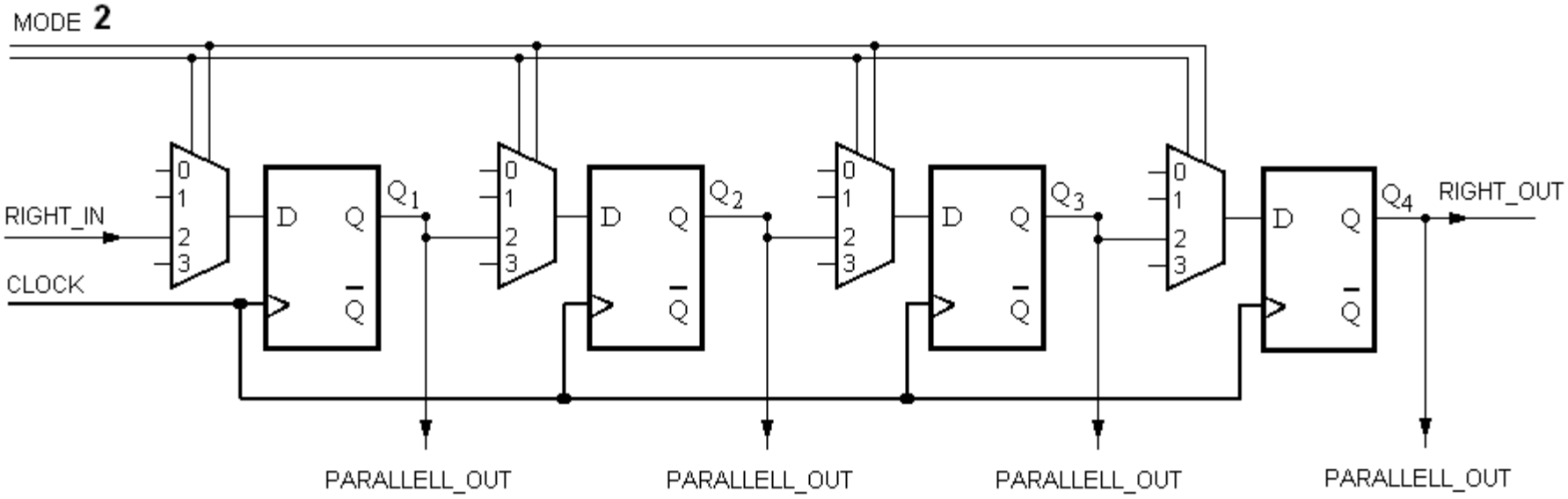
A universal shift register can shift in both the left-to-right and right-to-left directions, and it has parallell-load capability. Draw a circuit for such a shift register.

This is what a normal right shifting shift register looks like :



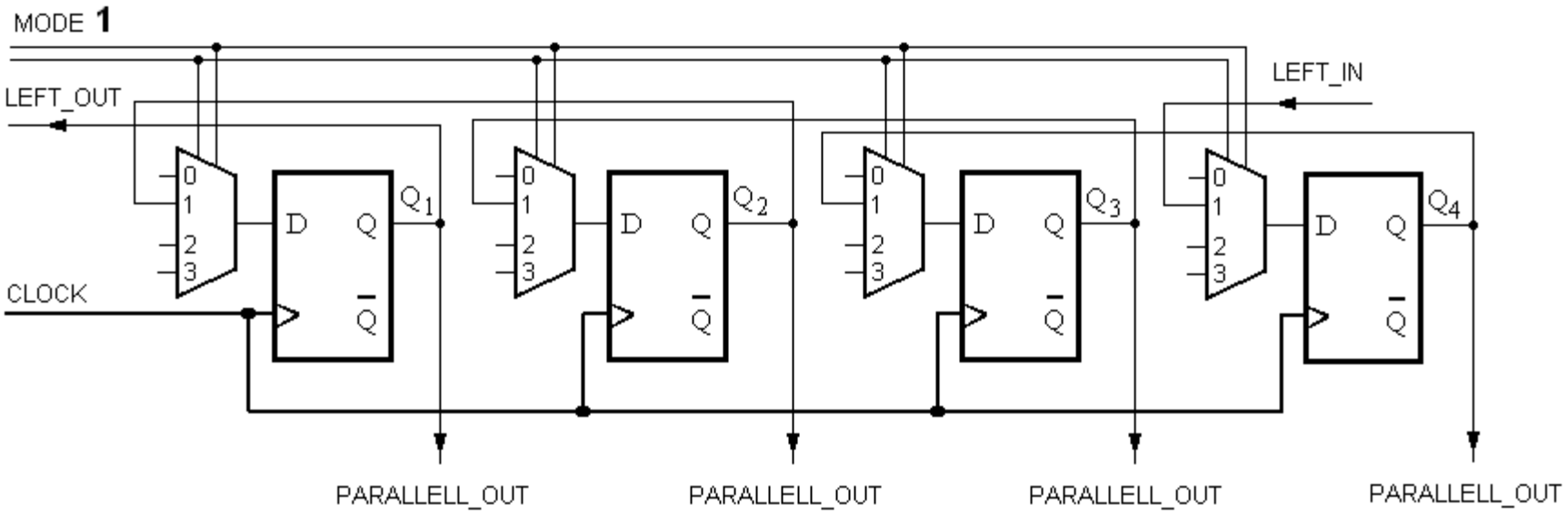
William Sandqvist william@kth.se

Mode = 2 Right shift



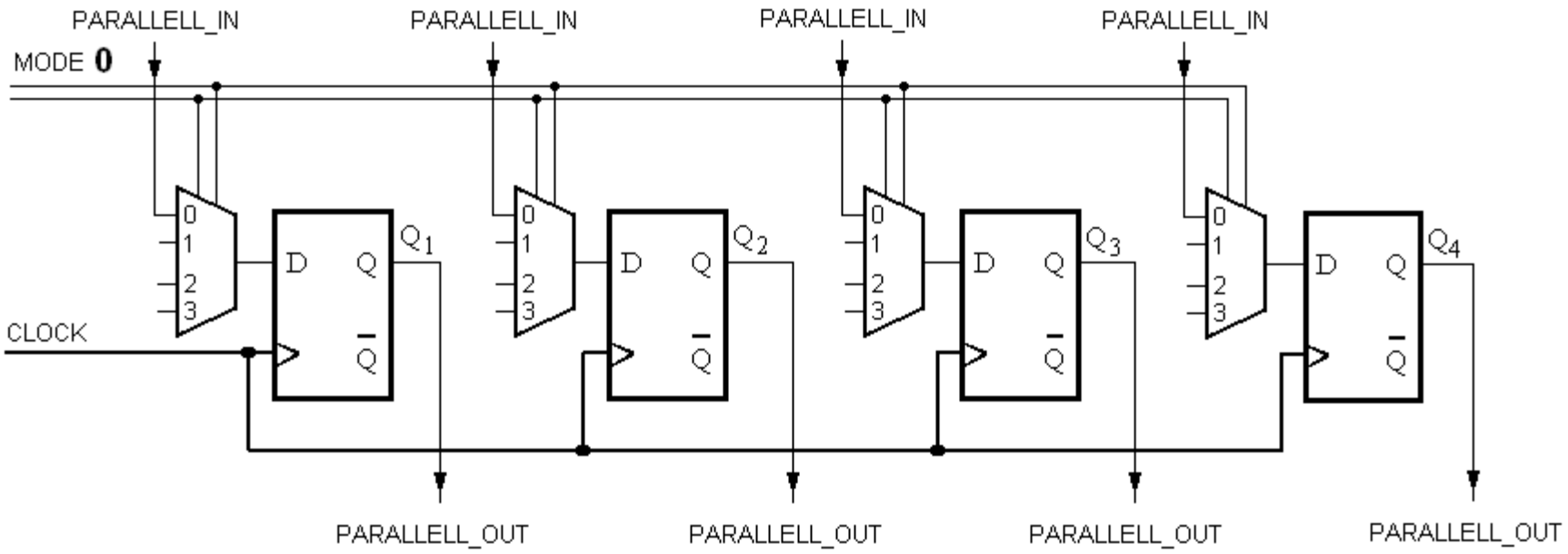
William Sandqvist william@kth.se

Mode = 1 Left Shift



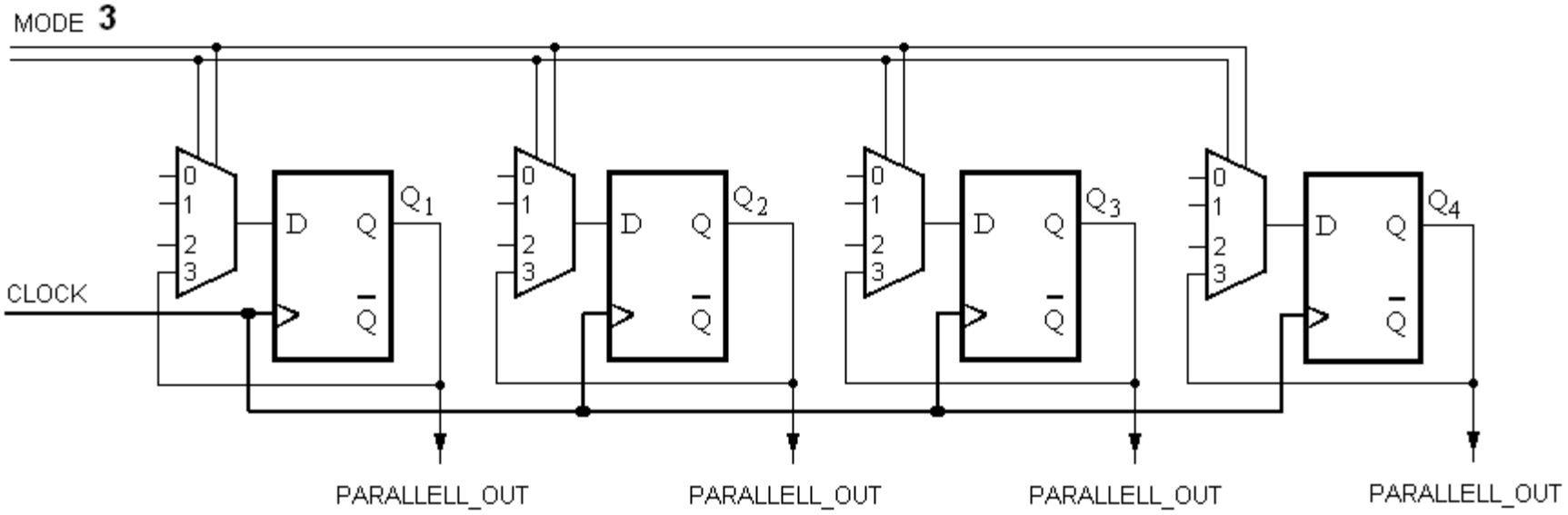
William Sandqvist william@kth.se

Mode = 0 Parallell Load



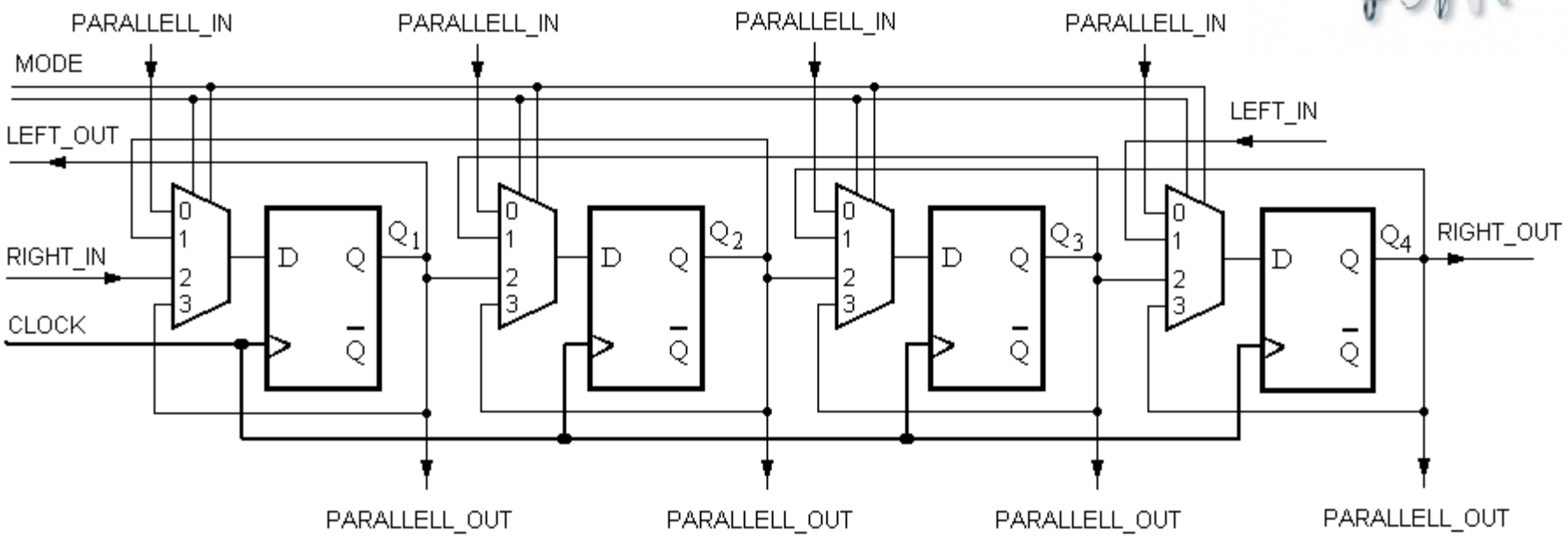
William Sandqvist william@kth.se

Mode = 3 Hold



William Sandqvist william@kth.se

Multifunction shiftregister



Mode **0** Parallell Load Mode **1** Left Shift
Mode **2** Right Shift Mode **3** Hold

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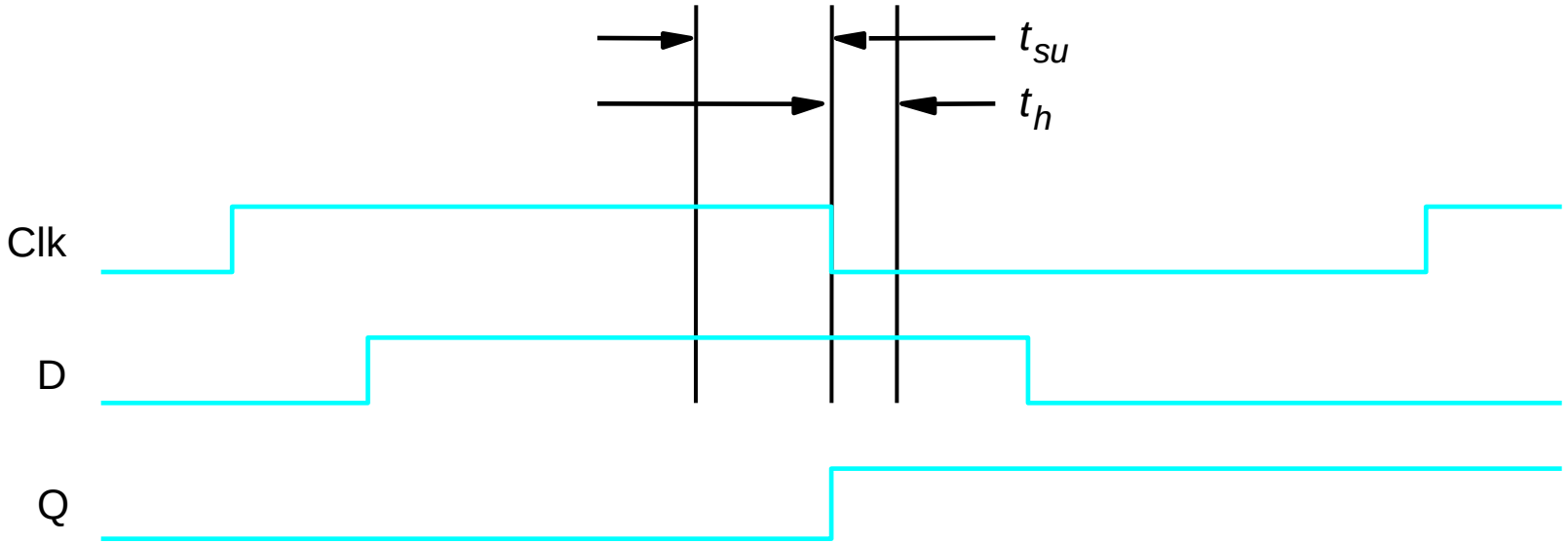


Figure 7.9. Setup and hold times.

BV 7.24

For the flip-flops in the counter in Figure 7.25, assume that t_{su} = 3 ns, t_h = 1ns and the propagation delay t_{pd} is 1ns, and the gates and the 2-to-1 multiplexer has the propagation delay t_{pd} equal to 1ns.

What is the maximum clock frequency for which the circuit will operate correctly?

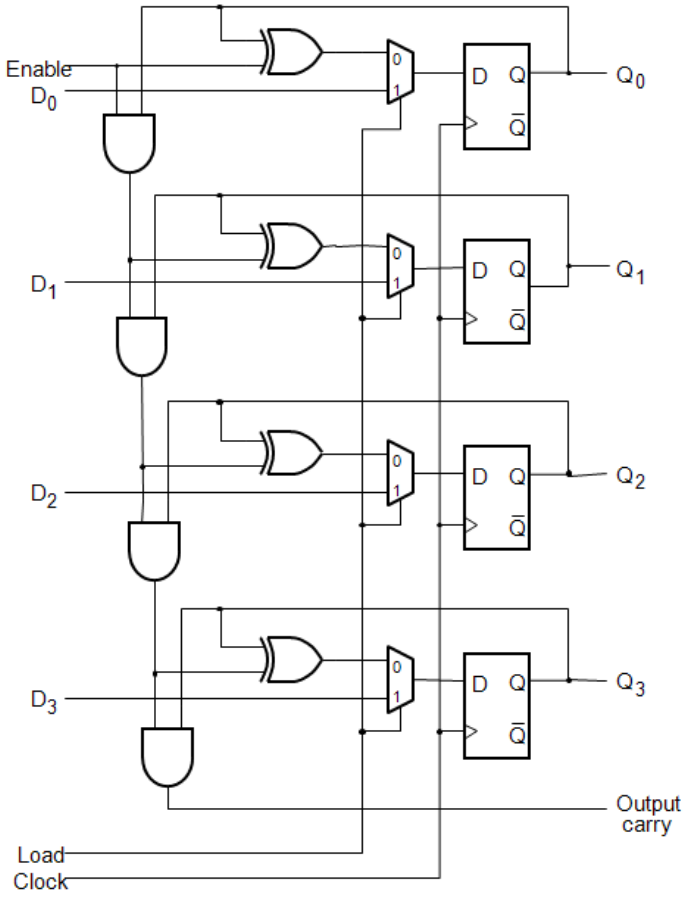


Figure 7.25. A counter with parallel-load capability.

BV 7.24

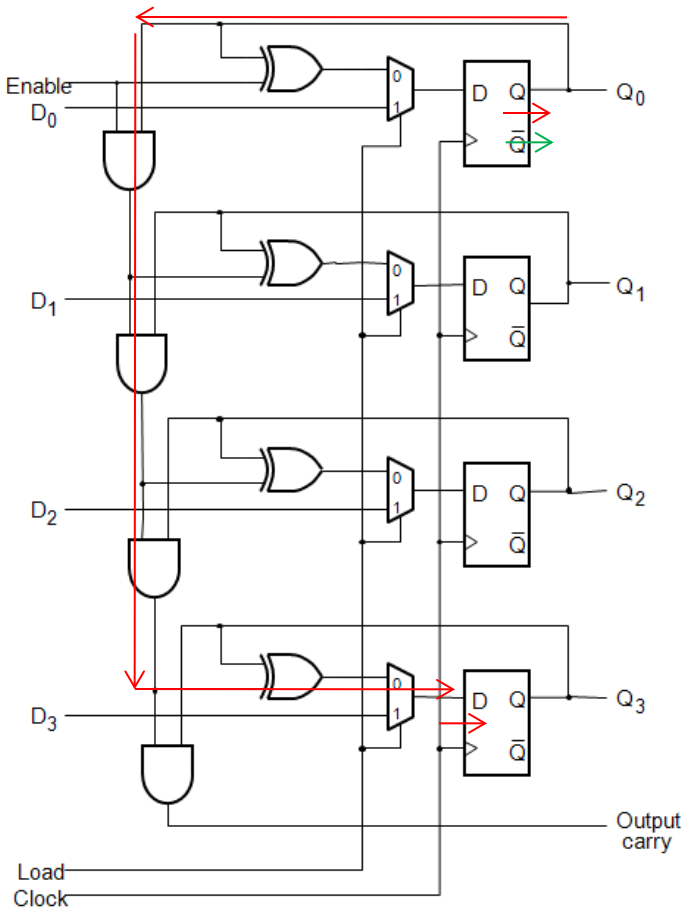


Figure 7.25. A counter with parallel-load capability.

The signal starts at flip-flop 0 after t_{pd} and passes 3 AND-gates, 1 XOR-gate and 1 MUX on its way to flip-flop 3. The flip-flops has demands on that the D signal must have been stable t_{su} before the clock-pulse.
The D-signal also must be continnue to be stable during t_h.

$$t_h < t_{pd} + 3 \cdot t_{AND} + t_{XOR} + t_{MUX}$$

Check!

$$T_{\min} = t_{pd} + 3 \cdot t_{AND} + t_{XOR} + t_{MUX} + t_{SU} =$$

$$= 1 + 3 + 1 + 1 + 3 = 9 \text{ ns}$$

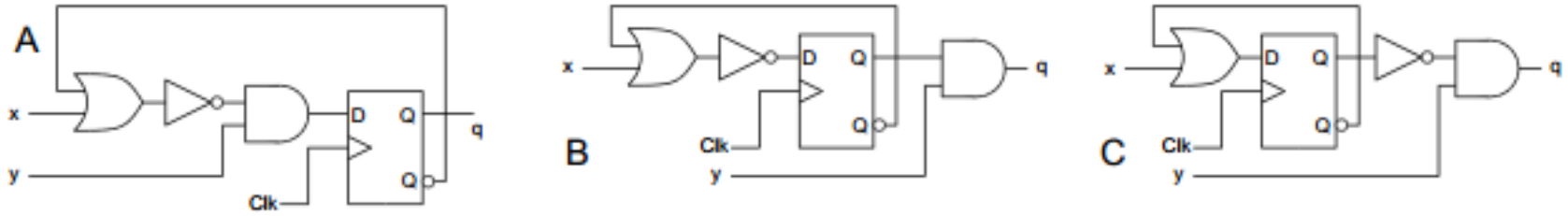
$$f = \frac{1}{T_{\min}} = \frac{1}{9\,[\text{ns}]} = 111 \text{ MHz}$$

William Sandqvist william@kth.se

(Ex. 9.7)

•The figure shows three different state machines. Specify the state machine (A, B or C) that can operate at the highest clock speed. Highlight the critical path (the path that limits clock frequency) in this figure and calculate the period time for the clock signal Clk.

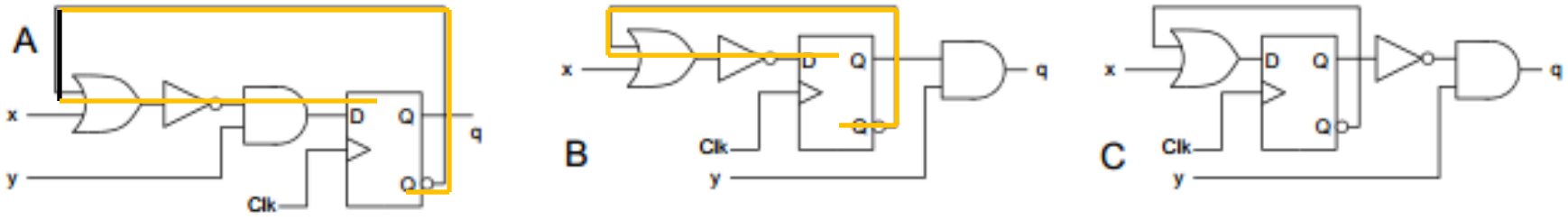
$t_{AND} = 0{,}4$ ns, $t_{OR} = 0{,}4$ ns, $t_{NOT} = 0{,}1$ ns, $t_{setup} = 0.3$ ns, $t_{dq} = 0{,}4$ns



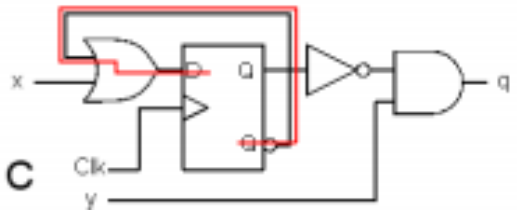
William Sandqvist william@kth.se

(Ex. 9.7)

$t_{AND} = 0{,}4$ ns, $t_{OR} = 0{,}4$ ns, $t_{NOT} = 0{,}1$ ns, $t_{setup} = 0.3$ ns, $t_{dq} = 0{,}4$ns



$$T = T_{OR} + T_{setup} + T_{dq} = 0{,}4 + 0{,}3 + 0{,}4 = 1{,}1 \text{ ns}$$



William Sandqvist william@kth.se

Heuristic methods of construction?

This time, we have constructed counters and shift registers by being "clever". (Heuristic methods of construction - based on experience)

It's not every day one is so slick, so the next exercise is about the systematic design methods that are general and therefore can be used on any sequence circuit problem, and all days.

- The Moore machine and the Mealy machine.