KTH Informations- och kommunikationsteknik

Written exam for
IE1204/5 Digital Design
Thursday 15/1 2015 9.00-13.00

General Information

Examiner: Ingo Sander.

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Exam text does not have to be returned when you hand in your writing.

Aids: No aids are allowed!
The exam consists of three parts with a total of 12 tasks, and a total of 30 points:

Part A1 (Analysis) contains eight short questions. Right answer will for six of the questions give you one point and for two of the questions one or two points. Incorrect answer will give you zero points. The total number of points in Part A1 **is 10 points**. To **pass the Part A1 requires at least 6p**, *if fewer points we will not look at the rest of your exam.*

Part A2 (Methods) contains two method problems on a total of 10 points.

To **pass the exam** requires at least **11 points** from A1 + A2 , *if fewer points we will not look at the rest of your exam.*

Part B (Design problems) contains two design problems of a total of 10 points. Part B is corrected only if there are at **least 11p** from the exam A- Part.

NOTE ! At the end of the exam text there is a submission sheet for Part A1 , which can be separated to be submitted together with the solutions for A2 and B.

For a passing grade (**E**) requires at **least 11 points on the exam**.

Grades are given as follows:

0 –	11 –	16 –	19 –	22 –	25
F	E	D	C	B	A

The result is expected to be announced before Thursday 5/2 2015.

Part A1: Analysis

Only answers are needed in Part A1. Write the answers on the submission sheet for Part A1, which can be found at the end of the exam text.

1. 1p/0p
A function $f(x, y, z)$ is described by the equation:

$$f(x, y, z) = x\overline{y} + \overline{y}z + yz + xy$$

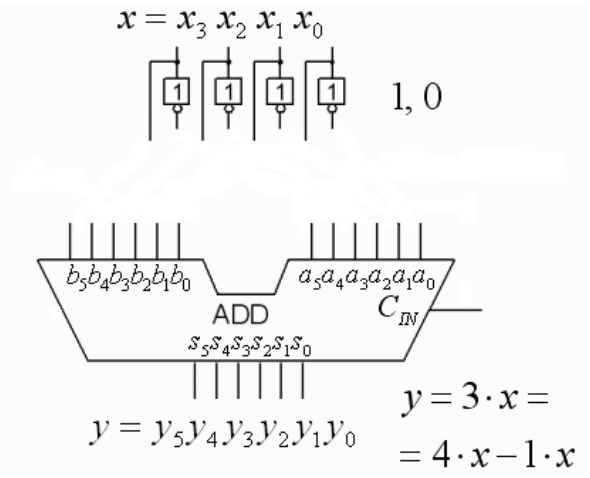
Minimize the function.

$$f(x, y, z)_{\min} = ?$$

2. 2p/1p/0p
A four bit unsigned integer x ($x_3x_2x_1x_0$) is to be multiplicated by the constant 3. $y = 3 \cdot x$.
The number x is connected to a six bit adder which is configured for the operation $3 \cdot x = 4 \cdot x + -1 \cdot x$

a) Suppose that the four bit number $x = 12$, which **six** bit number then represents $-x$
(in two complement representation)? Answer with a binary number.

b) Draw how the adder is to be configured. Exept the four bit in x there are also bits with the values 0 and 1 if needed. You will find a copy of the figure on the submission sheet.



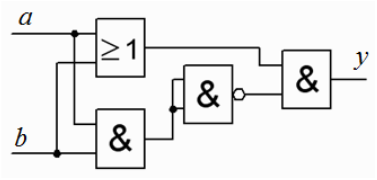
3. 1p/0p
Given is a Karnaugh map for a function of four variables $y = f(a, b, c, d)$. Write the function as a minimized sum of products, SP form. ”-” in the map means ”don’t care”.

a b \ c d	00	01	11	10
00	1	0	0	1
01	1	1	0	0
11	-	1	0	0
10	1	0	0	-

4. 1p/0p

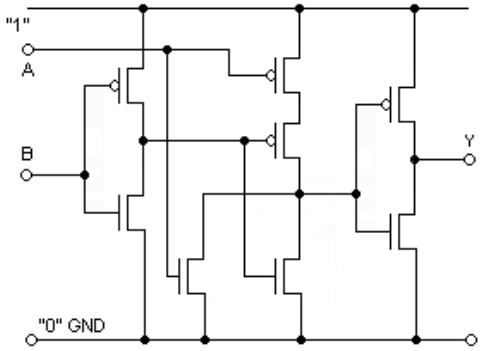
Write the logic function that is realized by the circuit as a minimized sum of products, SP form.

$y = f(a, b)$

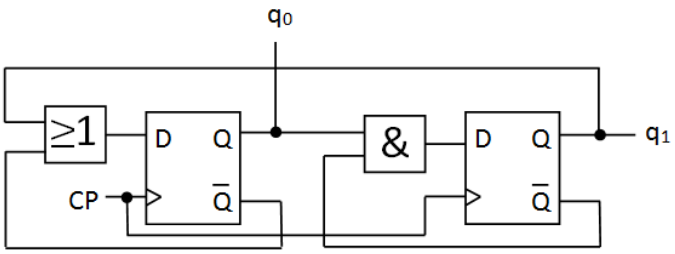


5. 1p/0p

Give an expression for the logical function realized by the CMOS circuit in the figure?



6. 1p/0p

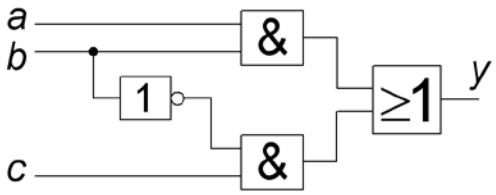


Sequence network starts in the state q_1q_0 00. Analyze the circuit and give the sequence for the following four clockpulses.

7. 2p/1p/0p
The circuit below is suffering from the hazard-phenomen.

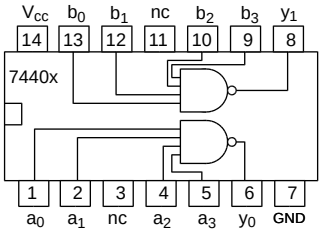
a) Write the logic function $y = f(a,b,c)$ that is realized by the circuit.

b) Which **product term** is to be added to the logical function y to prevent the hazard?



8. 1p/0p

The entity part of a VHDL-code describes the chip 7440x. (which is equivalent to the chip 7440, but with other names of the inputs and outputs). Unfortunately, some of the numbering of the logic vectors has become unreadable - correct this. (Correct the red question marks. The VHDL lines are also on the answer sheet).




```
ENTITY chip7440x IS
PORT (   a, b   : IN   STD_LOGIC_VECTOR( ? downto 0 ) ;
         y      : OUT  STD_LOGIC_VECTOR( ? downto 0 ) ;
END chip7440x ;
```

Part A2: Methods

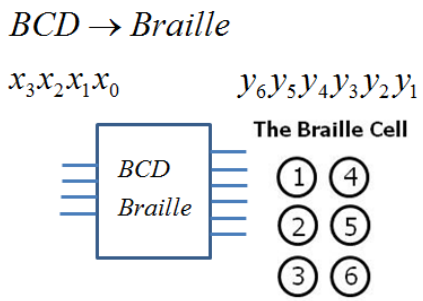
Note! Part A2 will only be corrected if you have passed part A1 (≥6p).

9. 5p

Displays for blind persons are using Braille cells with digitally controllable points (points feels like elevated to the finger when they are driven by logical 1).

You will design a combinatorial network which translates from the bit vector *x* in BCD code (the digits 0 to 9 binary coded), to the bit vector *y* in Braille alphabet numbers, see the table below.

Note that we restrict ourselves to only the digits 0 ... 9, no letters or other characters appear.



a/1	b/2	c/3	d/4	e/5	f/6	g/7	h/8	i/9	j/0
k	l	m	n	o	p	q	r	s	t
u	v	x	y	z					w

a) (1p) Derive the truth table for $y_6y_5y_4y_3y_2y_1 = f(x_3x_2x_1x_0)$.

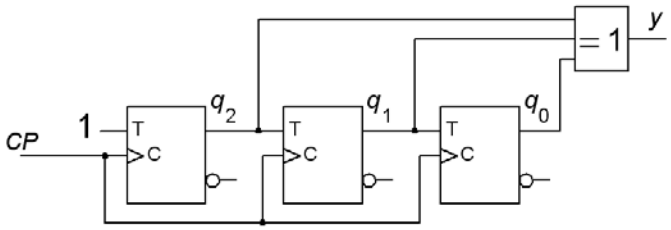
b) (1p) Develop the minimized expressions for y_6 y_5 y_4 y_3 y_2 y_1 (exploit don't care).

c) (1p) Realize the function y_1 with optional gates.. Draw the schematic.

d) (1p) Realize the function y_2 with only two and three - input NAND gates. Draw the schematic.

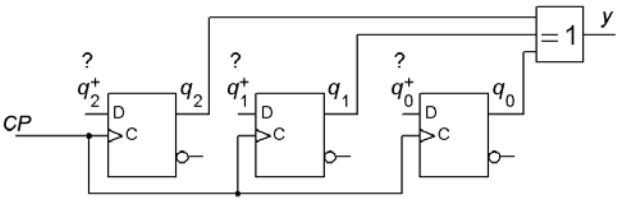
e) (1p) Realize the function y_5 with a 4: 1 MUX (can be solved without using any gates). Draw the schematic.

10. 5p. Analyze the following synchronous "shift register counter" with T-flip-flops.



a) (2p) Draw the counter **state diagram** (all 8 states). Derive the counter's **coded state table**.

b) (2p) Now implement the counter with D flip-flops instead of T the flip-flops.
Use your state table in a).



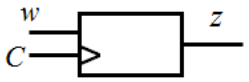
Derive the **minimized expressions** for the three D flip-flops **next state decoder**.
$q_2^+\ q_1^+\ q_0^+$ marked with "?" in the figure.

c) (1p) Draw the schematic for $q_2^+\ q_1^+\ q_0^+$ you may use optional gates.
(Inverted variables are available from the flip-flops)

Part B. Design Problems

Note! Part B will only be corrected if you have passed part A1+A2 (≥11p).

11. 6p. Sequence Detector.



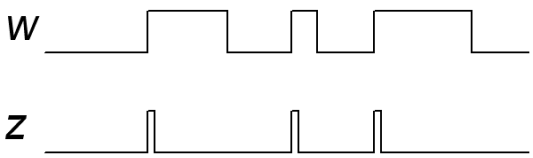
Obtain a minimal state table (show that it is minimal) for a synchronous sequential circuit of Moore-type with an input signal (*w*), and an output signal (*z*). The sequence net will generate the output 1 if it detects either input sequence 110 or 101, also overlapping sequences are valid (eg. 1101, is 110 followed by 101, will give output 00011). Derive the state diagram.

a) (4p) Set up the circuit's **state table**, **show** that it is **minimal**, and draw the **state diagram**.

b) (2p) Use Gray code to encode the states and set up the **encoded state table**. Obtain the **minimized expressions** for the **next state** and **output value**. No schematic of the circuit is needed to be drawn.

12. 4p Positive edge trigger.

Construct an asynchronous sequential circuit which at the change (0→1) of the input signal *w* generates a short pulse at the output *z*. For other input events the output should be $z = 0$. Output pulse length is given by the time for the transition state in the asynchronous sequential circuit. See timing diagram for clarification.



Your answer must include a **state diagram**, if necessary minimized, a **flow table**, and an appropriate **state assignment** with a **excitation table** that gives race-free net. You must also develop the hazard-free expressions for the **next state** and an expression for the **output**, and draw the gate circuit. It's free to use any type of gates.

Good Luck!

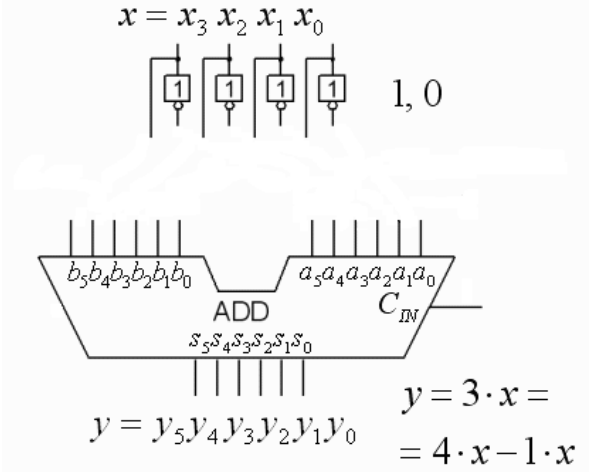
Submission sheet for Part A1 Sheet 1

(remove and hand in together with your answers for part A2 and part B)

Last Name: _____ **Given Name:** _____

Personal code number: _____

Write down your answers for the questions from Part A1 (1 to 8)

Question	Answer	
1	$f(x,y,z)_{\min} = ?$	
2	**a)** $x = 12$, what **six bit** two complement number represents $-x$? Answer with the binary number.	**b)** multiplication by the constant 3 (as 4-1). 
3	$y = f(a,b,c,d) = \{SoP\}_{\min} = ?$	
4	$y = f(a,b) = ?$	
5	$Y = f(A,B) = ?$	
6	$q_1 q_0$ 00,	
7	a) function $y = f(a,b,c)$ b) product-term?	

8	`ENTITY chip7440x IS`
	`PORT ( a, b : IN STD_LOGIC_VECTOR( ? downto 0 ) ;`
	`y : OUT STD_LOGIC_VECTOR( ? downto 0 ) ;`
	`END chip7440x ;`	

This table is completed by the examiner!!

Part A1	Part A2		Part B		Total	
Points	9	10	11	12	Sum	Grade