# DATA SHEET

# 74HC08; 74HCT08

# Quad 2-input AND gate

Product specification

Supersedes data of 1990 Dec 01

2003 Jul 25

**Philips**
**Semiconductors**

**PHILIPS**

# Quad 2-input AND gate

# 74HC08; 74HCT08

## FEATURES

- Complies with JEDEC standard no. 8-1A
- ESD protection:
  HBM EIA/JESD22-A114-A exceeds 2000 V
  MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from −40 to +85 °C and −40 to +125 °C.

## DESCRIPTION

The 74HC/HCT08 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A. The 74HC/HCT08 provide the 2-input AND function.

## QUICK REFERENCE DATA

GND = 0 V; $T_{amb}$ = 25 °C; $t_r$ = $t_f$ = 6 ns.

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | | UNIT |
|---|---|---|---|---|---|
| | | | **74HC08** | **74HCT08** | |
| $t_{PHL}$/$t_{PLH}$ | propagation delay nA, nB to nY | $C_L$ = 15 pF; $V_{CC}$ = 5 V | 7 | 11 | ns |
| $C_I$ | input capacitance | | 3.5 | 3.5 | pF |
| $C_{PD}$ | power dissipation capacitance per gate | notes 1 and 2 | 10 | 20 | pF |

**Notes**

1. $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in μW).

   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

   $f_i$ = input frequency in MHz;

   $f_o$ = output frequency in MHz;

   $C_L$ = output load capacitance in pF;

   $V_{CC}$ = supply voltage in Volts;

   N = total load switching outputs;

   $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

2. For 74HC08: the condition is $V_I$ = GND to $V_{CC}$.

   For 74HCT08: the condition is $V_I$ = GND to $V_{CC}$ − 1.5 V.

## FUNCTION TABLE

| INPUT | | OUTPUT |
|---|---|---|
| **nA** | **nB** | **nY** |
| L | L | L |
| L | H | L |
| H | L | L |
| H | H | H |

**Note**

1. H = HIGH voltage level;

   L = LOW voltage level.

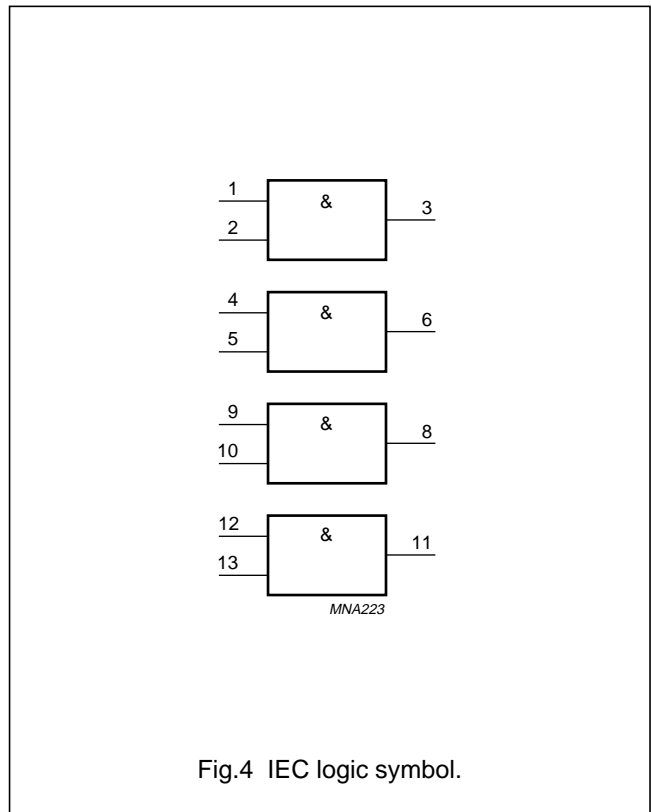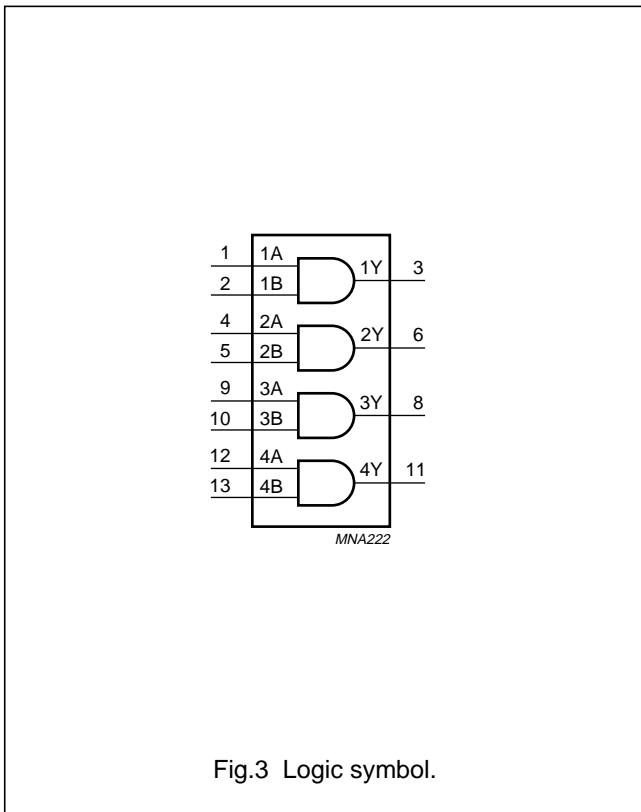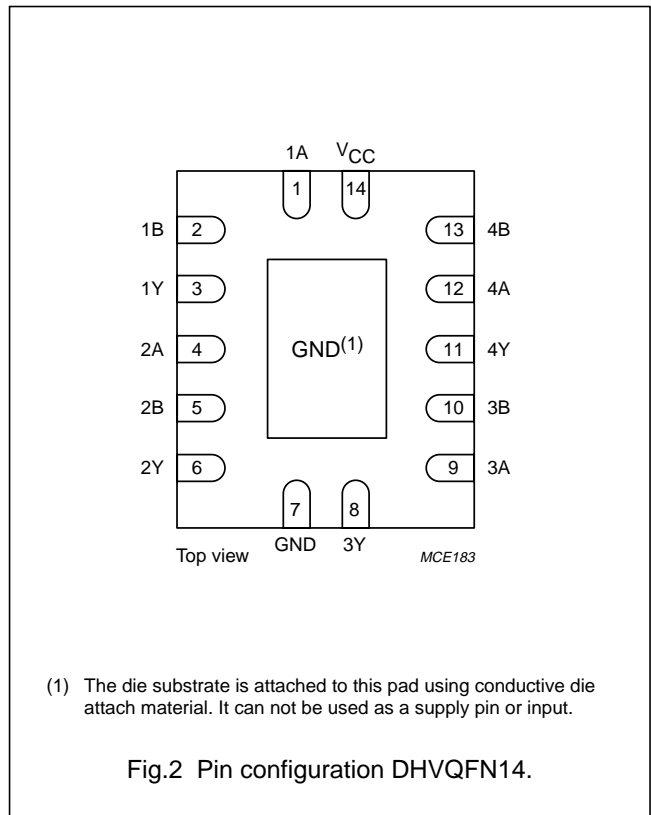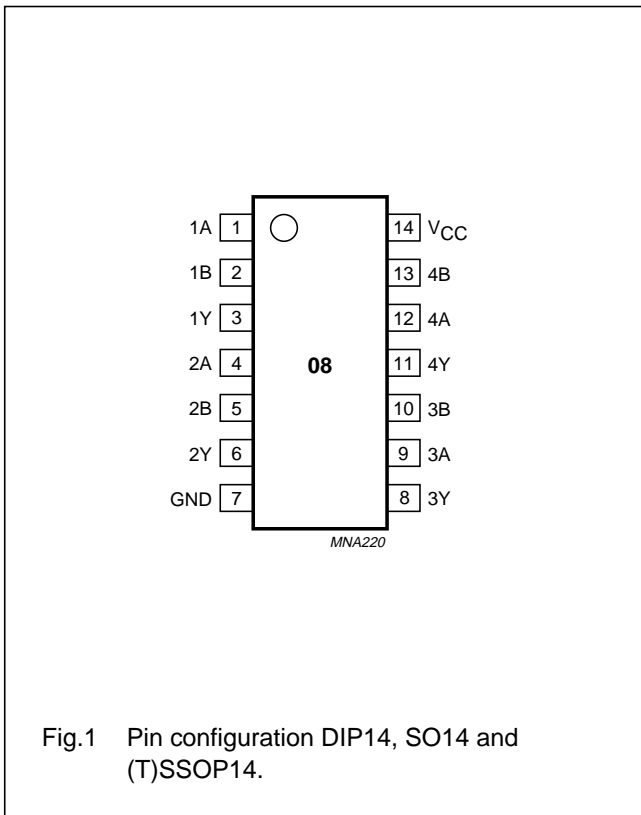## Quad 2-input AND gate

74HC08; 74HCT08

### ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | | | |
|---|---|---|---|---|---|
| | TEMPERATURE RANGE | PINS | PACKAGE | MATERIAL | CODE |
| 74HC08N | −40 to +125 °C | 14 | DIP14 | plastic | SOT27-1 |
| 74HCT08N | −40 to +125 °C | 14 | DIP14 | plastic | SOT27-1 |
| 74HC08D | −40 to +125 °C | 14 | SO14 | plastic | SOT108-1 |
| 74HCT08D | −40 to +125 °C | 14 | SO14 | plastic | SOT108-1 |
| 74HC08DB | −40 to +125 °C | 14 | SSOP14 | plastic | SOT337-1 |
| 74HCT08DB | −40 to +125 °C | 14 | SSOP14 | plastic | SOT337-1 |
| 74HC08PW | −40 to +125 °C | 14 | TSSOP14 | plastic | SOT402-1 |
| 74HCT08PW | −40 to +125 °C | 14 | TSSOP14 | plastic | SOT402-1 |
| 74HC08BQ | −40 to +125 °C | 14 | DHVQFN14 | plastic | SOT762-1 |
| 74HCT08BQ | −40 to +125 °C | 14 | DHVQFN14 | plastic | SOT762-1 |

### PINNING

| PIN | SYMBOL | DESCRIPTION |
|---|---|---|
| 1 | 1A | data input |
| 2 | 1B | data input |
| 3 | 1Y | data output |
| 4 | 2A | data input |
| 5 | 2B | data input |
| 6 | 2Y | data output |
| 7 | GND | ground (0 V) |
| 8 | 3Y | data output |
| 9 | 3A | data input |
| 10 | 3B | data input |
| 11 | 4Y | data output |
| 12 | 4A | data input |
| 13 | 4B | data input |
| 14 | $V_{CC}$ | supply voltage |

Quad 2-input AND gate

74HC08; 74HCT08

Fig.1    Pin configuration DIP14, SO14 and (T)SSOP14.

1A 1
1B 2
1Y 3
2A 4
2B 5
2Y 6
GND 7
**08**
14 $V_{CC}$
13 4B
12 4A
11 4Y
10 3B
9 3A
8 3Y

*MNA220*

Fig.2  Pin configuration DHVQFN14.

1A    $V_{CC}$
1     14

1B 2
1Y 3
2A 4
2B 5
2Y 6
$GND^{(1)}$
13 4B
12 4A
11 4Y
10 3B
9 3A

7    8
GND   3Y

Top view              *MCE183*

(1)   The die substrate is attached to this pad using conductive die attach material. It can not be used as a supply pin or input.

Fig.3  Logic symbol.

1   1A
2   1B      1Y   3

4   2A
5   2B      2Y   6

9   3A
10  3B      3Y   8

12  4A
13  4B      4Y   11

*MNA222*

Fig.4  IEC logic symbol.

1
2       &       3

4
5       &       6

9
10      &       8

12
13      &       11

*MNA223*

## Quad 2-input AND gate

## 74HC08; 74HC T08



Fig.5  HC logic diagram (one gate).



Fig.6  HCT logic diagram (one gate).

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | CONDITIONS | 74HC08 | | | 74HCT08 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. | |
| $V_{CC}$ | supply voltage | | 2.0 | 5.0 | 6.0 | 4.5 | 5.0 | 5.5 | V |
| $V_I$ | input voltage | | 0 | – | $V_{CC}$ | 0 | – | $V_{CC}$ | V |
| $V_O$ | output voltage | | 0 | – | $V_{CC}$ | 0 | – | $V_{CC}$ | V |
| $T_{amb}$ | ambient temperature | see DC and AC characteristics per device | −40 | +25 | +125 | −40 | +25 | +125 | °C |
| $t_r$, $t_f$ | input rise and fall times | $V_{CC}$ = 2.0 V | – | – | 1000 | – | – | – | ns |
| | | $V_{CC}$ = 4.5 V | – | 6.0 | 500 | – | 6.0 | 500 | ns |
| | | $V_{CC}$ = 6.0 V | – | – | 400 | – | – | – | ns |

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | −0.5 | +7.0 | V |
| $I_{IK}$ | input diode current | $V_I$ < −0.5 V or $V_I$ > $V_{CC}$ + 0.5 V | – | ±20 | mA |
| $I_{OK}$ | output diode current | $V_O$ < −0.5 V or $V_O$ > $V_{CC}$ + 0.5 V | – | ±20 | mA |
| $I_O$ | output source or sink current | −0.5 V < $V_O$ < $V_{CC}$ + 0.5 V | – | ±25 | mA |
| $I_{CC}$, $I_{GND}$ | $V_{CC}$ or GND current | | – | ±50 | mA |
| $T_{stg}$ | storage temperature | | −65 | +150 | °C |
| $P_{tot}$ | power dissipation | | | | |
| | DIP14 package | $T_{amb}$ = −40 to +125 °C; note 1 | – | 750 | mW |
| | other packages | $T_{amb}$ = −40 to +125 °C; note 2 | – | 500 | mW |

## Notes

1.  For DIP14 packages: above 70 °C derate linearly with 12 mW/K.

2.  For SO14 packages: above 70 °C derate linearly with 8 mW/K.

    For SSOP14 and TSSOP14 packages: above 60 °C derate linearly with 5.5 mW/K.

    For DHVQFN14 packages: above 60 °C derate linearly with 4.5 mW/K.

## Quad 2-input AND gate

### DC CHARACTERISTICS

#### Family 74HC08

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| SYMBOL | PARAMETER | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| | | OTHER | $V_{CC}$ (V) | | | | |
| **$T_{amb}$ = 25 °C** | | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | | 2.0 | 1.5 | 1.2 | – | V |
| | | | 4.5 | 3.15 | 2.4 | – | V |
| | | | 6.0 | 4.2 | 3.2 | – | V |
| $V_{IL}$ | LOW-level input voltage | | 2.0 | – | 0.8 | 0.5 | V |
| | | | 4.5 | – | 2.1 | 1.35 | V |
| | | | 6.0 | – | 2.8 | 1.8 | V |
| $V_{OH}$ | HIGH-level output voltage | $V_I = V_{IH}$ or $V_{IL}$ | | | | | |
| | | $I_O = -20$ µA | 2.0 | 1.9 | 2.0 | – | V |
| | | $I_O = -20$ µA | 4.5 | 4.4 | 4.5 | – | V |
| | | $I_O = -4.0$ mA | 4.5 | 3.98 | 4.32 | – | V |
| | | $I_O = -20$ µA | 6.0 | 5.9 | 6.0 | – | V |
| | | $I_O = -5.2$ mA | 6.0 | 5.48 | 5.81 | – | V |
| $V_{OL}$ | LOW-level output voltage | $V_I = V_{IH}$ or $V_{IL}$ | | | | | |
| | | $I_O = 20$ µA | 2.0 | – | 0 | 0.1 | V |
| | | $I_O = 20$ µA | 4.5 | – | 0 | 0.1 | V |
| | | $I_O = 4.0$ mA | 4.5 | – | 0.15 | 0.26 | V |
| | | $I_O = 20$ µA | 6.0 | – | 0 | 0.1 | V |
| | | $I_O = 5.2$ mA | 6.0 | – | 0.16 | 0.26 | V |
| $I_{LI}$ | input leakage current | $V_I = V_{CC}$ or GND | 6.0 | – | 0.1 | ±0.1 | µA |
| $I_{OZ}$ | 3-state output OFF current | $V_I = V_{IH}$ or $V_{IL}$; $V_O = V_{CC}$ or GND | 6.0 | – | – | ±0.5 | µA |
| $I_{CC}$ | quiescent supply current | $V_I = V_{CC}$ or GND; $I_O = 0$ | 6.0 | – | – | 2 | µA |

## Quad 2-input AND gate

| SYMBOL | PARAMETER | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| | | OTHER | $V_{CC}$ (V) | | | | |
| **$T_{amb}$ = −40 to +85 °C** | | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | | 2.0 | 1.5 | – | – | V |
| | | | 4.5 | 3.15 | – | – | V |
| | | | 6.0 | 4.2 | – | – | V |
| $V_{IL}$ | LOW-level input voltage | | 2.0 | – | – | 0.5 | V |
| | | | 4.5 | – | – | 1.35 | V |
| | | | 6.0 | – | – | 1.8 | V |
| $V_{OH}$ | HIGH-level output voltage | $V_I = V_{IH}$ or $V_{IL}$ | | | | | |
| | | $I_O = -20 \mu A$ | 2.0 | 1.9 | – | – | V |
| | | $I_O = -20 \mu A$ | 4.5 | 4.4 | – | – | V |
| | | $I_O = -4.0$ mA | 4.5 | 3.84 | – | – | V |
| | | $I_O = -20 \mu A$ | 6.0 | 5.9 | – | – | V |
| | | $I_O = -5.2$ mA | 6.0 | 5.34 | – | – | V |
| $V_{OL}$ | LOW-level output voltage | $V_I = V_{IH}$ or $V_{IL}$ | | | | | |
| | | $I_O = 20 \mu A$ | 2.0 | – | – | 0.1 | V |
| | | $I_O = 20 \mu A$ | 4.5 | – | – | 0.1 | V |
| | | $I_O = 4.0$ mA | 4.5 | – | – | 0.33 | V |
| | | $I_O = 20 \mu A$ | 6.0 | – | – | 0.1 | V |
| | | $I_O = 5.2$ mA | 6.0 | – | – | 0.33 | V |
| $I_{LI}$ | input leakage current | $V_I = V_{CC}$ or GND | 6.0 | – | – | ±1.0 | μA |
| $I_{OZ}$ | 3-state output OFF current | $V_I = V_{IH}$ or $V_{IL}$; $V_O = V_{CC}$ or GND | 6.0 | – | – | ±5.0 | μA |
| $I_{CC}$ | quiescent supply current | $V_I = V_{CC}$ or GND; $I_O = 0$ | 6.0 | – | – | 20 | μA |

## Quad 2-input AND gate

## 74HC08; 74HCT08

| SYMBOL | PARAMETER | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
| --- | --- | --- | --- | --- | --- | --- | --- |
| | | OTHER | $V_{CC}$ (V) | | | | |
| $T_{amb}$ = −40 to +125 °C | | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | | 2.0 | 1.5 | – | – | V |
| | | | 4.5 | 3.15 | – | – | V |
| | | | 6.0 | 4.2 | – | – | V |
| $V_{IL}$ | LOW-level input voltage | | 2.0 | – | – | 0.5 | V |
| | | | 4.5 | – | – | 1.35 | V |
| | | | 6.0 | – | – | 1.8 | V |
| $V_{OH}$ | HIGH-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | |
| | | $I_O$ = −20 μA | 2.0 | 1.9 | – | – | V |
| | | $I_O$ = −20 μA | 4.5 | 4.4 | – | – | V |
| | | $I_O$ = −4.0 mA | 4.5 | 3.7 | – | – | V |
| | | $I_O$ = −20 μA | 6.0 | 5.9 | – | – | V |
| | | $I_O$ = −5.2 mA | 6.0 | 5.2 | – | – | V |
| $V_{OL}$ | LOW-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | |
| | | $I_O$ = 20 μA | 2.0 | – | – | 0.1 | V |
| | | $I_O$ = 20 μA | 4.5 | – | – | 0.1 | V |
| | | $I_O$ = 4.0 mA | 4.5 | – | – | 0.4 | V |
| | | $I_O$ = 20 μA | 6.0 | – | – | 0.1 | V |
| | | $I_O$ = 5.2 mA | 6.0 | – | – | 0.4 | V |
| $I_{LI}$ | input leakage current | $V_I$ = $V_{CC}$ or GND | 6.0 | – | – | ±1.0 | μA |
| $I_{OZ}$ | 3-state output OFF current | $V_I$ = $V_{IH}$ or $V_{IL}$; $V_O$ = $V_{CC}$ or GND | 6.0 | – | – | ±10.0 | μA |
| $I_{CC}$ | quiescent supply current | $V_I$ = $V_{CC}$ or GND; $I_O$ = 0 | 6.0 | – | – | 40 | μA |

## Quad 2-input AND gate

**Family 74HCT08**

At recommended operating conditions; voltages are referenced to GND (ground = 0).

| SYMBOL | PARAMETER | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| | | OTHER | $V_{CC}$ (V) | | | | |
| **$T_{amb}$ = 25 °C** | | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | | 4.5 to 5.5 | 2.0 | 1.6 | – | V |
| $V_{IL}$ | LOW-level input voltage | | 4.5 to 5.5 | – | 1.2 | 0.8 | V |
| $V_{OH}$ | HIGH-level output voltage | $V_I = V_{IH}$ or $V_{IL}$ | | | | | |
| | | $I_O = -20$ μA | 4.5 | 4.4 | 4.5 | – | V |
| | | $I_O = -4.0$ mA | 4.5 | 3.84 | 4.32 | – | V |
| $V_{OL}$ | LOW-level output voltage | $V_I = V_{IH}$ or $V_{IL}$ | | | | | |
| | | $I_O = 20$ μA | 4.5 | – | 0 | 0.1 | V |
| | | $I_O = 4.0$ mA | 4.5 | – | 0.15 | 0.26 | V |
| $I_{LI}$ | input leakage current | $V_I = V_{CC}$ or GND | 5.5 | – | – | ±0.1 | μA |
| $I_{OZ}$ | 3-state output OFF current | $V_I = V_{IH}$ or $V_{IL}$; $V_O = V_{CC}$ or GND; $I_O = 0$ | 5.5 | – | – | ±0.5 | μA |
| $I_{CC}$ | quiescent supply current | $V_I = V_{CC}$ or GND; $I_O = 0$ | 5.5 | – | – | 2 | μA |
| $\Delta I_{CC}$ | additional supply current per input | $V_I = V_{CC} - 2.1$ V; $I_O = 0$ | 4.5 to 5.5 | – | 60 | 216 | μA |
| **$T_{amb}$ = −40 to +85 °C** | | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | | 4.5 to 5.5 | 2.0 | – | – | V |
| $V_{IL}$ | LOW-level input voltage | | 4.5 to 5.5 | – | – | 0.8 | V |
| $V_{OH}$ | HIGH-level output voltage | $V_I = V_{IH}$ or $V_{IL}$ | | | | | |
| | | $I_O = -20$ μA | 4.5 | 4.4 | – | – | V |
| | | $I_O = -4.0$ mA | 4.5 | 3.84 | – | – | V |
| $V_{OL}$ | LOW-level output voltage | $V_I = V_{IH}$ or $V_{IL}$ | | | | | |
| | | $I_O = 20$ μA | 4.5 | – | – | 0.1 | V |
| | | $I_O = 4.0$ mA | 4.5 | – | – | 0.33 | V |
| $I_{LI}$ | input leakage current | $V_I = V_{CC}$ or GND | 5.5 | – | – | ±1.0 | μA |
| $I_{OZ}$ | 3-state output OFF current | $V_I = V_{IH}$ or $V_{IL}$; $V_O = V_{CC}$ or GND; $I_O = 0$ | 5.5 | – | – | ±5.0 | μA |
| $I_{CC}$ | quiescent supply current | $V_I = V_{CC}$ or GND; $I_O = 0$ | 5.5 | – | – | 20 | μA |
| $\Delta I_{CC}$ | additional supply current per input | $V_I = V_{CC} - 2.1$ V; $I_O = 0$ | 4.5 to 5.5 | – | – | 270 | μA |

Quad 2-input AND gate

74HC08; 74HCT08

| SYMBOL | PARAMETER | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| | | OTHER | $V_{CC}$ (V) | | | | |
| **$T_{amb}$ = −40 to +125 °C** | | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | | 4.5 to 5.5 | 2.0 | − | − | V |
| $V_{IL}$ | LOW-level input voltage | | 4.5 to 5.5 | − | − | 0.8 | V |
| $V_{OH}$ | HIGH-level output voltage | $V_I = V_{IH}$ or $V_{IL}$ | | | | | |
| | | $I_O = −20$ µA | 4.5 | 4.4 | − | − | V |
| | | $I_O = −4.0$ mA | 4.5 | 3.7 | − | − | V |
| $V_{OL}$ | LOW-level output voltage | $V_I = V_{IH}$ or $V_{IL}$ | | | | | |
| | | $I_O = 20$ µA | 4.5 | − | − | 0.1 | V |
| | | $I_O = 4.0$ mA | 4.5 | − | − | 0.4 | V |
| $I_{LI}$ | input leakage current | $V_I = V_{CC}$ or GND | 5.5 | − | − | ±1.0 | µA |
| $I_{OZ}$ | 3-state output OFF current | $V_I = V_{IH}$ or $V_{IL}$; $V_O = V_{CC}$ or GND; $I_O = 0$ | 5.5 | − | − | ±10 | µA |
| $I_{CC}$ | quiescent supply current | $V_I = V_{CC}$ or GND; $I_O = 0$ | 5.5 | − | − | 40 | µA |
| $\Delta I_{CC}$ | additional supply current per input | $V_I = V_{CC} − 2.1$ V; $I_O = 0$ | 4.5 to 5.5 | − | − | 294 | µA |

Quad 2-input AND gate

74HC08; 74HCT08

## AC CHARACTERISTICS

### Family 74HC08
GND = 0 V; $t_f = t_f$ = 6 ns; $C_L$ = 50 pF.

| SYMBOL | PARAMETER | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|--------|-----------|-----------|---------|------|------|------|------|
| | | WAVEFORMS | $V_{CC}$ (V) | | | | |
| **$T_{amb}$ = 25 °C** | | | | | | | |
| $t_{PHL}/t_{PLH}$ | propagation delay nA, nB to nY | see Figs 7 and 8 | 2.0 | – | 25 | 90 | ns |
| | | | 4.5 | – | 9 | 18 | ns |
| | | | 6.0 | – | 7 | 15 | ns |
| $t_{THL}/t_{TLH}$ | output transition time | see Figs 7 and 8 | 2.0 | – | 19 | 75 | ns |
| | | | 4.5 | – | 7 | 15 | ns |
| | | | 6.0 | – | 6 | 13 | ns |
| **$T_{amb}$ = −40 to +85 °C** | | | | | | | |
| $t_{PHL}/t_{PLH}$ | propagation delay nA, nB to nY | see Figs 7 and 8 | 2.0 | – | – | 115 | ns |
| | | | 4.5 | – | – | 23 | ns |
| | | | 6.0 | – | – | 20 | ns |
| $t_{THL}/t_{TLH}$ | output transition time | see Figs 7 and 8 | 2.0 | – | – | 95 | ns |
| | | | 4.5 | – | – | 19 | ns |
| | | | 6.0 | – | – | 16 | ns |
| **$T_{amb}$ = −40 to +125 °C** | | | | | | | |
| $t_{PHL}/t_{PLH}$ | propagation delay nA, nB to nY | see Figs 7 and 8 | 2.0 | – | – | 135 | ns |
| | | | 4.5 | – | – | 27 | ns |
| | | | 6.0 | – | – | 23 | ns |
| $t_{THL}/t_{TLH}$ | output transition time | see Figs 7 and 8 | 2.0 | – | – | 110 | ns |
| | | | 4.5 | – | – | 22 | ns |
| | | | 6.0 | – | – | 19 | ns |

## Quad 2-input AND gate

**Family 74HCT08**

GND = 0 V; $t_f = t_f = 6$ ns; $C_L = 50$ pF.

| SYMBOL | PARAMETER | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|---|
| | | WAVEFORMS | $V_{CC}$ (V) | | | | |
| **$T_{amb}$ = 25 °C** | | | | | | | |
| $t_{PHL}/t_{PLH}$ | propagation delay nA, nB to nY | see Figs 7 and 8 | 4.5 | – | 14 | 24 | ns |
| $t_{THL}/t_{TLH}$ | output transition time | see Figs 7 and 8 | 4.5 | – | 7 | 15 | ns |
| **$T_{amb}$ = −40 to +85 °C** | | | | | | | |
| $t_{PHL}/t_{PLH}$ | propagation delay nA, nB to nY | see Figs 7 and 8 | 4.5 | – | – | 30 | ns |
| $t_{THL}/t_{TLH}$ | output transition time | see Figs 7 and 8 | 4.5 | – | – | 19 | ns |
| **$T_{amb}$ = −40 to +125 °C** | | | | | | | |
| $t_{PHL}/t_{PLH}$ | propagation delay nA, nB to nY | see Figs 7 and 8 | 4.5 | – | – | 36 | ns |
| $t_{THL}/t_{TLH}$ | output transition time | see Figs 7 and 8 | 4.5 | – | – | 22 | ns |

**AC WAVEFORMS**
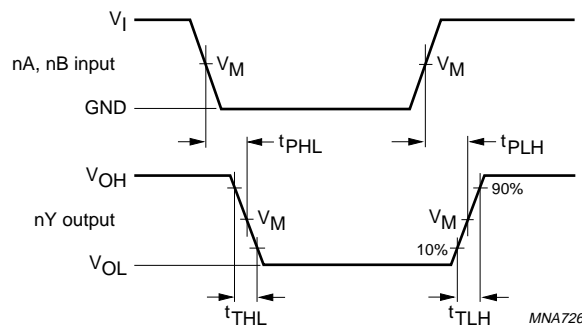
74HC08: $V_M$ = 50%; $V_I$ = GND to $V_{CC}$.
74HCT08: $V_M$ = 1.3 V; $V_I$ = GND to 3 V.

Fig.7  Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.

Quad 2-input AND gate                                        74HC08; 74HCT08
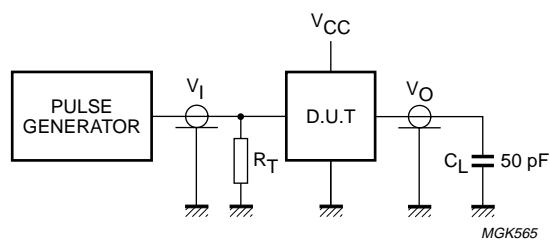


Definitions for test circuit:

$C_L$ = Load capacitance including jig and probe capacitance.

$R_T$ = Termination resistance should be equal to the output impedance $Z_o$ of the pulse generator.

Fig.8 Load circuitry for switching times.

## Quad 2-input AND gate

**PACKAGE OUTLINES**

**DIP14: plastic dual in-line package; 14 leads (300 mil)**

**SOT27-1**



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | A_1 min. | A_2 max. | b | b_1 | c | D (1) | E (1) | e | e_1 | L | M_E | M_H | w | Z (1) max. |
|------|--------|----------|----------|---|-----|---|-------|-------|---|-----|---|-----|-----|---|-----------|
| mm | 4.2 | 0.51 | 3.2 | 1.73 1.13 | 0.53 0.38 | 0.36 0.23 | 19.50 18.55 | 6.48 6.20 | 2.54 | 7.62 | 3.60 3.05 | 8.25 7.80 | 10.0 8.3 | 0.254 | 2.2 |
| inches | 0.17 | 0.02 | 0.13 | 0.068 0.044 | 0.021 0.015 | 0.014 0.009 | 0.77 0.73 | 0.26 0.24 | 0.1 | 0.3 | 0.14 0.12 | 0.32 0.31 | 0.39 0.33 | 0.01 | 0.087 |

**Note**

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|------|-------|---|---------------------|------------|
| | IEC | JEDEC | JEITA | | | |
| SOT27-1 | 050G04 | MO-001 | SC-501-14 | | | ~~99-12-27~~ 03-02-13 |

## Quad 2-input AND gate

## 74HC08; 74HCT08

**SO14: plastic small outline package; 14 leads; body width 3.9 mm**

**SOT108-1**



```
0        2.5        5 mm
|__|__|__|__|__|__|__|__|
          scale
```

**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | $\theta$ |
|------|--------|-------|-------|-------|-------|---|-----------|-----------|---|-------|---|-------|---|---|---|---|-----------|----------|
| mm | 1.75 | 0.25 0.10 | 1.45 1.25 | 0.25 | 0.49 0.36 | 0.25 0.19 | 8.75 8.55 | 4.0 3.8 | 1.27 | 6.2 5.8 | 1.05 | 1.0 0.4 | 0.7 0.6 | 0.25 | 0.25 | 0.1 | 0.7 0.3 | 8° 0° |
| inches | 0.069 | 0.010 0.004 | 0.057 0.049 | 0.01 | 0.019 0.014 | 0.0100 0.0075 | 0.35 0.34 | 0.16 0.15 | 0.05 | 0.244 0.228 | 0.041 | 0.039 0.016 | 0.028 0.024 | 0.01 | 0.01 | 0.004 | 0.028 0.012 | |

**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|-------|-------|---|---------------------|------------|
| | IEC | JEDEC | JEITA | | | |
| SOT108-1 | 076E06 | MS-012 | | | | ~~99-12-27~~ 03-02-19 |

Quad 2-input AND gate

74HC08; 74HCT08

**SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm**

**SOT337-1**



detail X

```
0        2.5        5 mm
|____|____|____|____|____|
         scale
```
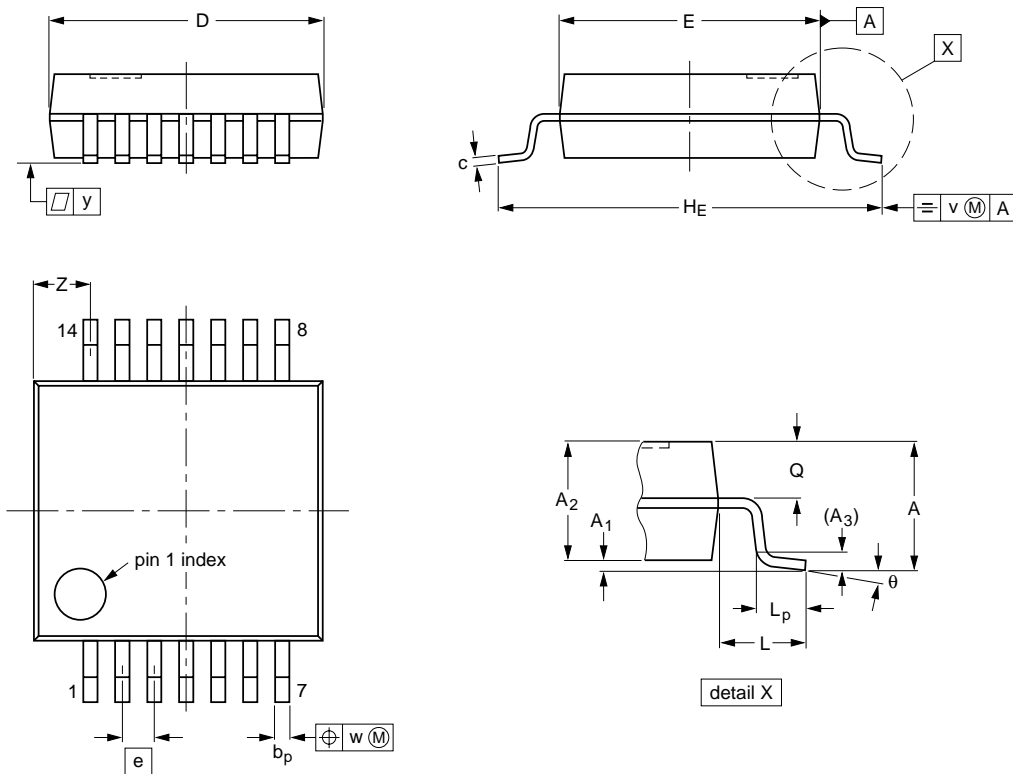
**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | A₁ | A₂ | A₃ | bₚ | c | D⁽¹⁾ | E⁽¹⁾ | e | H_E | L | Lₚ | Q | v | w | y | Z⁽¹⁾ | θ |
|------|--------|----|----|----|-----|---|------|------|---|-----|---|-----|---|---|---|---|------|---|
| mm | 2 | 0.21 0.05 | 1.80 1.65 | 0.25 | 0.38 0.25 | 0.20 0.09 | 6.4 6.0 | 5.4 5.2 | 0.65 | 7.9 7.6 | 1.25 | 1.03 0.63 | 0.9 0.7 | 0.2 | 0.13 | 0.1 | 1.4 0.9 | 8° 0° |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|-------|-------|--|---------------------|------------|
| | IEC | JEDEC | JEITA | | | |
| SOT337-1 | | MO-150 | | | | ~~99-12-27~~ 03-02-19 |

## Quad 2-input AND gate

## 74HC08; 74HCT08

**TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm**          **SOT402-1**



detail X

0          2.5          5 mm
scale
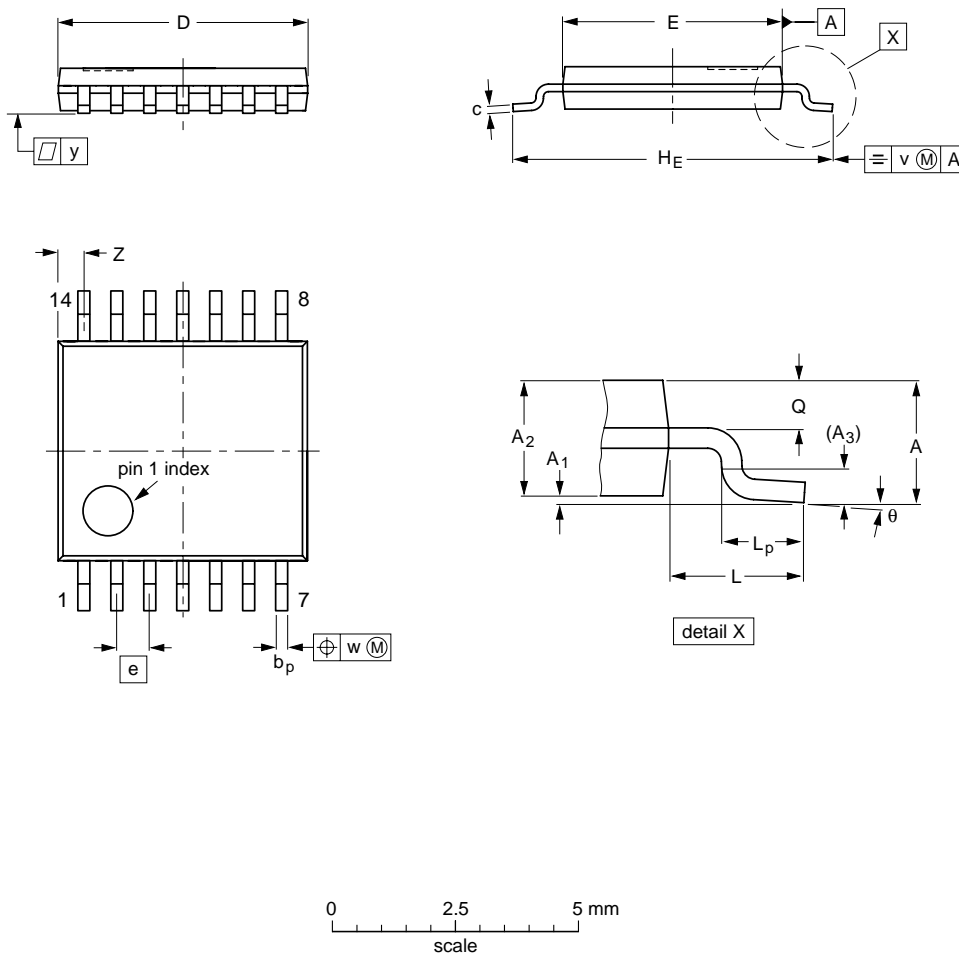
**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | A₁ | A₂ | A₃ | b_p | c | D (1) | E (2) | e | H_E | L | L_p | Q | v | w | y | Z (1) | θ |
|------|--------|-----|-----|------|------|-----|-------|-------|------|-----|---|------|-----|-----|------|-----|-------|----|
| mm | 1.1 | 0.15 0.05 | 0.95 0.80 | 0.25 | 0.30 0.19 | 0.2 0.1 | 5.1 4.9 | 4.5 4.3 | 0.65 | 6.6 6.2 | 1 | 0.75 0.50 | 0.4 0.3 | 0.2 | 0.13 | 0.1 | 0.72 0.38 | 8° 0° |

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|-------|-------|---|---------------------|------------|
| | IEC | JEDEC | JEITA | | | |
| SOT402-1 | | MO-153 | | | | ~~99-12-27~~ 03-02-18 |

## Quad 2-input AND gate

74HC08; 74HCT08

**DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;
14 terminals; body 2.5 x 3 x 0.85 mm** SOT762-1
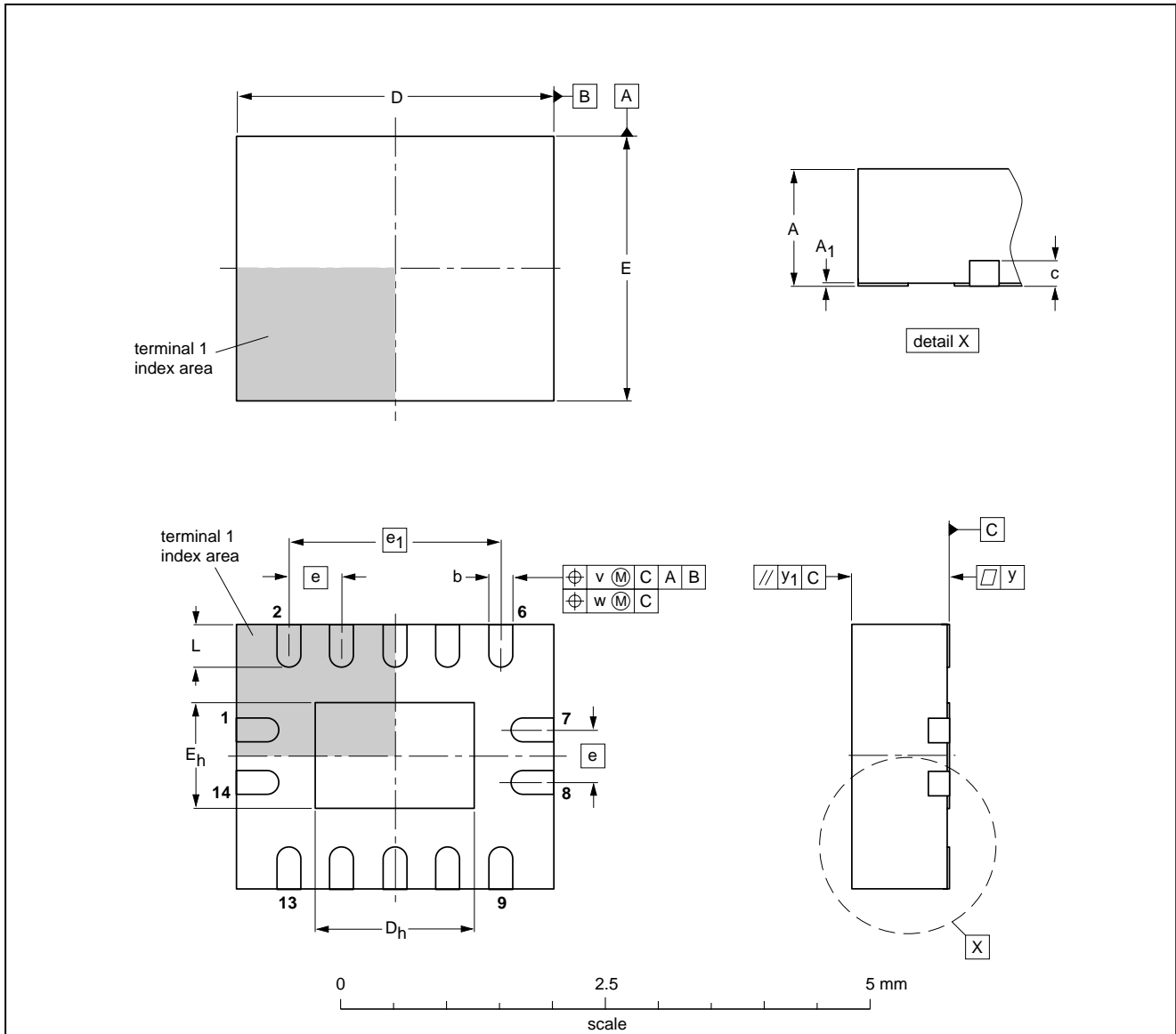


**DIMENSIONS (mm are the original dimensions)**

| UNIT | A[1] max. | A_1 | b | c | D[1] | D_h | E[1] | E_h | e | e_1 | L | v | w | y | y_1 |
|------|-----------|-----|---|---|------|-----|------|-----|---|-----|---|---|---|---|-----|
| mm | 1 | 0.05 0.00 | 0.30 0.18 | 0.2 | 3.1 2.9 | 1.65 1.35 | 2.6 2.4 | 1.15 0.85 | 0.5 | 2 | 0.5 0.3 | 0.1 | 0.05 | 0.05 | 0.1 |

**Note**

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|---|---|---|---------------------|------------|
| | IEC | JEDEC | JEITA | | | |
| SOT762-1 | - - - | MO-241 | - - - | | | ~~02-10-17~~ 03-01-27 |

Quad 2-input AND gate

74HC08; 74HCT08

**DATA SHEET STATUS**

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|-------|----------------------|----------------------|------------|
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