Mu2e CRV FEB

```
Addr  8 Word Header  : Note: Only 'RDB' cmd Updates Header
(06A) Spill WrdCnt+8 : 00000000  (0)
(066) Spill Trig Cnt : 00000000  (0)
(068) Spill Cycle    : 0000      (0)
(021) Chan Mask Reg  : 0000
( uC) Board ID       : 0000
(076) Spill Status   : 0000   4=GateOpen, 2=EndOfSpill, 1=SeqBsy
---------------------
( 6A) Wrd Cnt FPGA0  :00001800        CSR0=0000
(46A) Wrd Cnt FPGA1  :00001800        CSR1=0000
(86A) Wrd Cnt FPGA2  :00000000        CSR2=0003
(C6A) Wrd Cnt FPGA3  :00000000        CSR3=0003
---------------------
( uC) Total Word Cnt : 3000
( uC) LastUserReqSiz : 0
( uC) UserReq OvrRun : 0
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FPGA0 WrdCnt  sLEN=254(D)* 4 *TRGs=0(D) +TRGs*8(eHDR)= 0
FPGA1 WrdCnt  sLEN=254(D)* 4 *TRGs=0(D) +TRGs*8(eHDR)= 0
FPGA2 WrdCnt  MaskBits=0  (No valid data)
FPGA3 WrdCnt  MaskBits=0  (No valid data)

-------- fpga regs --------
(002) SDRam Wr Ptr   : 3000
(004) SDRam Rd Ptr   : 820
(023) Test Counter   : 1F
(072) Time Stamp     : 11DB2EB1
(074) Pulse Trg Dly  : 0
(075) Spill Error    : 0
(300) FlashGate CSR  : 0
(301) FlshGate ON nS : 0.00
(302) FlshGate OFF nS: 0.00
(303) Trigger Cntrl  : 0
(304) PipeLine Dly nS: 200.96
(305) Sample Length  : FE
(306) Test Pulser    : 4B
(308) TstPulsLen(sec): 2
(309) TstPulsGap(sec): 4
--------- uC regs ---------
( uC) MuxChan        : 0
( uC) Trig Src  LEMO : 1
( uC) Link Dir  REC  : 0
( uC) ADC MUX Reg    : 10
( uC) BiasVolt Ch0   : 55.19
( uC) BiasVolt Ch1   : 5.47
( uC) BiasVolt Ch2   : 3.66
( uC) BiasVolt Ch3   : 3.68
( uC) BiasVolt Ch4   : 67.37
( uC) BiasVolt Ch5   : 46.58
( uC) BiasVolt Ch6   : 42.86
( uC) BiasVolt Ch7   : 43.76
```