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CRV FEB FPGA Register Map (word addresses)

There are four FPGAs on the FEB. The address space for each FPGA is offset by 0x400 from its neighbor.

0x000..0x3FF – FPGA1. CMB Inputs 1..4 *connected to HDMI inputs* 1..4
0x400..0x7FF – FPGA2. CMB Inputs 1..4 *connected to HDMI inputs* 5..8
0x800..0xBFF – FPGA3. CMB Inputs 1..4 *connected to HDMI inputs* 9..12
0xC00..0xFFF – FPGA4. CMB Inputs 1..4 *connected to HDMI inputs13*..16

0x000: Control and status register

Bit 0: Power Down AFE 0. 0: Run. 1: Power down.
Bit 1: Power Down AFE 1. 0: Run. 1: Power down.
Bit 2: Issue a reset to the AFE deserializer logic in the FPGA
Bit 3: Issue a MIG DDR interface reset
Bit 4: Reset readout sequencer 1: Reset, 0: No action
Bit 5: Issue a general reset. The AFE FIFOs, Trigger counter, Spill counter and Readout sequencer are reset.
Bit 6: Reset the serial controller in the AFE chips.
Bit 7: Clear FM receive parity error.
Bits15:8: Not presently defined.

15..8	7	6	5	4	3	2	1	0
Not Used	Clear FM Rx Parity Error	AFE Reset	General Reset	Force MIG DDR Write Command	Reset MIG DDR Interface	Reset AFE de-serializers	AFE 1 Power Down	AFE 0 Power Down

0x002: Set SDRam Write address upper bits

A write to this address defines the upper 12 bits of the SDRam byte write address

0x003: Set SDRam Write address lower bits

A write to this address defines the lower 16 bits of the SDRam byte write address.

0x004: Set SDRam Read address upper bits

A write to this address defines bits the upper 12 bits of the SDRam byte read address

0x005: Set SDRam Read address lower bits

A write to this address defines the lower 16 bits of the SDRam byte read address. At the end of this write cycle, the, the specified address is applied to the MIG command register and a burst read into the MIG read FIFO occurs.

0x006: Byte swapped SDRam read data port

Reads from this port will present data with the upper and lower bytes exchanged.

0x007: Un-swapped SDRam data port

Repeated writes to this address will pack two words into the MIG write FIFO and a write command will be issued after burst size number of long words have been written.
Repeated reads will unpack words from the MIG read FIFO and a burst read command will be issued after burst size number of long words have been read.

0x008: MIG Status Register

15..10	9	8	7	6	5	4	3	2	1	0
Not Used	Read Data FIFO Empty	Read Data FIFO Full	Read Command FIFO Empty	Read Command FIFO Full	Write Data Fifo Empty	Write Data FIFO Full	Write Command FIFO Empty	Write Command FIFO Full	DDR Cal Done	DDR Reset Busy

0x009: MIG FIFO Count

15..14	13..8	7..6	5..0
Not Used	MIG DDR Write Count	Not Used	MIG DDR Write Count

0x00A: MIG Burst Size

Presently fixed at 8 long words.

0x010: Histogram counter threshold for AFE 0

If the unsinged ADC value is above this 12 bit threshold and is above its adjacent samples, the AFE 0 histogram counter increments. A write to this value reset the counter and start the AFE 0 interval count down timer. The read back of this address will display the threshold in bits 11..0. Bit 12 reads back a '1' so long as the interval counter is > 0.

0x011: Histogram counter threshold for AFE 1

If the unsinged ADC value is above this 12 bit threshold and is above its adjacent samples, the AFE 1 histogram counter increments. A write to this value reset the counter and start the AFE 1 interval count down timer. . The read back of this address will display the threshold in bits 11..0. Bit 12 reads back a '1' so long as the interval counter is > 0.

0x012: Histogram count interval

A 12 bit counting interval in steps of 1 millisecond.

0x013: Histogram channel selector

A three bit register specifying which of the eight AFE channels is applied to the threshold.

0x014: AFE 0 Histogram count bits upper bits

Bits 23..16 of the AFE 0 histogram counter.

0x015: AFE 0 Histogram count bits lower bits

Bits 15..0 of the AFE 0 histogram counter.

0x016: AFE 0 Histogram count bits upper bits

Bits 23..16 of the AFE 1 histogram counter.

0x017: AFE 0 Histogram count bits lower bits

Bits 15..0 of the AFE 1 histogram counter.

0x020: I/V ADC Input Multiplexer control register

Selects which of 16 DAC trim resistors is connected to the lower level 16:1multiplexer. Set Mux enable to 0 before taking SiPM pulsed data. The top level 4:1 mux is controlled by the microprocessor. That mux has no disconnect option. The command Mux n where n is 0..3 chooses which lower level mux is connected to the PGA and 24 bit ADC. The microprocessor command A0 n will display n conversions of the 24 bit ADC.

15..5	4	3..0
Not Used	Mux Enable	Channel Select

0x021: Channel Mask Register

A four bit register to select which CMBs to read out. Bits 0..3 enable CMBs 1..4

0x022: Read/Write test Counter Bits 31...16

A write to this address defines the upper 16 bits of the 32 bit test counter. A read returns the present value of the upper bits.

0x023: Read/Write test Counter Bits 15...0

A write to this address defines the lower 16 bits of the 32 bit test counter. A read from this address displays the value of the lower order bits and increments all 32 bits of the counter after the read.

0x024: One wire command register

Bits 0..7: If an individual write transaction is requested, the lower eight bits of this register are sent to the one wire interface.

Bit 8: Start the read temperature sequencer. A complete read temperature sequence will execute when this bit is set. The read value of this bit will return a 0 until the sequence is complete.

Bit 9: Start the read ROM sequencer. A complete ROM read sequence will execute when this bit is set. The read value of this bit will return a 0 until the sequence is complete.

15..10	9	8	7..0
Not Used	Read ROM	Read Temperature	Command Byte

0x025: One wire control register

Bit 0..3: Selects which CMB read data is stored in the register file

Bit 4: Request a write transaction

Bit 5: Request a read transaction

Bit 6: Request a reset transaction

Bit 7: Transaction status. Returns a '1' when transaction is in progress

Bit 15..8: Transaction bitcount (N-1). For a write set to seven. For a 72 bit read set to 71.

15..8	7	6	5	4	3..0
Transaction bit count	Busy	Rst	Read	Write	CMB Sel

0x026..0x2A: One wire returned data register file

The contents depend on the specifics of the one wire transaction

0x02F: AFE Input FIFO empty flags

Shows the level of the empty flags of the 16 FIFOs used to buffer data destined for the DDR RAM.

0x030..0x3F: Bias trim DAC voltage setting

16 12 bit DACs with a span of ±4.096V.

0x040..0x43: LED flasher intensity DACs

Four 12 bit DACs with a span of 0..14V. Addresses 0x40..0x43 Apply to CMB 1..4.

0x044..0x45: Bias bus DACs

Two 12 bits DACs with a possible span of 0..80V. Address 0x44 applies to CMB1..2, Address 0x45 applies to CMB 3..4. The maximum voltage is in fact set by the bias generator jumper setting on the board. At the highest position the maximum bias voltage is about 76V.

0x046..0x47: AFE VGA DACs

Two 12 bits DACs with a span of 0..1.54V. Address 0x46 applies to AFE 1, Address 0x47 applies to AFE 2.

0x048..0x5F: DAC setup registers

These normally don't require modifying. For details see the AD5328 data sheet

0x066: Read the Spill Trigger Counter bits 31..16

Reads the number of triggers received during the spill

0x067: Read the Spill Trigger Counter bits 15..0

0x068: Read the Spill Counter

Increments once per spill. Use buffer reset to reset this counter

0x069: Read Event word count

Read the word count from the most recent event

0x06A: Read the Spill Word Counter bits 31..16

Reads the number of TDC words accumulated during the spill.

0x06B: Read the Spill Word Counter bits 15..0

0x06C: Uptime Counter bits 31...16

0x06D: Uptime Counter bits 15...0

A counter showing the number of seconds since the last FPGA reset

0x072: Time stamp bits 31...16

0x073: Timestamp bits 15...0

A register showing the time stamp of the most recent trigger

0x074: Pulser trigger delay value

An eight bit value in steps of 6.28ns that specifies the delay between receipt of a pulser trigger command from the controller and the issuing of a test pulse to the CMB LEDs. The desire is to obviate the need for pipeline readjustment between data taking and pulser triggers.

0x075: Read the Spill Error register

Bit 0: One or more of the AFE FIFOs has overflowed.
Bit 1: The above FIFO is empty. This should be the case at the end of spill.
Bit 2: Parity error on the command link from the controller to the TDC.

15..3	2	1	0
Not Used	Command Link Parity Error	Event FIFO Empty	Event FIFO Overflow

0x076: Read the Spill State register

Bit 0: The DDR write sequencer is busy.
Bit 1: Spill End Flag.
Bit 2: Spill Gate.

15..3	2	1	0
Not Used	Spill Gate	Spill End Flag	DDR Write Seq Busy

0x080..0x8F: Read of individual AFE FIFOs

A diagnostic to check AFE data without the readout sequencer.

0x0FF: AFE setup data read register

Data returned from an AFE in response to a read request is stored here.

0x100..0x13B: AFE 1 register file

This space is mapped onto to the AFE5807 register map..

0x200..0x23B: AFE 2 register file

Broadcast Addresses

A write to these addresses will set the corresponding registers in all four FPGAs at once. Reads are still individual to each FPGA. This is a way of checking that the broadcast did actually occur.

0x300: Flash gate control register

Bit 0: Enable the flash gate
Bit 1: Select the CMB pulse routing. 0: Flash Gate, 1: LED flasher.
Bit 2: LED Flasher signal source. 0: Test pulser, 1: Flash Gate.

15..3	2	1	0
Not Used	LED Source	CMB Pulse Select	Flash Gate Enable

0x301: Flash Gate Turn on tine

A write to this address defines the time in the microbunch in steps of 6.28ns that the flash gate is asserted, that is when the SiPM voltage is lowered. The microbunch duration is 270 steps.

0x302: Flash Gate Turn off tine

A write to this address defines the time in the microbunch in steps of 6.28ns that the flash gate is de-asserted, that is when the SiPM voltage is raised.

0x303: Trigger Control Register

Bit 0: Writing a '1' to this bit position sends a software trigger.
Bit 1: Selects the trigger input type as a pulse or an FM data stream
The assumption is that a trigger pulse comes from the LEMO connector, the FM encoded trigger message comes from the RJ-45 connector. The microprocessor controls the multiplexer that routes either the LEMO or the RJ-45 signal to the trigger input on the FPGAs.
Bit 2: Trigger Inhibit. If trigger inhibit is enabled, this bit goes to one in response to a trigger.
Bit 3: Trigger Inhibit enable.
Bit 4: Spill Inhibit. If spill inhibit is enabled, this bit goes to one in response to end of spill.
Writing a '1' to this position sets a request to clear the inhibit. Clear spill inhibit will wait until any spill in progress finishes before clearing and allow more triggers.
Bit 6: Spill Inhibit enable.
Bit 7: Not used.
Bit 8: Enable the on card test pulser
Bit 9: Run the test pulser for one spill or continuously
1: Run once 0: Run continuously

15..5	9	8	7	6	5	4	3	2	1	0
Not Used	Single Step/ Free Run	Test Pulse Enable	Not Used	Spill Inhibit Enable	Clear Spill Inhibit Request	Spill Inhibit	Trigger Inhibit Enable	Trigger Inhibit	Trigger source	Software Trigger

0x304: Hit Pipeline Delay Register

Specifies the number of pipeline stages the hit data traverses before being presented to the first level FIFO. This is used to compensate for trigger delays. The least count is 12.56 ns and the span is eight bits. The minimum delay setting is one and increases monotonically up to a setting of 255. A setting of zero corresponds to a delay of 256 or 3.22μs.

0x305: Sample length Register

Specifies the number ADC samples per trigger to record. 1..254 Samples.

0x306: Read/Write upper byte of the Test Pulser frequency word

A write to this address defines the upper 16 bits of the test pulser repetition rate.

0x307: Read/Write lower word of the Test Pulser frequency word

A write to this address defines the lower 16 bits of the test pulser repetition rate. The rate is 0.0741 Hz per count.

0x308: Test pulser spill duration

A write to this address defines the length of the internally generated spill in seconds

0x309: Test pulser interspill spill duration

A write to this address defines the length of the internally generated gap between spills in seconds. This is only significant if the test pulser is set to run continuously.